Signal Integrity Tips and Techniques
Using TDR, VNA and Modeling

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Simulation
What is the Signal Integrity Challenge?
How does simulation help?

• Distributed Model of the Physical Channel

• Using simple simulations to interpret TDR, TDT, and S-Parameters:
  • Stub Z discontinuity
  • Series Z discontinuity

• Simulation + Measurement = Insight
Example – SI Channel Degradation

Non-Ideal TX Data

Channel Degradation

Corrupt Data at RX
Distributed Model of the Physical Channel

PCI Express Channel Simulation

S-PARAMETERS

TDR
NEXT
FEXT

Package Fan-out
4in PCB Trace
Connector
12in PCB Trace
Package Fan-out

Impedance, Ohms

0 1 2 3 4 5 6
Time, nS

0.50
0.25
0.00
-0.25
-0.50
Voltage, V

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Impact of Rise Time on TDR

Reflection:
\[ \Gamma = \frac{Z_{\Delta x} - Z_0}{Z_{\Delta x} + Z_0} \]

for small R:
\[ Z = \frac{L}{\sqrt{C}} \]

Time Delay:
\[ TD_{\text{inch}} = vL \]
\[ v = \frac{\sqrt{dK}}{12 \text{ mils}} \]
Example FR4:
\[ = \frac{\sqrt{4}}{12} (100) \approx 17 \text{ ps} \]
< 25 ps Rise time

<table>
<thead>
<tr>
<th>Bit Rate</th>
<th>~1/10th Rise Time Feature Size</th>
<th>High Speed Feature Size</th>
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<tr>
<td>1 MBit</td>
<td>3 m (10 ft)</td>
<td>Matched Termination</td>
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<tr>
<td>10 MBit</td>
<td>30 cm (12 in)</td>
<td>T-Line Zo</td>
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<tr>
<td>100 MBit</td>
<td>3 cm (1.2 in)</td>
<td>Connector Zo</td>
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<tr>
<td>1 GBit</td>
<td>3 mm (120 mils)</td>
<td>Passive SMT Zo</td>
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<tr>
<td>5 GBit</td>
<td>0.6 mm (24 mils)</td>
<td>Via Zo</td>
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<td>10 GBit</td>
<td>0.3 mm (12 mils)</td>
<td>Die, Package, PCB Co-sim</td>
</tr>
<tr>
<td>40 GBit</td>
<td>0.075 mm (6 mils)</td>
<td>Machining Tolerances</td>
</tr>
</tbody>
</table>

Zpeak = 35 ohms
Simple simulations benefit analysis of TDR/TDT measurements.

**Stub Resonance**

- Input Port 1: 50 mm
- 7.5 mm Stub
- Output Port 2: 25 mm

**Series Resonance**

- Input Port 1: 50 mm
- 7.5 mm
- Output Port 2: 25 mm

**T-Line Model for Simulation**

- Input Port 1: 50 mm
- Stub: 7.5 mm
- Output Port 2: 25 mm

**Fast Frequency Domain Sweep**
Series Impedance Discontinuity
Time and Frequency Domain Analysis

Physical Layout

L < Rising Edge

L > Rising Edge

Time Domain Reflectometry

Zmin = 34 ohms

Zmin = 24 ohms

Frequency Domain Insertion Loss

25 ohm Discontinuity with Length from 25 mm to 1 mm

1 mm
25 mm

Real World Eye at 5 GB/s, PRBS 7

1mm Mismatch

25 mm Mismatch

Signal Loss S21

freq, GHz

-10

-9

-8

-7

-6

-5

-4

-3

-2

-1

0

0

2

4

6

8

10

12

14

16

18

20

25 ohm, 25 mm Long Mismatch Impedance

25 ohm, 25 mm Long Mismatch Impedance
Stub Impedance Discontinuity
Time and Frequency Domain Analysis

Physical Layout
L < Rising Edge
L > Rising Edge

Time Domain Reflectometry
Zmin = 40 ohms
Zmin = 25 ohms

Real World Eye at 5 GB/s, PRBS 7

Frequency Domain Insertion Loss
50 Ohm Stub Length from 10mm to 1mm

VIA STUBS
A Closer Look at TDR vs TDT

Stub Resonance

50 mm  25 mm
input Port 1  output Port 2
7.5 mm Stub

Series Resonance

50 mm  7.5 mm  25 mm
input Port 1  output Port 2

Excess C and L Calculations

\[ C_{Total} = \frac{t_d}{Z_0} \]
\[ C = \frac{2\pi}{Z_0} = -\frac{2}{Z_0} \int_0^{+\infty} \text{reflected}_n \cdot dt \]
\[ L_{Total} = t_d Z_0 \]
\[ L = 2Z_0\tau = 2Z_0 \int_0^{+\infty} \text{reflected}_n \cdot dt \]

Integrate from Marker 4 to 5 to get
Excess C = 1.4 pF
Why is the TDT different for the same delta Z change?

Excess C is 1.4 pF and Z~ 26 ohms

Stub Resonance

Series Resonance

input Port 1 50 mm 25 mm output Port 2

input Port 1 50 mm 7.5 mm 25 mm output Port 2
Measurement Based T-Line Model for Debugging the Channel – Virtual Lab

TDR/TDT

ADS

Eric Bogatin’s “Hacking the Backplane”
Solving the Problem with Pre-Layout, Post-Layout, Measurement

Everyone believes measurements except for the person who made them...

No one believes simulations except for the person who made them...

Simulation + Measurement = Insight
Measurement
Agenda, “Finding the Causes of EMI and How TDR can Help”

– How do high speed serial designs typically cause EMI?
– In high speed serial designs, where do common currents come from?
– A quick overview of the DUT evaluated
– How can TDR Help address the EMI issue?
What Causes EMI?

- Of course, there are many potential causes of EMI but in high-speed serial designs one of the largest sources of EMI is radiation (that gets out of the box) from **common currents generated by a differential data channel**.

- The differential channel ideally has no common currents but it takes only a very small common signal to create an EMI issue.

- As a rule of thumb, to pass an FCC certification test the maximum allowable common signal on an external twisted pair should be < 10 mV at 1 GHz.
Agenda

– How do high speed serial designs typically cause EMI?
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Where do the common currents come from?

In theory, if the drivers produce a perfect differential signal (no common component) and the differential signal passes through a perfect differential channel, there will be NO common signal generated.

In practice that is **NEVER** the case!

Assuming the driver is perfect and we consider just the channel, any asymmetry in a coupled differential channel will convert some of the differential signal into a common signal. This is known as “Mode Conversion”.

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Mode Conversion

- Differential Signal in
- Differential Signal out (transmitted)
- Common Signal out (transmitted)

Port 1

Port 2

- $T_{DD21}$
- $T_{CD21}$
What Causes Mode Conversion in the Channel?

ANY asymmetries in the coupled lines can cause mode conversion:

- Non-equal line widths
- Non-equal line lengths
- Different “local” effective dielectric constants (even due to the glass weave in the laminate)
- A discontinuity in the ground plane

Let’s look at a real example
Agenda

– How do high speed serial designs typically cause EMI?
– In high speed serial designs, where do common currents come from?
– A quick overview of the DUT evaluated
– How can TDR Help address the EMI issue?
Using TDR to evaluate the channel:

TDR remote heads enable connecting directly to the DUT without the need for cables.
Using TDR to evaluate the channel: A quick look at the DUT

Via field in backplane

Via field in daughter card

Connector

Daughter Card SMA (end of DUT)
Agenda

– How do high speed serial designs typically cause EMI?
– In high speed serial designs, where do common currents come from?
– A quick overview of the DUT evaluated
– How can TDR Help address the EMI issue?
How can TDR help find the source of EMI issues?
Part 1: Is there mode conversion?

Start with a quick review of S-parameter terms

Stimulus (in)

\[ S_{CD21} \]

Response (out)
How can TDR help find the source of EMI issues?
Part 1: Is there mode conversion?

Differential Pair

Port 1  Differential Signal in

Port 2  Differential Signal out (transmitted)
         Common Signal out (transmitted)

Similar – but not exactly the same – signal velocity
How can TDR help find the source of EMI issues?

Part 1: Is there mode conversion? TDT

Port 1

Differential Pair

Port 2

Differential Signal in

Common Signal out (transmitted)

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How can TDR help find the source of EMI issues?

Part 1: Is there mode conversion? How dependent is it on edge speed?

Differential Pair

Port 1

Port 2

Stimulus Rise Time:
- 6 ps
- 36 ps
- 56 ps
- 76 ps
- 100 ps

Stimulus Rise Time (transmitted): TC21

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How can TDR help find the source of EMI issues?

Part 2: There is mode conversion; what is causing it?

This shows the position and magnitude of differential reflections.

Remember, velocities are similar.
How can TDR help find the source of EMI issues?
Part 2: There is mode conversion; what is causing it?

Port 1  Differential Pair  Port 2

Differential Signal in

Differential Reflection $T_{DD11}$

Common Reflection $T_{CD11}$

Via field in backplane
Via field in daughter card
1. Even a small Common Mode signal, if it gets “out of the box”, can cause EMI and possibly an FCC certification test failure.

2. Any asymmetries (line width, line length, local dielectric, discontinuity in the ground plane, etc.) in a coupled differential line can cause Mode Conversion.

3. The Differential and Common signals travel at similar velocities so comparing the reflected Differential signal ($T_{DD11}$, impedance profile) with the reflected Common signal, $T_{CD11}$, will show where/what in the DUT is causing the Mode Conversion.
Error Correction
Removing Fixtures

Historically – 2 methods:

- Model the fixture using EM Simulation and then de-embed the fixtures from the measurement
- Build a calibration kit (SOLT or TRL)
  - SOLT requires characterization of standards (difficult)
  - TRL is an easier calibration technique to move measurement reference planes to the DUT. (preferred method)
Assumptions for single ended TRL

- Connectors and launches are identical
- All lines have same Transmission Line characteristics
  - Impedance, loss, propagation
  - Only differ in length
- Lines are usable 20 to 160 degrees relative to thru
- No coupling in fixture is removed
- Usually 2-4 lines depending on frequency range
Differential Cross Talk Calibration aka Diff TRL

4-port TRL Calibration Technique
Fixture may be asymmetric
Similar assumptions to single ended TRL
  • Repeatability of connector, launch, and line
  • Lines are usable 20 to 160 degrees relative to thru
Additional differential constraints
  • $SDC_{nm}$ and $SCD_{nm} < -30$ dB
  • Skew between lines < 10 degrees
Coupling in fixture is removed
Example of Typical TRL Calibration Kits
Automatic Fixture Removal (2X THRU)

Yesterday TRL

Thru
Line 3
Line 2
Line 1
Open
DUT

Today AFR

Thru
or
Diff Thru

Note: Customers are now migrating from TRL to AFR after comparing results.
Automatic Fixture Removal (1-Port)

New:
- Open or Short
- Best when 2X THRU is hard to fab

Applications:
- Fast, easy and inexpensive to fabricate
- Smallest footprint
- PC board
  - measure unloaded board
  - load part and measure
- Probes
  - measure open and shorted
- Socketed packages
  - measure open fixture
  - measure loaded part
Differential Automatic Fixture Removal

Assumptions:

• 2X THRU can be Asymmetric in length and match
• Still needs to be Symmetric top to bottom with minimal mode conversion
• The return loss and insertion loss of the 2xThru cannot cross each other in the measurement frequency range, often at least 5 dB separation is required
• Impedance of fixture and 2X THRU calibration standard must be identical!
Differential **Automatic Fixture Removal**

Assumptions:
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Impedance of fixture and 2X THRU calibration standard must be identical!

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No longer a restriction in PLTS 2016!
Design Case Study - Mezzanine Connector
Design Case Study Objective

– A test-fixture is required to characterize connectors

– Standard test-fixture removal methods (TRL, AFR) have some issues
  
  • Do not take into account the impedance variations between the calibration structure and test-fixture

– In this design case study a new test-fixture removal method is introduced that overcomes (some of) the issues with standard test-fixture removal methods.
Design Case Study - Mezzanine Connector

Step 1

• Describe the test fixture

New enhancement when fixture impedance is different from 2X THRU

Note: Acknowledgements to Samtec for use of graphics
Design Case Study - Mezzanine Connector

Step 2

- Specify standards

Fixture A

Fixture B

Fixture A + DUT + Fixture B
Design Case Study- Mezzanine Connector

Step 3

• Measure the standards

Note: Use previously measured “Fixtured DUT” as calibration standard
Design Case Study- Mezzanine Connector

Step 4

• Remove the fixtures
Design Case Study- Mezzanine Connector

Step 5

- Save all files (de-embedded DUT and test fixtures models)
Comparison of Before and After AFR Enhancement in PLTS 2016

Non-causal behavior

causal behavior

Before

After
Conclusions

• Simulation, TDR, VNA with Error correction are all critically important
• New applications push state of the art test and measurement
• Simulation + Measurement = Insight only if the calibration is good

Thank You!

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