25Gb/s Ethernet Channel Design in Context:
Channel Operating Margin (COM)

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Agenda

- Backplane and Copper Cable Ethernet Interconnect
- Channel Compliance before IEEE 802.3bj
- What is COM?
- Examples of Signal Integrity Decisions
- “Simple” Interconnect Models have Opportunities for modeling improvements
- Questions?

Backplane Ethernet Syntax Example

<XX>BASE-KR and <XX>BASE-KR4

- **K** -> bacKplane
- <XX> for BASE-KR, example: 10G\40G\25G\100G
- Lane data rate by dividing number of lanes

Choice of MDI Interconnect. Left up to implementer

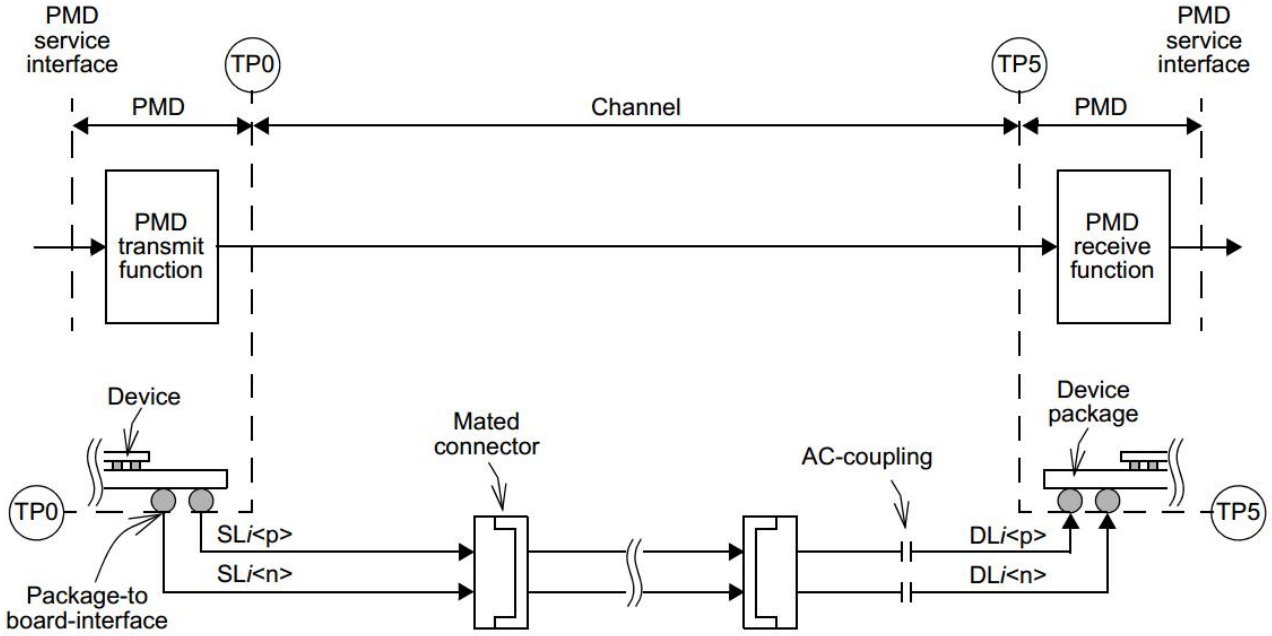
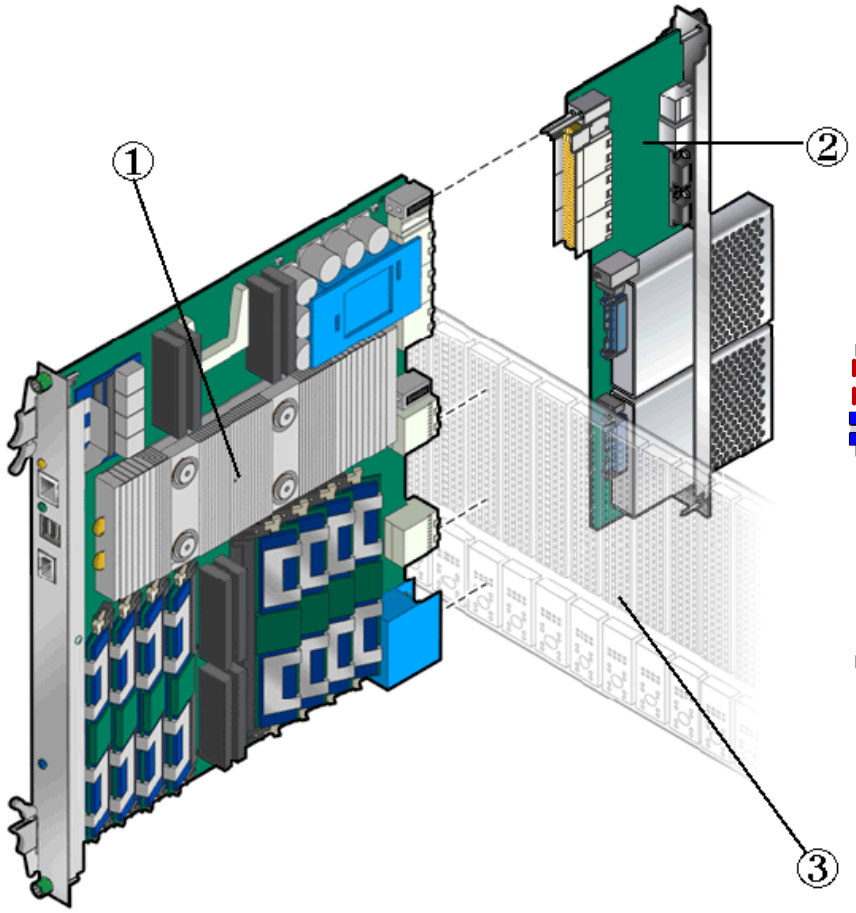


Figure 93–2—100GBASE-KR4 link (one direction for one lane is illustrated)

IEEE Std 802.3bj-2014

“Traditional” Backplane (“KR”)



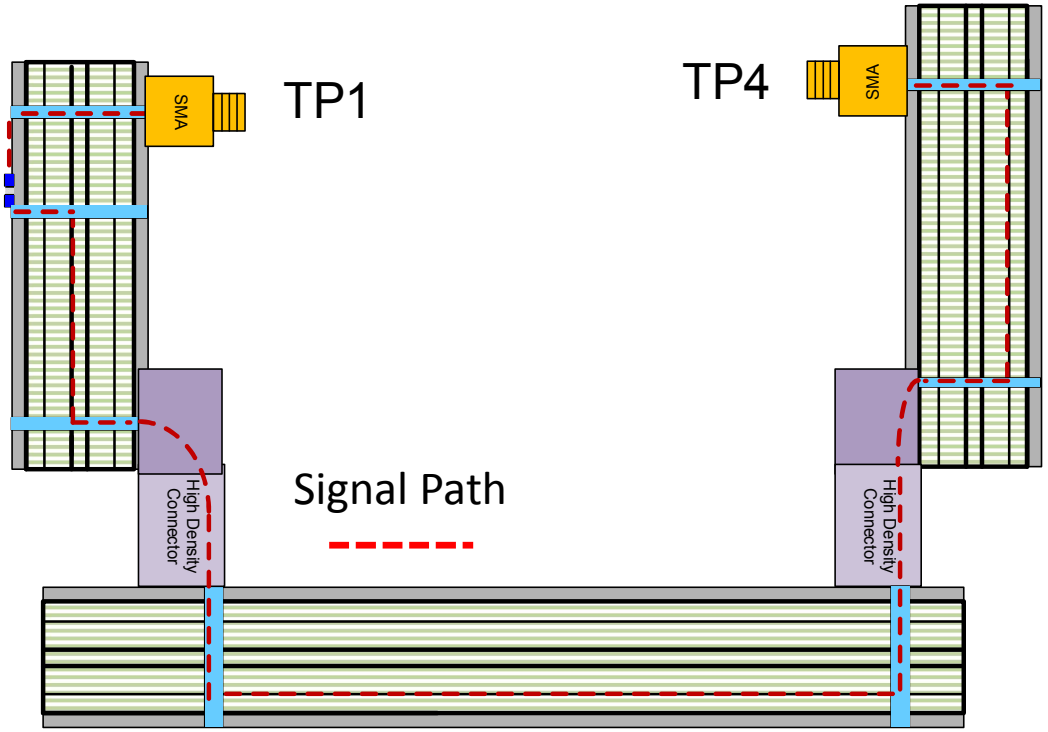
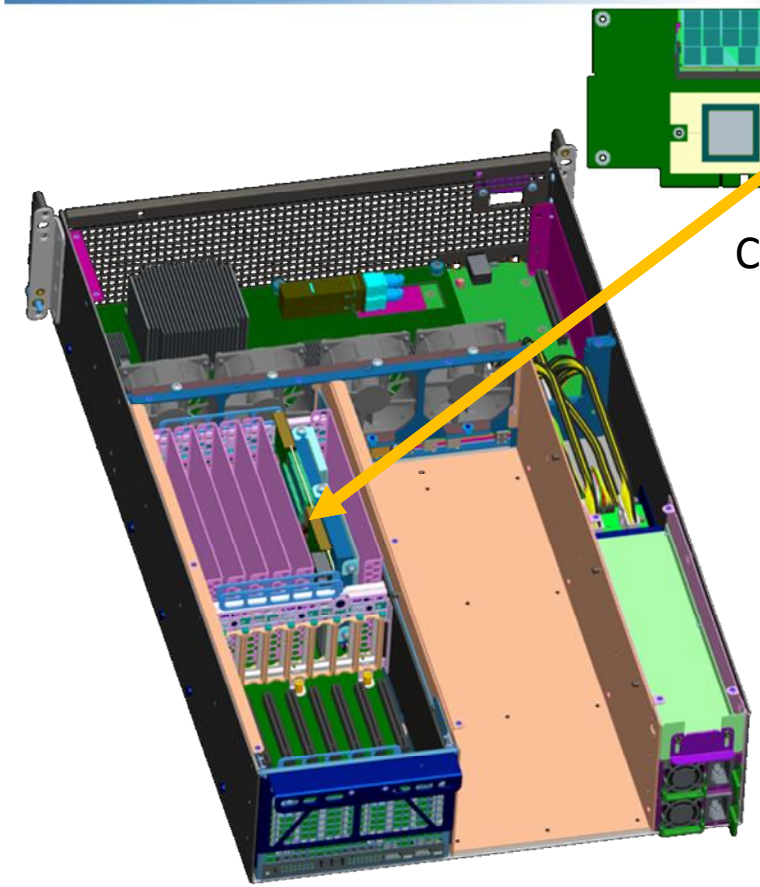


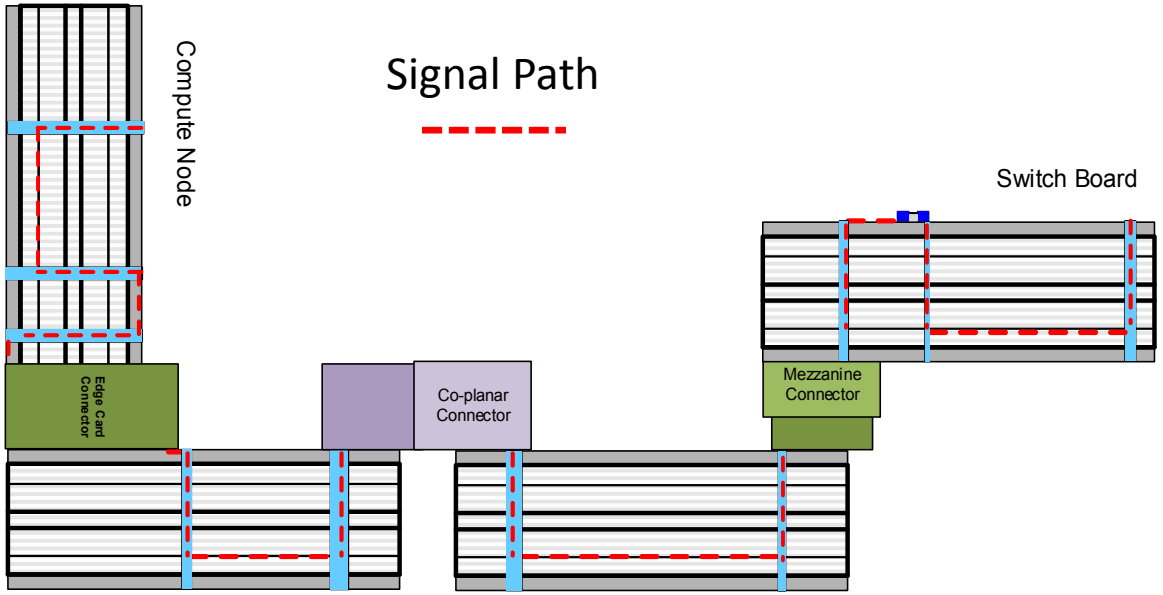
Image Source: https://docs.oracle.com/cd/E19536-01/820-0457-11/intro.html

Non-Traditional Backplane use cases have emerged.



Compute Node

INTEL® Reference Design



Cable Ethernet Syntax Example

- <XX>BASE-**C**R and <XX>BASE-**C**R4
- **C** -> **C**opper Twin-Ax Cable
- <XX> for BASE-CR, example 40G\25G\100G

Choice of MDI Interconnect **not** left up to implementer

- Mix of observable and non-observable test points

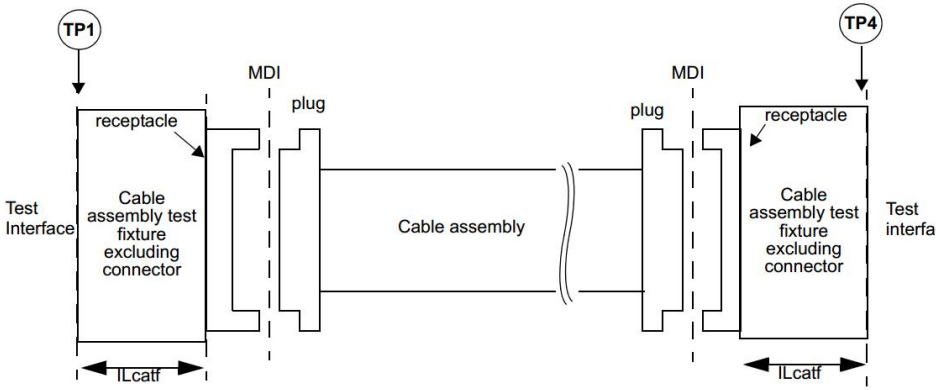


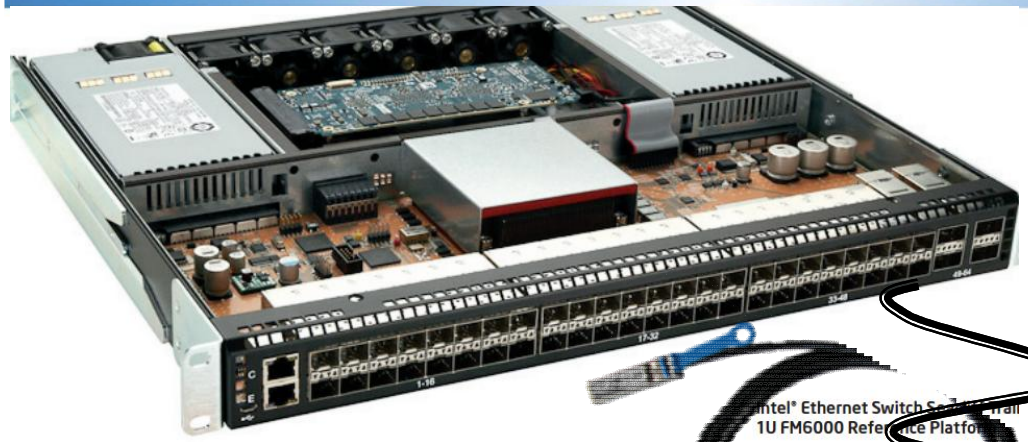
Figure 92–17—Cable assembly test fixtures

IEEE Std 802.3™-2012, SECTION SIX

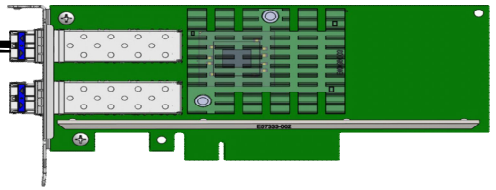
Table 85–4—40GBASE-CR4 and 100GBASE-CR10 test points

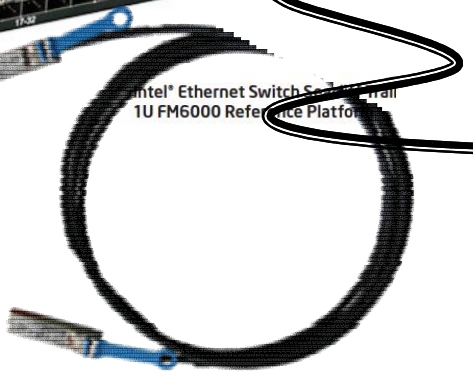
Test points	Description
TP0 to TP5	The 40GBASE-CR4 and 100GBASE-CR10 channels including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 85–2. The cable assembly test fixture of Figure 85–13 or its functional equivalent, is required for measuring the cable assembly specifications in 85.10 at TP1 and TP4.
TP0 to TP1 TP4 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 85.8.3 and 85.8.4. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 85.8.3.4.
TP2	Unless specified otherwise, all transmitter measurements and tests defined in Table 85–5 are made at TP2 utilizing the test fixture specified in 85.8.3.5.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 85.8.4 are made at TP3 utilizing the test fixture specified in 85.8.3.5.

Example Copper Cable (“CR”)

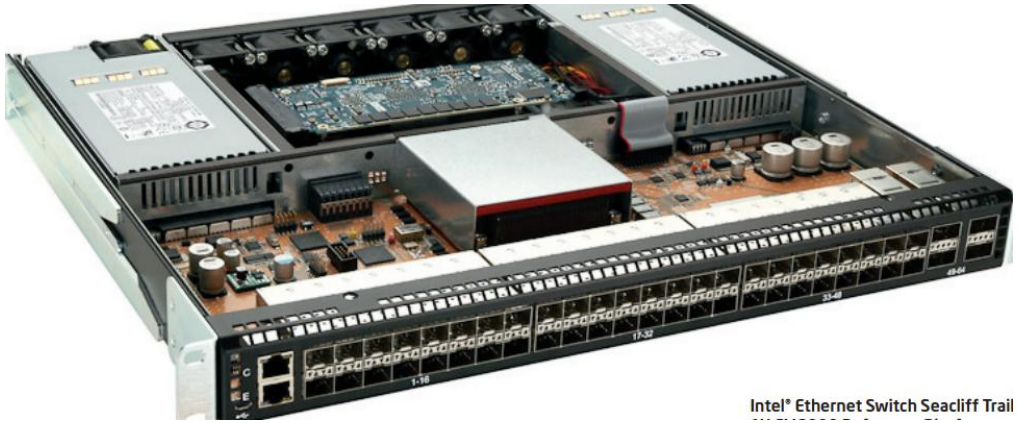


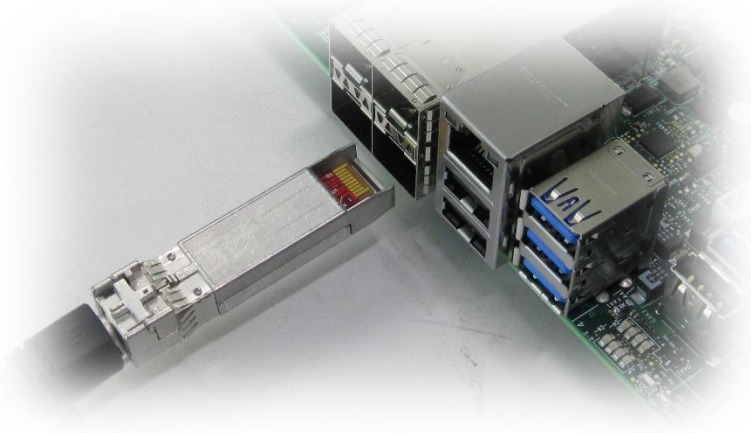
Ethernet NIC





SFP+\QSFP+

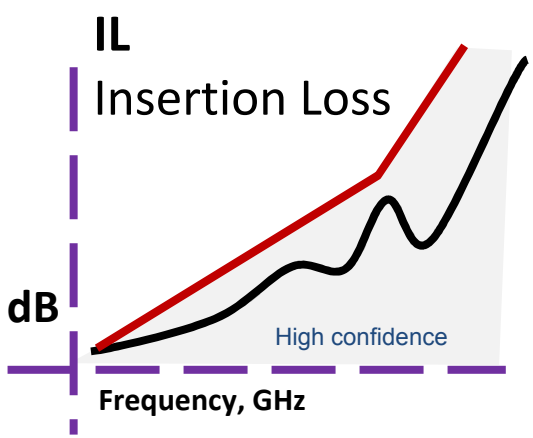


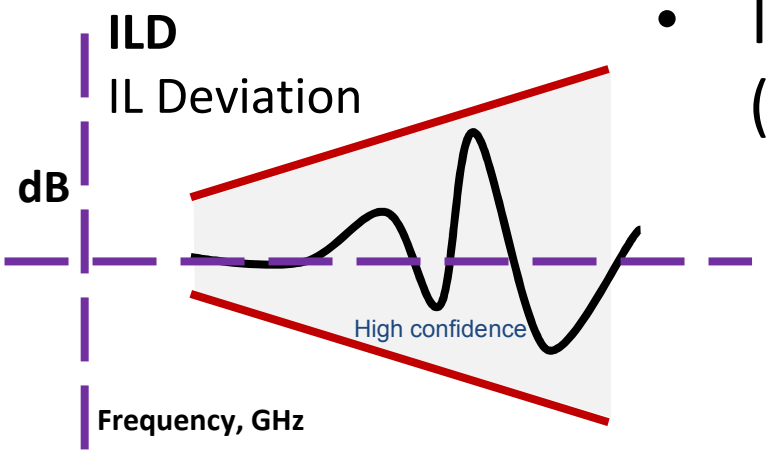


Agenda

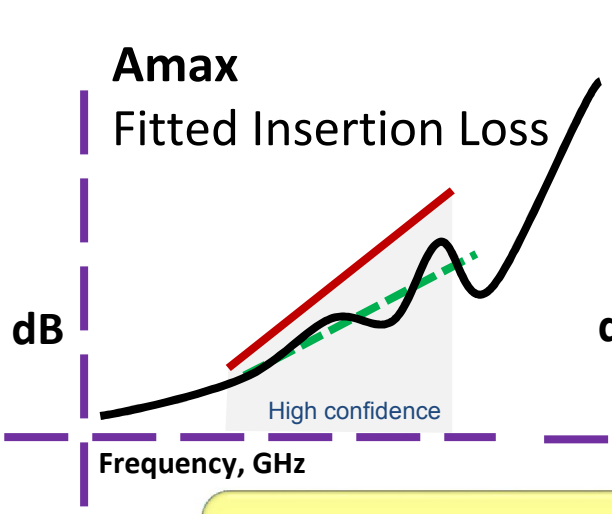
- Backplane and Copper Cable Ethernet Interconnect
- Channel Compliance before IEEE 802.3bj
- What is COM?
- Examples of Signal Integrity Decisions
- “Simple” Interconnect Models have Opportunities for modeling improvements
- Questions?

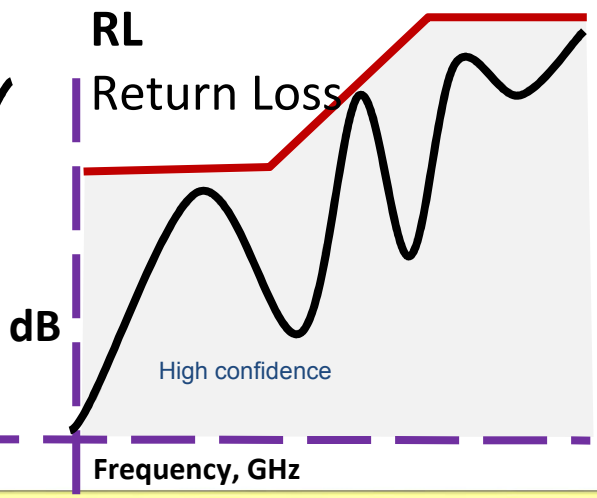
Frequency Domain Masks:
10GBASE-KR and 40GBASE-KR4

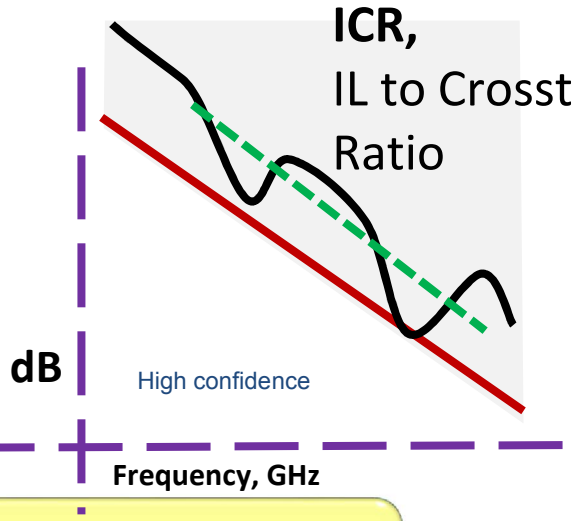




- Informative (no guarantee)

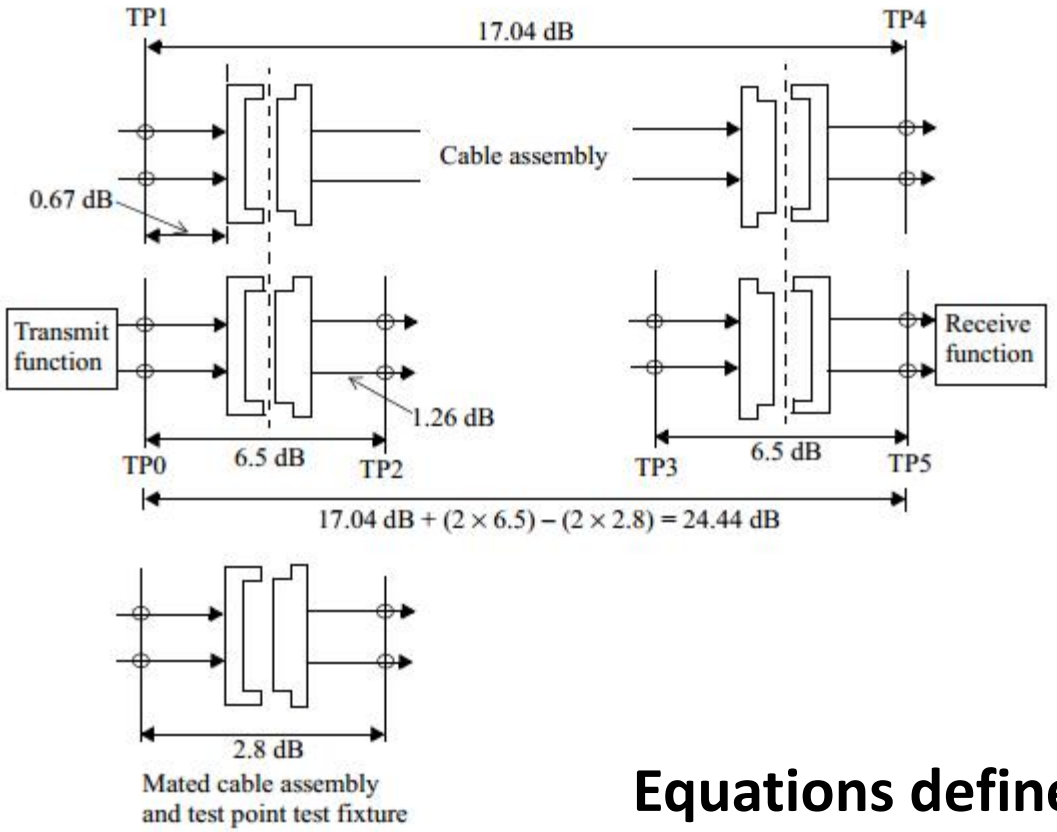






Useful but limited trade-off possibilities

Frequency Domain Masks:
40GBASE-CR4



- TP0-TP5 also informative
- Replaced ICR with Integrated Crosstalk Noise (ICN)
- TP1-TP4 is **normative**

Equations defined in CL-85

IEEE Std 802.3™-2012, SECTION SIX

Budgeting Dilemmas

- Frequency domain channel requirements may lead to insufficient margin for manufacturing
  - Margin to masks?
  - Limited trade-offs of impairments
  - Best return on investments
  - Lower cost paradigms drive need of sufficient channel rather than optimal

IEEE 802.3bj: Channel Operating Margin

- COM is a time domain channel (normative) specification
- Collaboration between silicon and platform engineers involved with Ethernet standards development.

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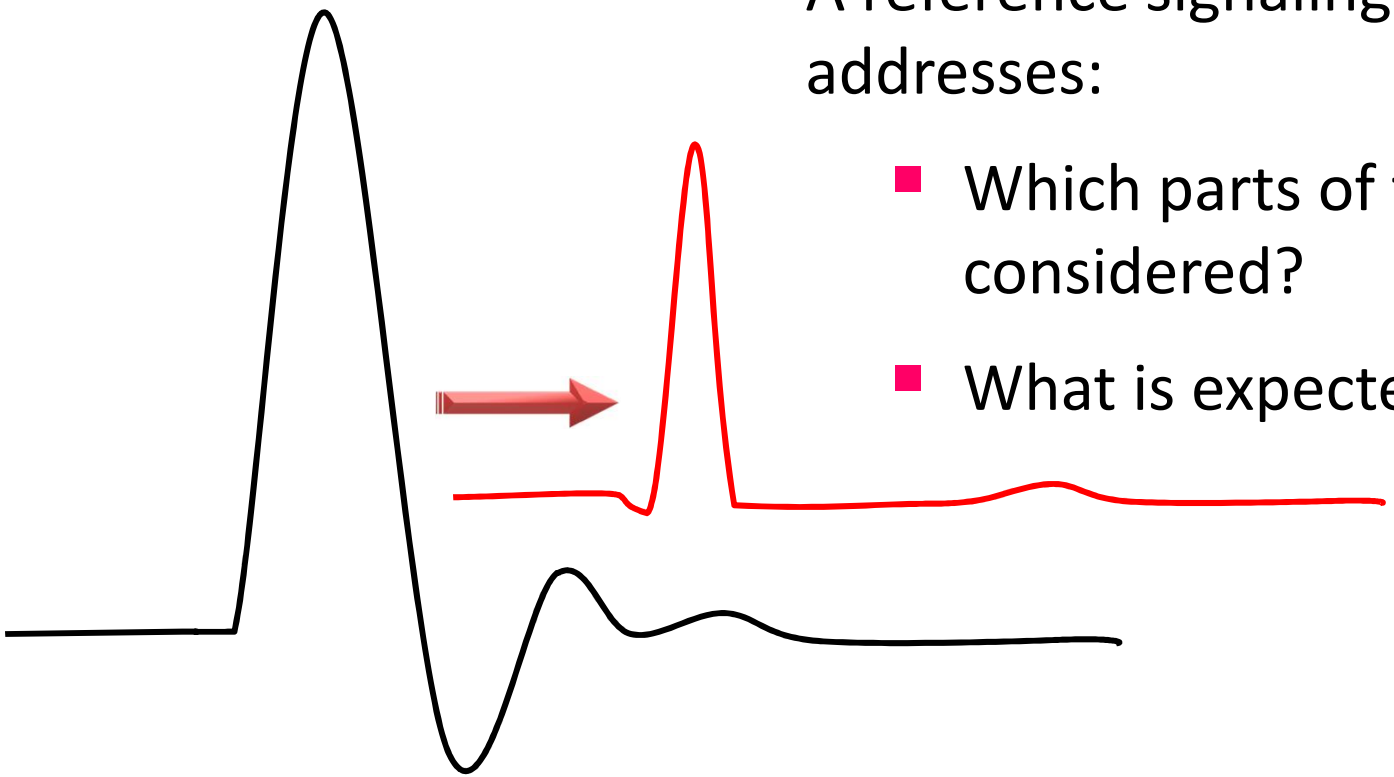
Buffers operate in time
not frequency.

A single bit response (SBR) may be used to determine a realistic figure of merit

Interpretation requires “context”

A reference signaling architecture addresses:

- Which parts of the signal considered?
- What is expected filtering?

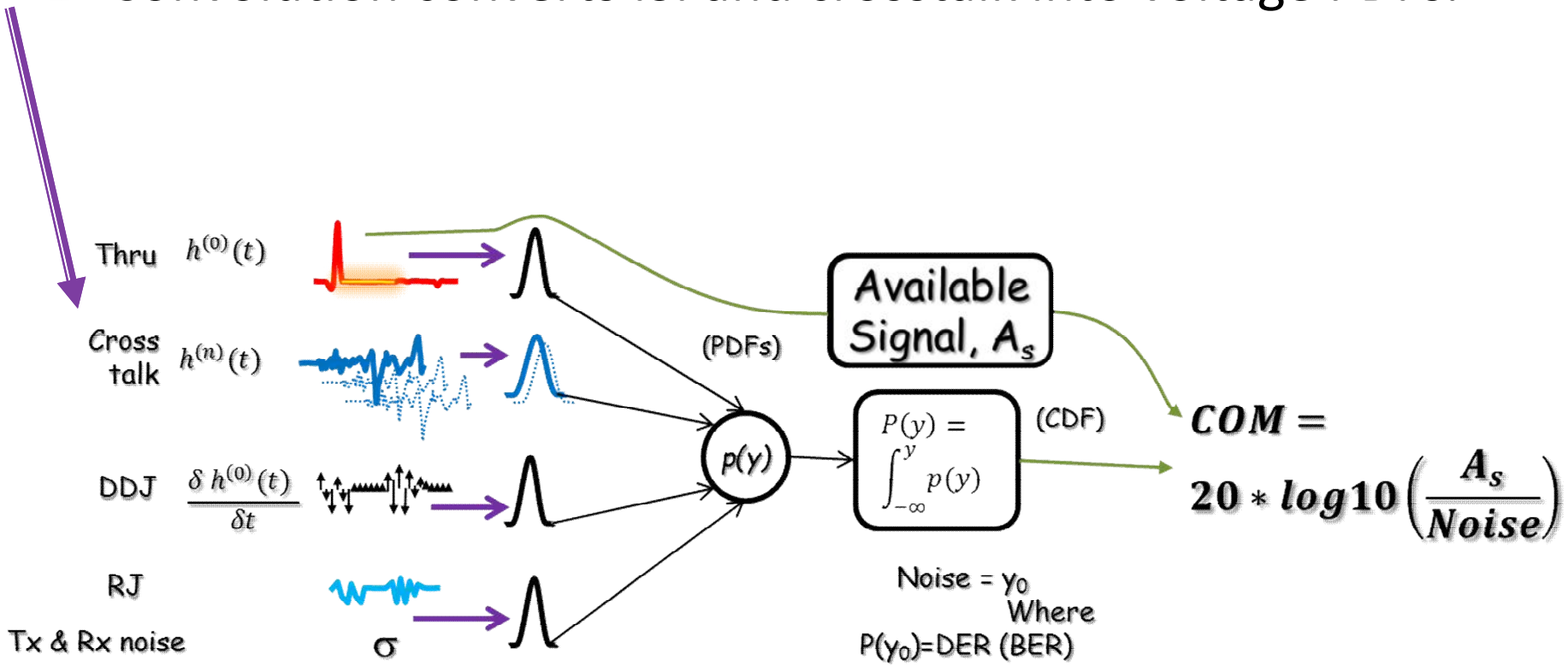


COM (Channel Operating Margin)

- Is computed from the **time domain**
- Is a **single metric** good for a wide range of designs
- Is a **closed budget** for allocation of
  - Compensable and un-compensable ISI
  - Crosstalk
  - Loss
  - Tx and Rx specifications
- Utilizes an agreed upon minimum **reference signaling architecture**
- Produces interim results for separating and budgeting channel impairments

The COM Simplification

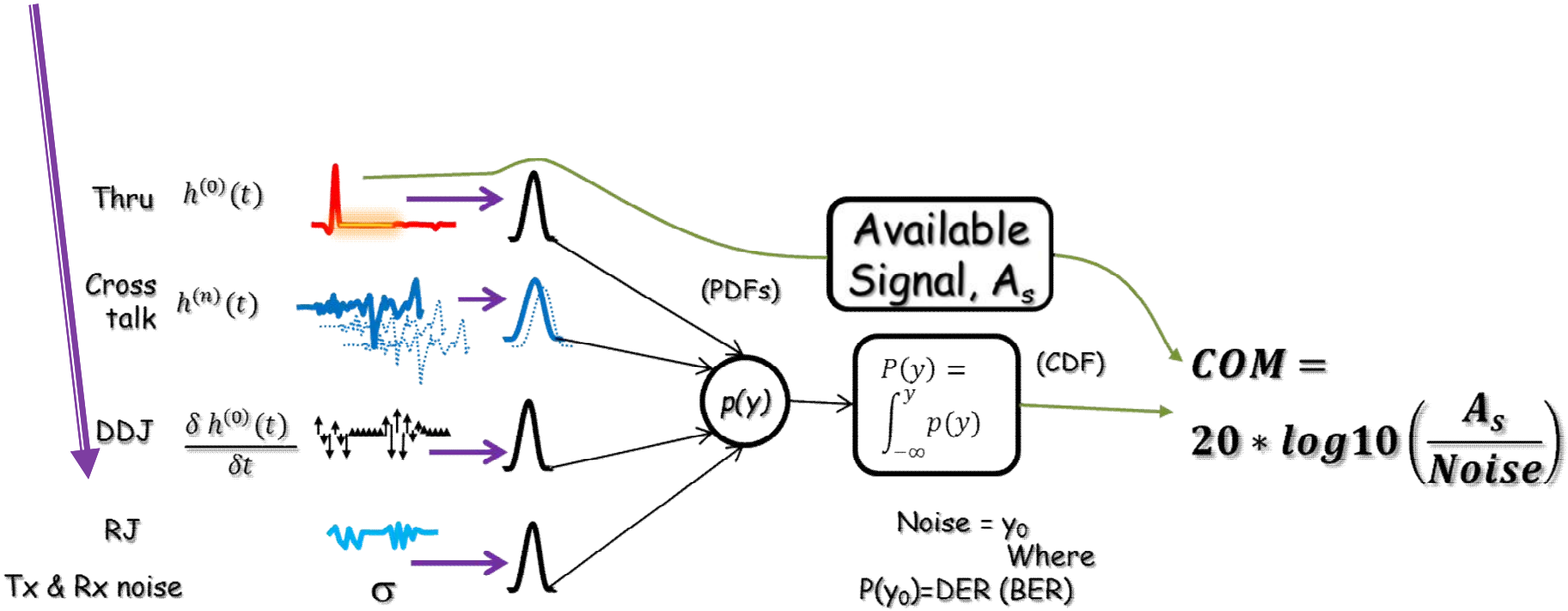
- Starts with converting filtered s-parameters into SBRs $h^{(0)}(t)$, $h^{(n)}(t)$
- Convolution converts ISI and crosstalk into voltage PDFs.



(http://www.ieee802.org/3/bj/public/jul12/mellitz_01_0712.pdf)

The COM Simplification

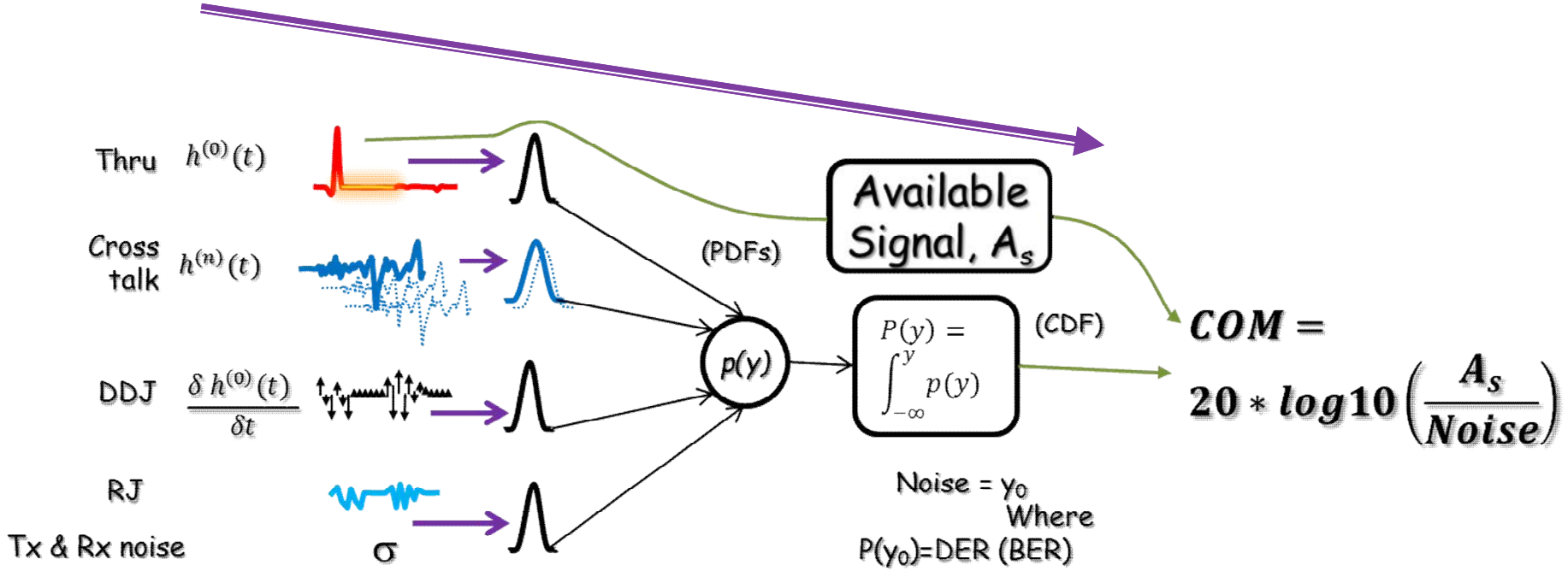
- The derivative of the Thru SBR is used to compute the jitter PDF
- Tx and Rx noise determine another PDF



(http://www.ieee802.org/3/bj/public/jul12/mellitz_01_0712.pdf)

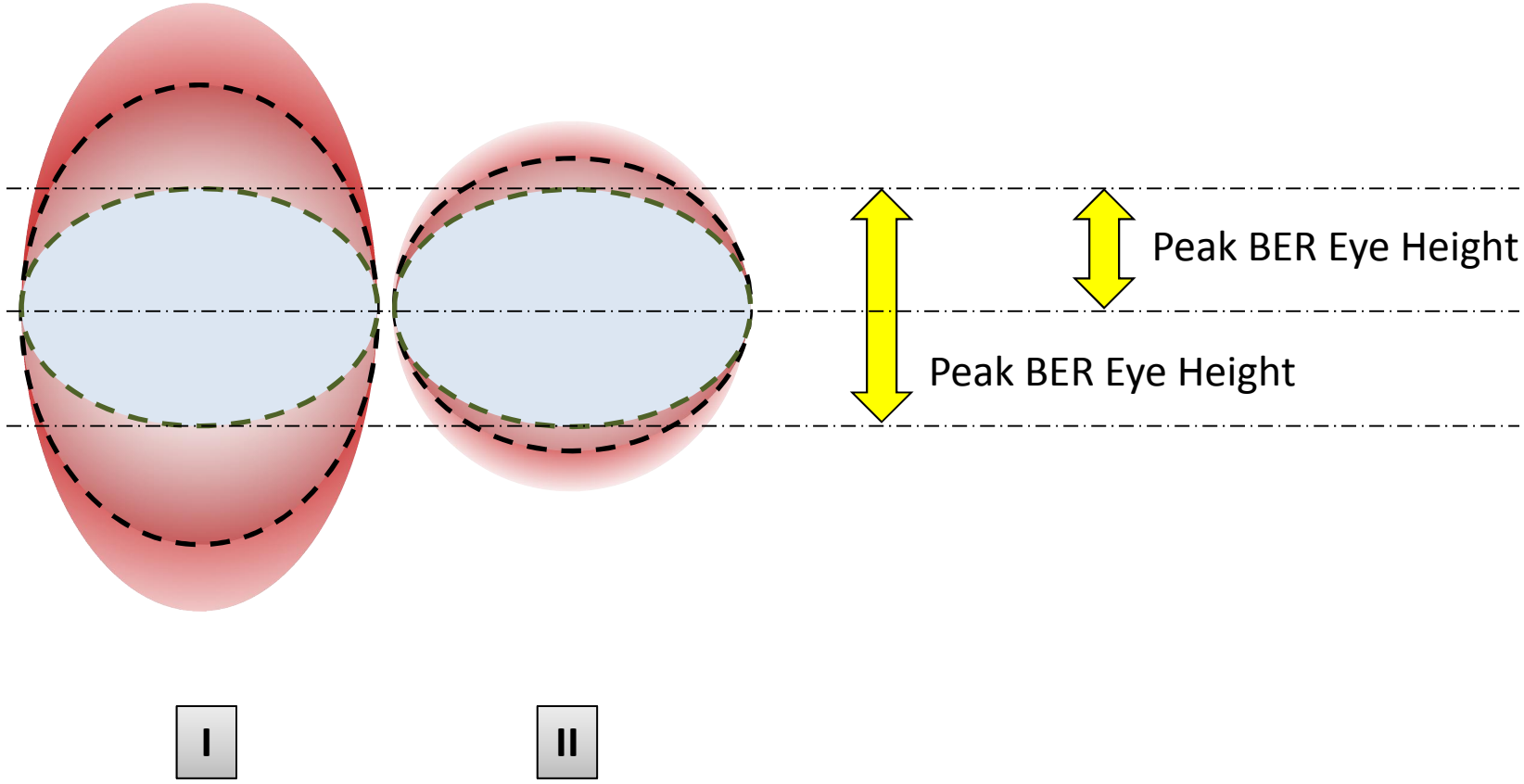
The COM Simplification

- *Noise* at BER is determined from the noise cumulative distribution function (CDF) created from the combined PDF's
- COM is defined as the ratio of available signal to noise

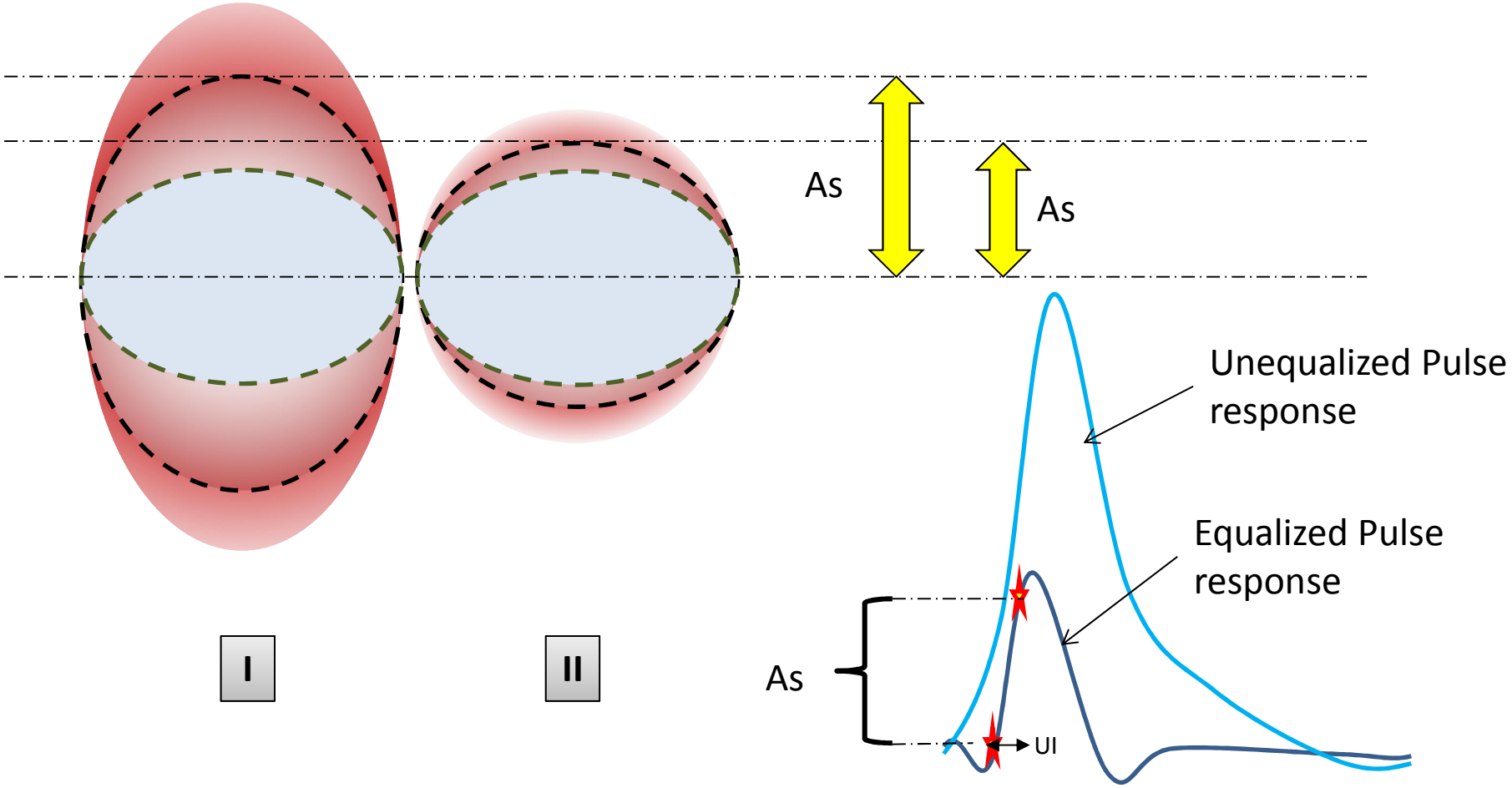


(http://www.ieee802.org/3/bj/public/jul12/mellitz_01_0712.pdf)

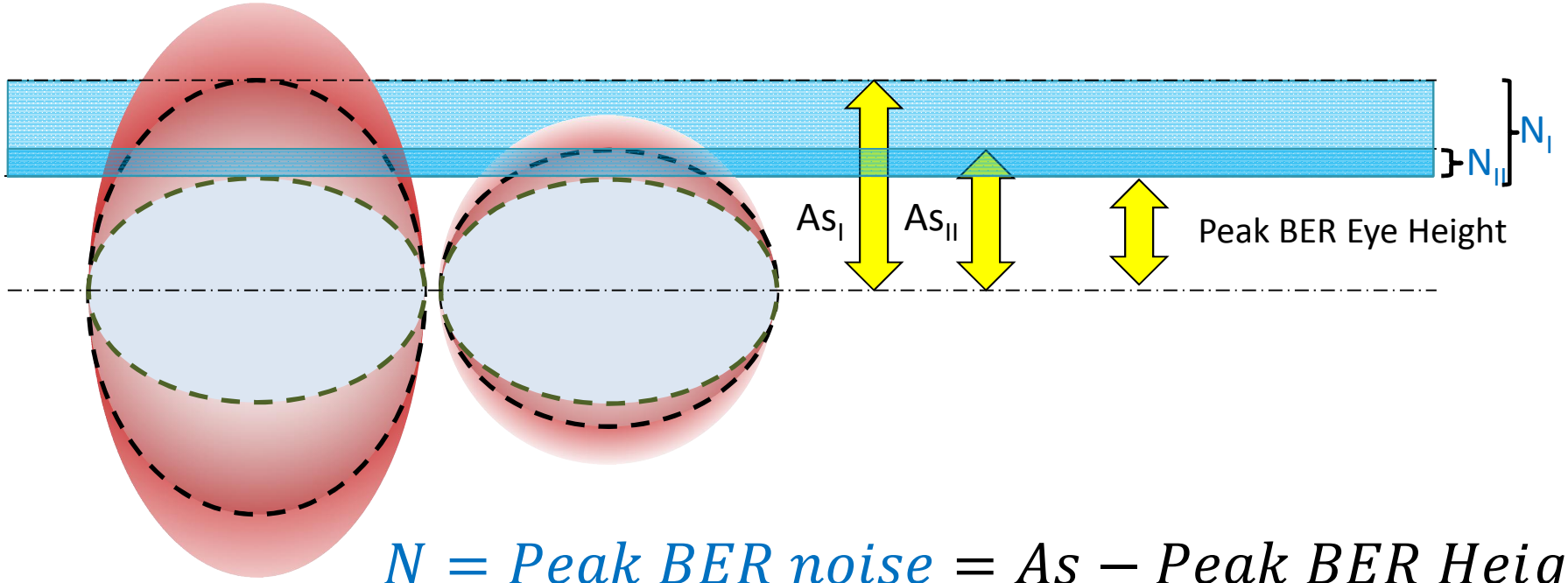
Peak BER Eye Heights
are the same



Average signal height is
greater for channel 1



$$COM = 20 * log10\left(\frac{A_s}{N}\right)$$



$$N = Peak\ BER\ noise = As - Peak\ BER\ Height$$

I II

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Fundamental Dilemmas
Oppose Optimal Signal Integrity Design

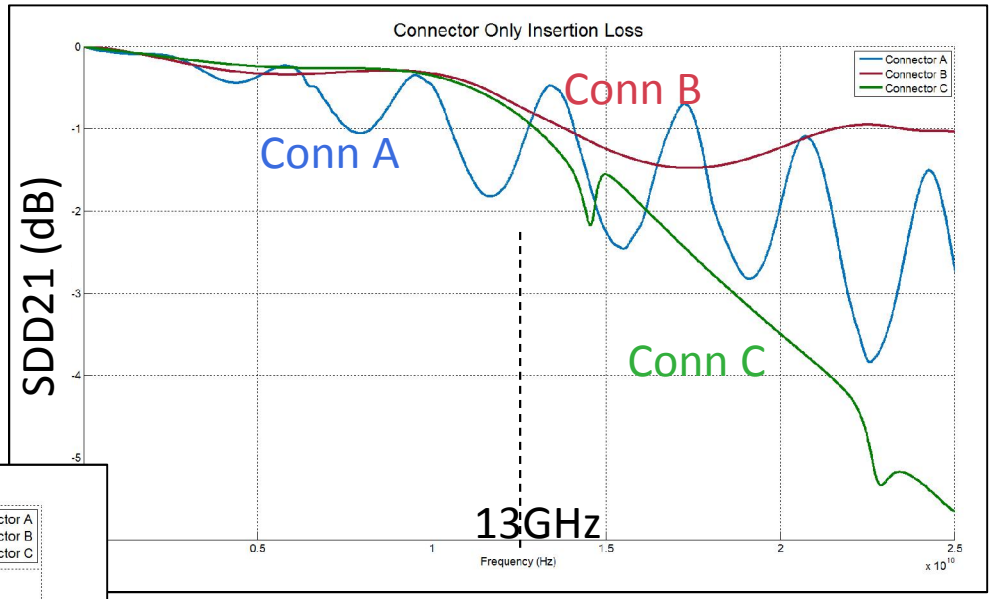
Signal Integrity Wish List	But…
Signal Loss	
Wide Traces \ Thick dielectrics	Cost, Density, and DDR
Smooth Copper	Peel Strength
Best Material	Cost and Manufacturing
Reflection Noise	
Eliminate VIA stubs	Cost
Electrically Small Connectors	Mechanical and form factor
Coupling (Crosstalk) Noise	
< 60dB (0.1%)	Routing Density

Trade-offs are readily made using COM evaluation

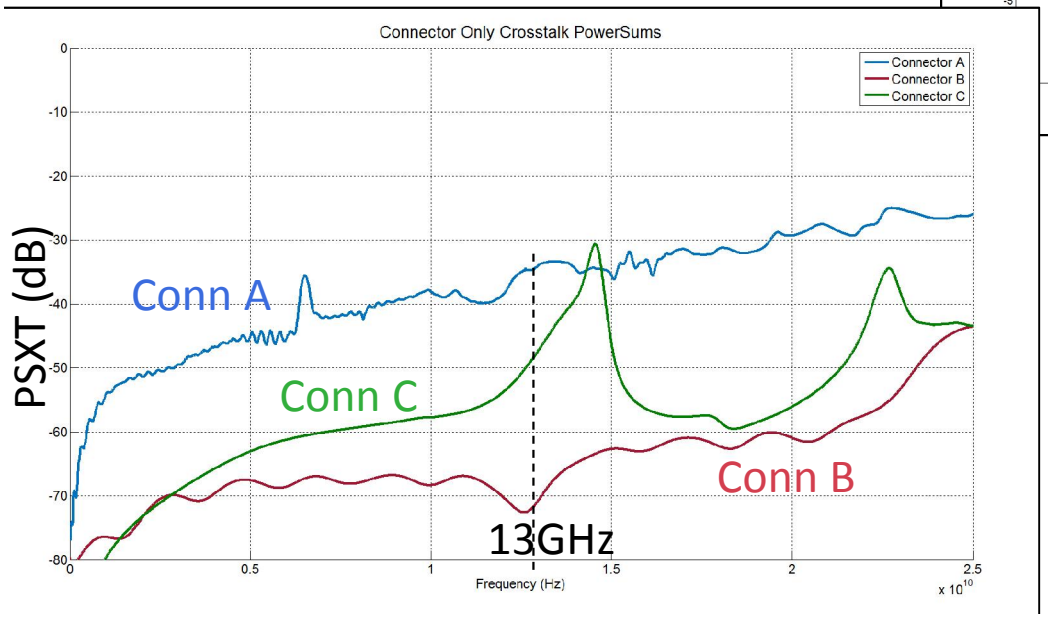
Connector Example:
Component Only Performance

- Connector A
  - Highest PSXT
  - Largest IL and RL

Insertion Loss

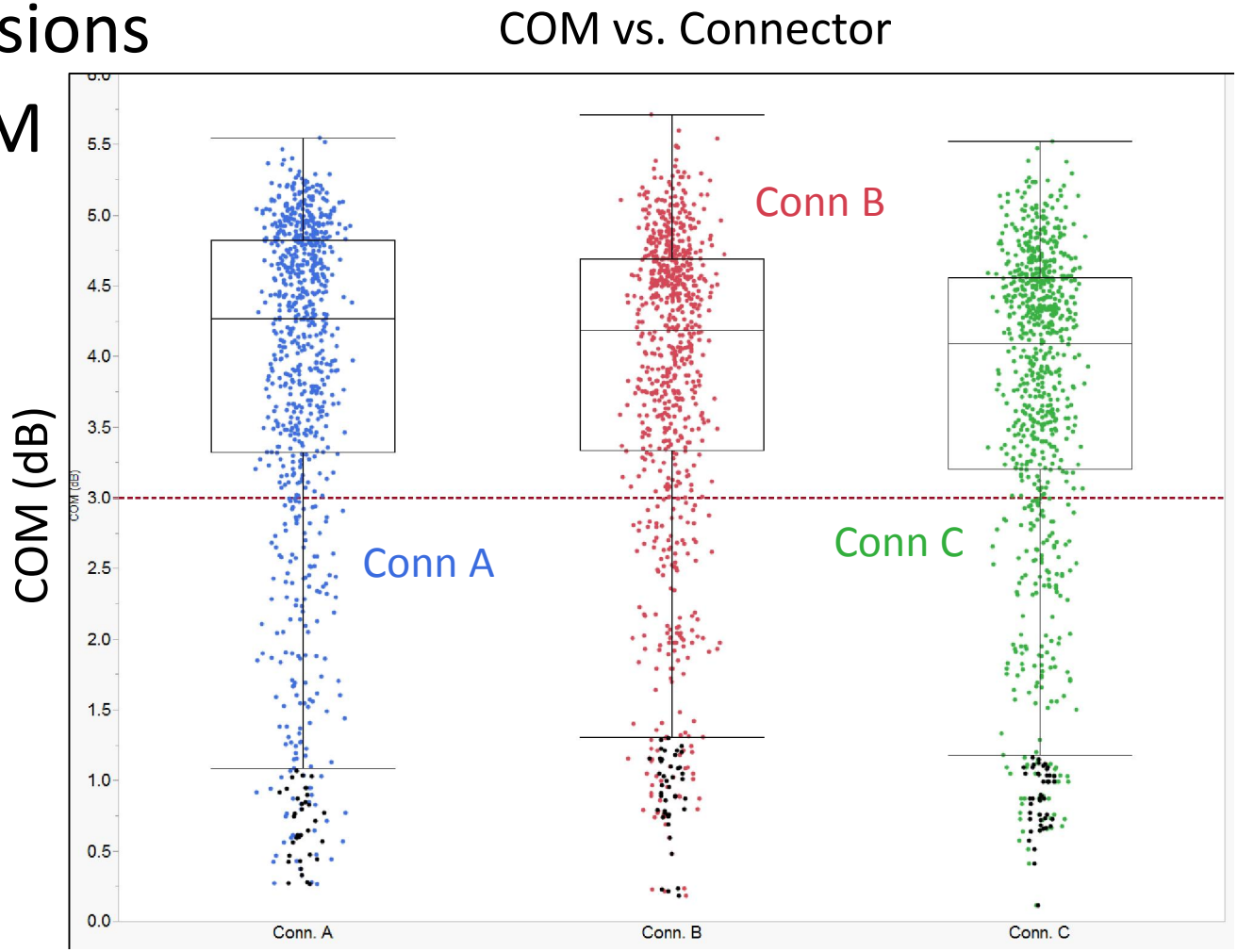


Crosstalk Power Sum



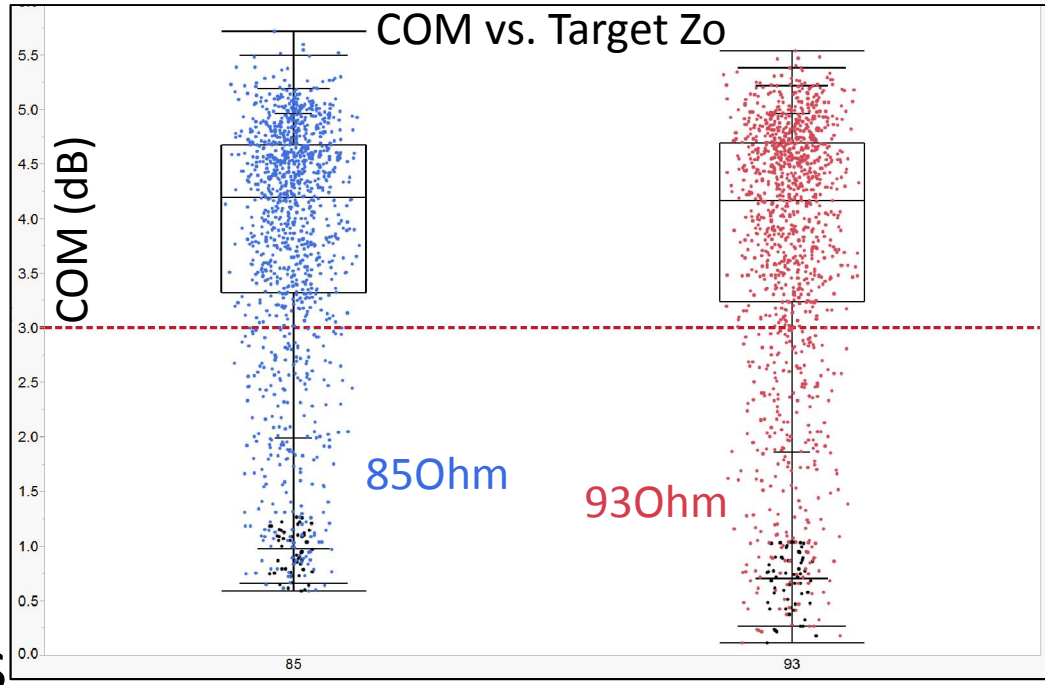
Connector Example:
Similar pin to pin performance

- ~2.5k COM evaluations per connector
- In context decisions possible with COM evaluation



Target Impedance:
Motivation to go lower on PCB

- Wider traces for dense stack ups
  - Easier to manufacture
  - Lower copper loss
  - Tighter differential coupling
- Match low impedance discontinuities
- Preparation for 50Gbps PAM4?
  - http://www.ieee802.org/3/50G/public/adhoc/archive/mellitz_021716_50GE_NGOATH_adhoc.pdf



COM evolution can quickly determine best target impedance.

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Opportunities for modeling improvements

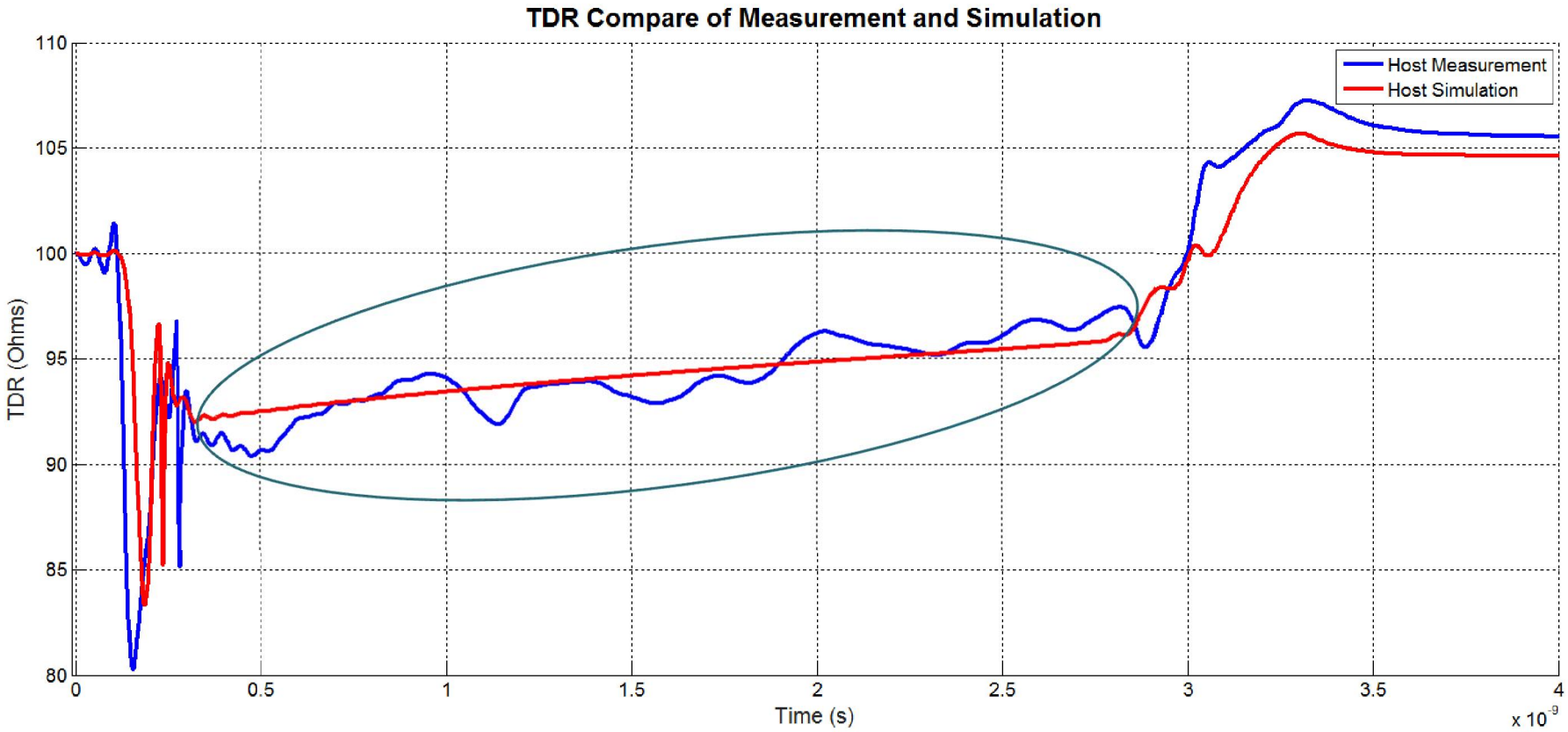
- COM evaluations allow trade-offs in the context of a reference PHY architecture
- How much should be included in interconnect modeling?
- Following poses questions not answers.
- Focusing on “simple” interconnect models
  - Transmission Lines
  - PCB Layer Transition Via

Transmission Line Models

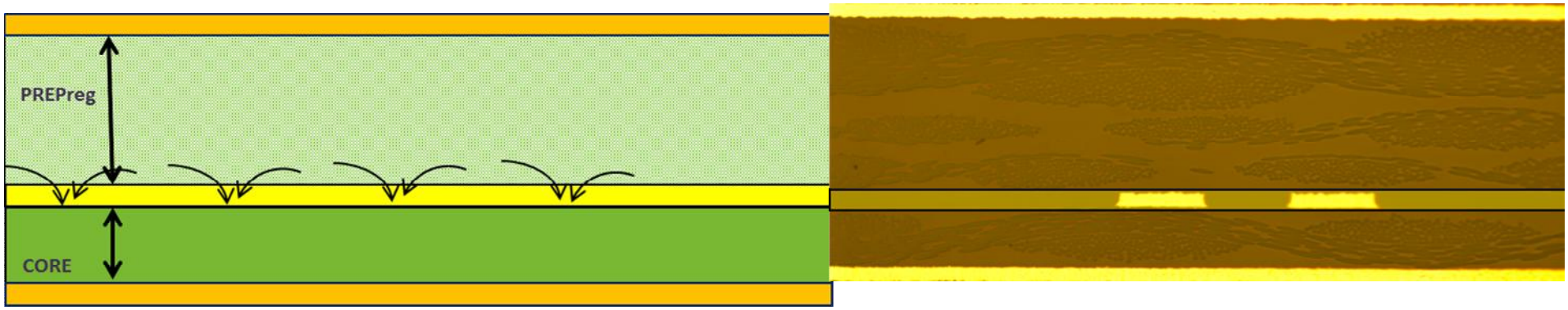
- Typically Transmission Line Models include
  - Physical variations: Etch, core, pre-preg, stackup
  - Dielectric change with frequency
  - Power loss from conductor roughness
  - Variation from temperature changes
- What else might matter?
  - Variation along the etch
  - Effective Dk versus Resin Pocket
  - Infinite speed of light

Channel performance varies along the routing

- +/- 1.5 Ohm peak variation



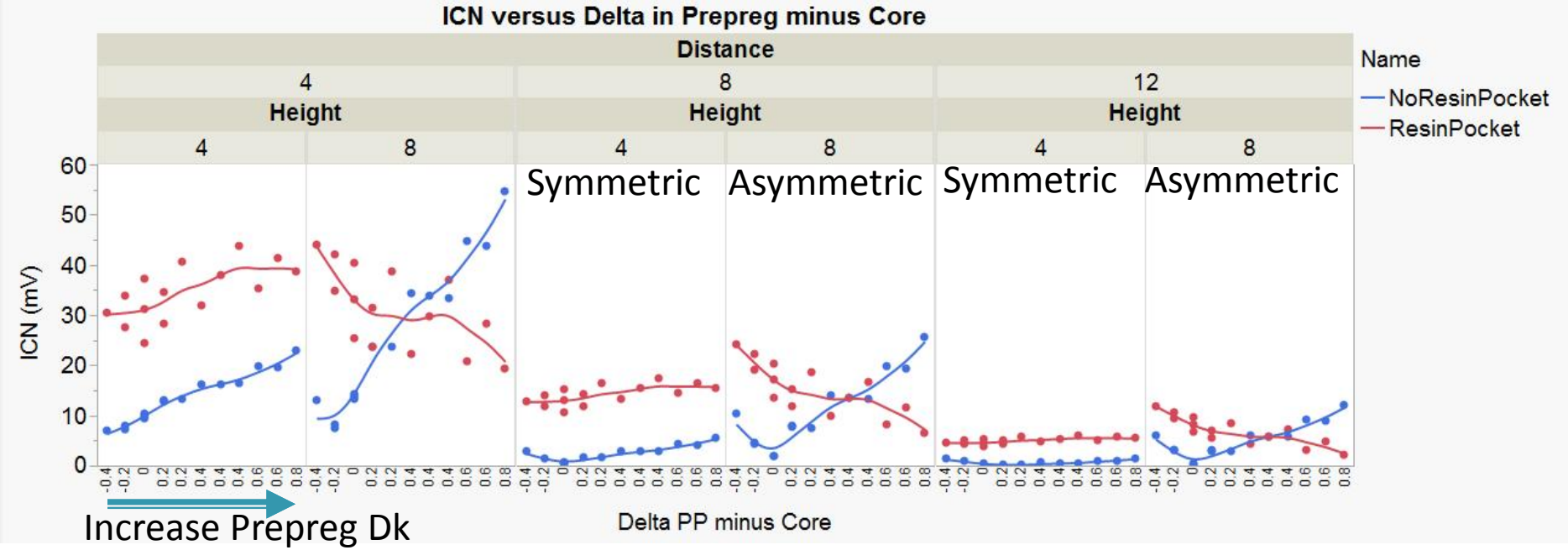
PCB is not homogeneous



- Can approximate a pocket of resin
- This has effect on crosstalk performance in simulation

2D Simulation Example

Resin Pocket reverses trend
of ICN (cross talk)



- Conductor separation reduces ICN magnitude
- Symmetric Core\Pre-preg has similar ICN trend with Dk mismatch
- Asymmetric Core\Pre-preg has opposite trends in ICN

Transmission Line Modeling
Simplifying Assumption of Low Frequency

- Simulators often make simplifying assumptions
- Calculations for solving transmission lines often assume infinite speed of light or Quasi-Static
- For crosstalk, $\frac{\omega R}{v}$ may not be << 1.

20% error at 10GHz

$$\vec{E}(\vec{x},\omega)=\frac{1}{4\pi\varepsilon}\iiint\left[\vec{r}\,\frac{1}{R^2}(1+j\frac{\omega R}{\upsilon})\rho(\vec{x}',\omega)e^{-j\omega R/\upsilon}-j\frac{\omega}{\upsilon^2 R}\vec{J}(\vec{x}',\omega)e^{-j\omega R/\upsilon}\right]d^3x'$$

$$\vec{B}(\vec{x},\omega)=\frac{\mu}{4\pi}\iiint\frac{1}{R^2}(1+j\frac{\omega R}{\upsilon})\left[\vec{J}(\vec{x}',\omega)e^{-j\omega R/\upsilon}\times\vec{r}\,\right]d^3x'$$

If $\frac{\omega R}{v}\ll 1$ (Quasi-Static)

$$\vec{E}(\vec{x},\omega)=\frac{1}{4\pi\varepsilon}\iiint e^{-j\omega R/\upsilon}\left[\vec{r}\,\frac{1}{R^2}\rho(\vec{x}',\omega)-j\frac{\omega}{R\upsilon^2}\vec{J}(\vec{x}',\omega)\right]d^3x'$$

$$\vec{B}(\vec{x},\omega)=\frac{\mu}{4\pi}\iiint\frac{1}{R^2}e^{-j\omega R/\upsilon}\left[\vec{J}(\vec{x}',\omega)\times\vec{r}\,\right]d^3x'$$

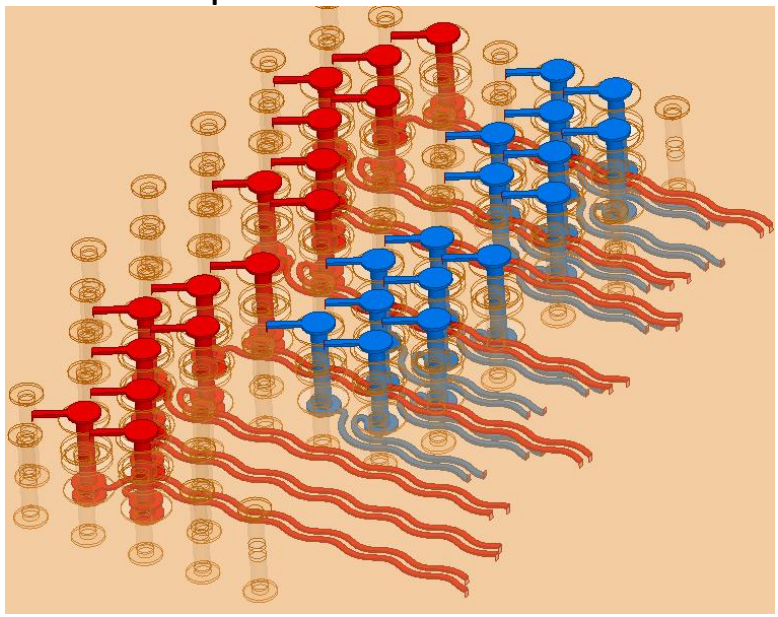
$\omega R/v$ for PCB environment

	f (Hz)	$R=20mils$	$R=5mils$
DC	0	0.000	0.000
100MHz	1.00E+08	0.002	0.001
1GHz	1.00E+09	0.021	0.005
10GHz	1.00E+10	0.213	0.053
20GHz	2.00E+10	0.426	0.106
100GHz	1.00E+11	2.129	0.532

Layer Transition VIAs

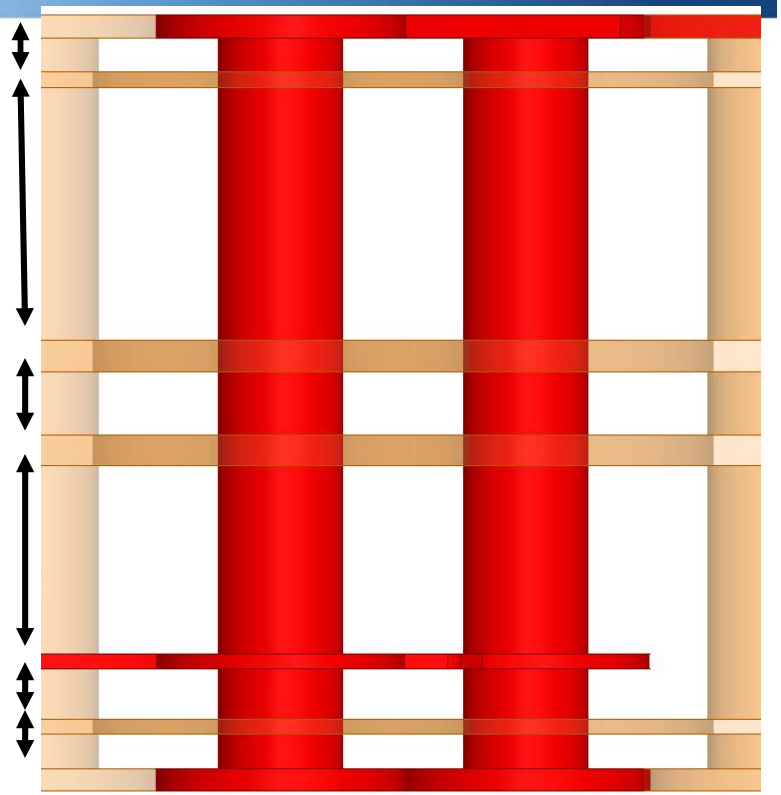
- VIA modeling can be analyzed in 3D EMAG software
- Additional model considerations?
  - Shadow of the device is sometimes overlooked
  - Manufacturing variation for a VIA
  - Layout versus Gerber

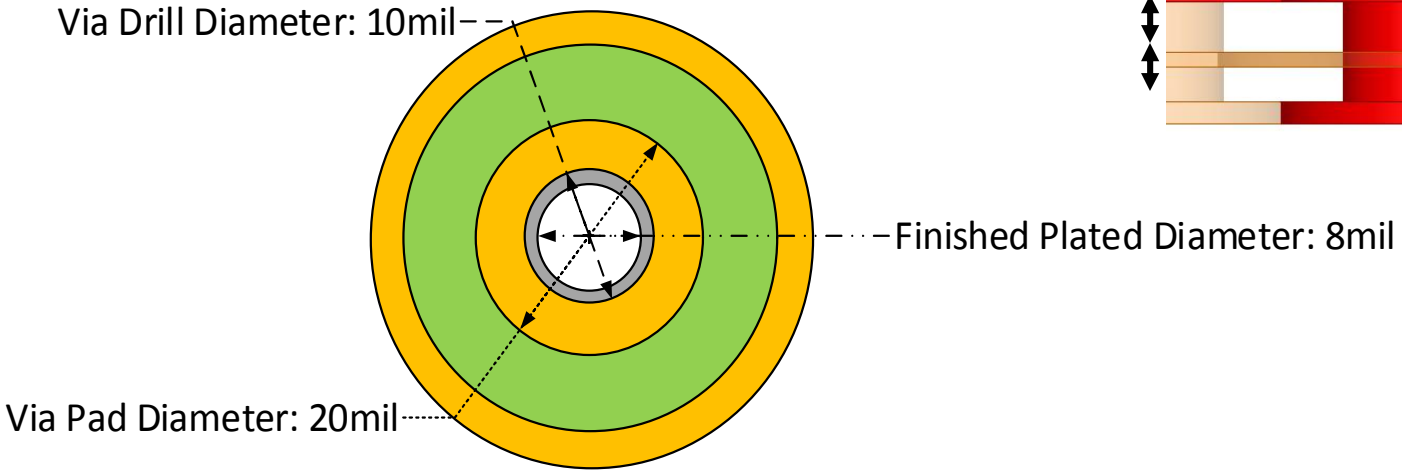
VIAs required in shadow of device



VIA design can be more reflective

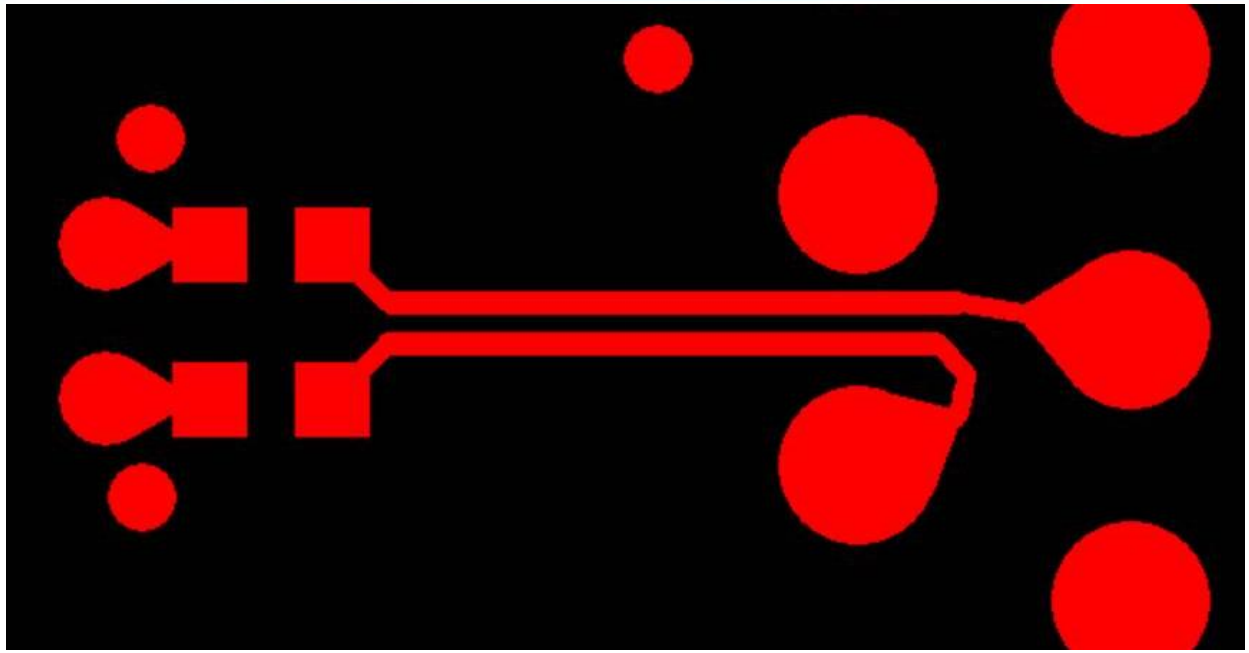
- Each Layer of PCB has tolerance
- Drill\Pad has tolerance
  - Larger drill desired for manufacturing
  - Does metal clearance get adjusted?

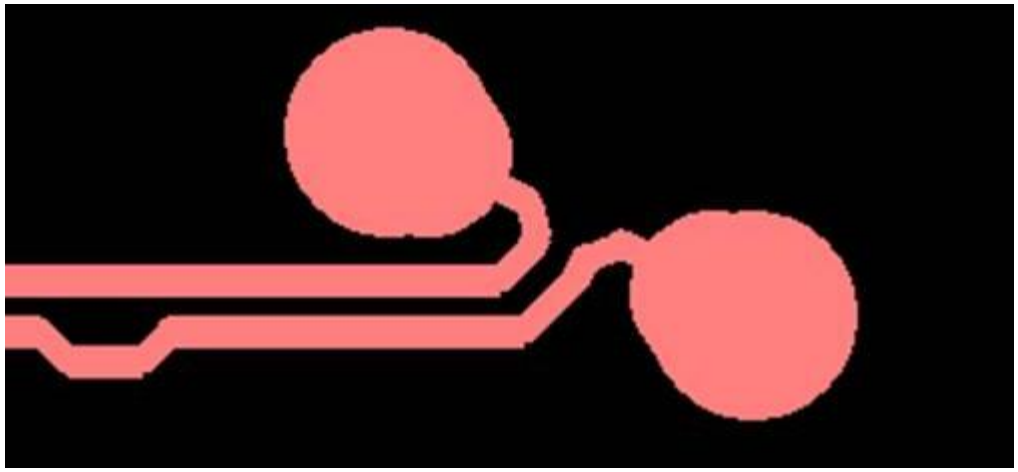




CAD artwork may not match
Gerbers

- Vendors have pad requirements
- Examples
  - Tear Drop Pads
  - Bubble Pads





More reflective vias

Summary

- Frequency domain masks are useful but trade-offs are limited
- COM Evaluation enables quick signal integrity trade-offs in context
- Modeling assumptions should be continually revisited

Questions?

Resources

- IEEE Std 802.3bj-2014, https://standards.ieee.org/findstds/standard/802.3bj-2014.html
- IEEE Std 802.3™-2012, Section Six, https://standards.ieee.org/findstds/standard/802.3-2012.html
- *Mellitz, R. et al, "Time-Domain Channel Specification: Proposal for Backplane Channel Characteristic Sections", IEEE Plenary Meeting July 2012, http://www.ieee802.org/3/bj/public/jul12/mellitz_01_0712.pdf*
- Mellitz, R., "Channel Operating Margin Tutorial", IEEE 802.3cb, IEEE Plenary Meeting, March 2016, http://www.ieee802.org/3/cb/public/mar16/mellitz_3cb_01_0316.pdf
- Mellitz, R., "Backplane Channels: BGA Ball to BGA Ball with Manufacturing Considerations", 50Gb/s Ethernet Study Group, February 17th 2016 Teleconference, http://www.ieee802.org/3/50G/public/adhoc/archive/mellitz_021716_50GE_NGOATH_adhoc.pdf
- Gore B., Mellitz R., "An Exercise in Applying Channel Operating Margin (COM) for 10GBASE-KR Channel Design"
- Gore B., Long G., Loyer J., "PCB Material and Copper Foil Considerations for Insertion Loss" Tutorial, DesignCon 2015
- Peng Ye, "Applying the Retarded Solution of Fields to PCB Transmission Line RLGC Modeling", Ph.D. dissertation, College of Engineering and Computing, University of South Carolina, Columbia, SC, 2015.