Advances in VNA-based Signal Integrity Tools and Techniques

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13th Central PA Signal Integrity Symposium





Outline

- I Technology Driver: Data Rates
- Improving measurement technology for SI applications
 - De-embedding methods
 - De-embedding tools



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Data Rate Trajectory

- LTE success driving wired communicating networks
- Amount of data generated has exploded
- Core network capacity doubles every 18 months
- Server I/O doubles every 24 months
- 100 GE is currently deployed





Double Data Rate with PAM4

PAM4 example

- 4 discrete levels (symbols)
- 2 bits per symbol



Fig.1 A PAM-4 signal in time domain. T= symbol period.



What is an Eye Diagram?

- Overlay of a bit sequence of a digital signal
- Look at 21-bit sequence "010101101001110010111"



PAM4 Measurement



Comparison of PAM4 vs. NRZ

- Advantages:
 - Requires ¹/₂ bandwidth of NRZ
- I Challenges:
 - 1/3 eye height of NRZ
 - ½ to 1/3 eye width of NRZ

 - More sensitive to reflection than NRZ
 More sensitive to crosstalk than characterization in crucial for PAMA signaling
 Much more sensitive for the change of the characterization in crucial for PAMA signaling
 - More sensitive to nonlinearities than NRZ



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Improving measurement technology for SI applications

- SI Measurement Objective is similar to ANY VNA Measurement Objective:
 - Measure ONLY the DUT
 - Remove reflections
 - Remove extraneous loss
 - Remove extraneous phase shift/rotations
 - Focus on Ease of Use...



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Problem Description: Device Performance



Concept of test coupon

- Add test coupon to characterize trace
 - Either on the same board
 - External board but same material
 - External board and different material
- Typical calibration standards
 - TRL calibration standards
 - 2x through
 - 1x through
 - Other reference traces



Reference Plane (TP4)

2x through

Reference Plane (TP1)

strip traces to a DUT

eference Plane Reference Plan (TP3)

(TP2)

Figure GG-GG - Coaxial connectors on a PCB with differentia

Classic approach

- TRL Calibration
 - Requires:
 - Reflect standard
 - Zero-length through standard
 - Line Standard:

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- 20 degrees at lowest freq
- 160 degrees at highest freq

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TRL Standards for Custom Kit (Three Line standards cover 375 MHz to 24 GHz)

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TRL Challenges

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- Multiple lines required to cover higher frequencies
- Still requires Match standard for lower frequencies
- Cal Plane established in center of THRU standard



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CEI56, VSR, MR, LR

Very Short Reach

- 10 cm
- Chip-to-Chip
- One Connector

Medium Reach

- 50 cm
- Chip-to-Chip
- One Connector

Long Reach

- Chip-to-Chip
- Two Connector



Figure 17-1.CEI-56G-MR Reference Model

AC Coupling

Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model

host PCB up to 7.3 dB

Chip

Line Card Host IC

Test Point R

'Component edge

..........

module PCB

+ cap up to

AC

Test Point T

'Component edge'

Chip

Coupling

Cap

1.5 dB

Module IC

....

conn.

up to

1.2 dB

Connector

Common Features:

- Equalization
 CTLE/FFE/DFE
 - CILE/FFE/DF
- Error correction
 - FEC

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Alternative (simpler) solutions

- I Use Offset De-embed
- One Way Loss/Auto Length/Loss
- Use S-parameters from board simulation
- Use advanced fixture de-embedding techniques







- Auto Length
 - Advantages:
 - Simple (requires only an OPEN)
 - Remove reflections
 - Remove extraneous loss
 - Remove extraneous phase shift/rotations
 - Disadvantages:

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Assumes line (to be removed) is Zo

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- Auto Length & Loss
 - Advantages:
 - Simple (requires only an OPEN)
 - Remove reflections
 - Remove extraneous loss
 - Remove extraneous phase shift/rotations
 - Disadvantages:

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- Assumes line (to be removed) is Zo

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- ∎ Fixture Compensation
 - Advantages:
 - Simple (requires only an OPEN)
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 - Disadvantages:

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Assumes line (to be removed) is Zo

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 Can provide "overly optimistic" results

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- ∎ Fixture De-Embedding
 - Advantages:
 - Remove reflections
 - Remove extraneous loss
 - Remove extraneous phase shift/rotations
 - Disadvantages:
 - Requires 2-port s-parameters
 - (measured or modelled)

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2-X Thru Tools:

- Keysight: AFR (Automatic Fixture Removal)
- Packet Micro: SFD (Smart Fixture De-Embedding)
- Ataitec: ISD (In-Situ De-embedding)
 - Disadvantages:
 - May produce non-casual response





2x thru fixture

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What is causality?

cau·sal·i·ty

In other words:

noun

- 1. the relationship between cause and effect.
- the principle that everything has a cause. 2.

How to identify non-causal S parameter

Convert S parameter into TDR/TDT.





Check phase angle.







ISD and SFD Dialog in ZNB, ZNBT Vector Network Analyzers



ISD provided by Ataitec, SFD provided by PacketMicro

