Penn State
Signal Integrity Symposium

Overcoming the SI Challenges in Designing 25 – 40 Gb/s Backplane Channels

Stephen B. Smith
Madhumitha Rengarajan
FCI USA LLC

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Outline of Presentation

- Objective of paper
- The connector
- Discussion of resonance
- Daughter cards
- The first backplane
- The second backplane
- Conclusions / Summary

The Objective

- Design and build a passive backplane system that successfully operates at a data rate of 25 Gb/s
  - Doing it on the first try would be nice
  - What defines success?
    - Meeting the Optical Internetworking Forum's CEI-25G-LR Specification
    - Meeting the IEEE 802.3bj Committee's criterion
    - Demonstrating success with actual SerDes chips
- Figure out how to extend this wisdom to data rates higher than 25 Gb/s

The Connector (Required Features)

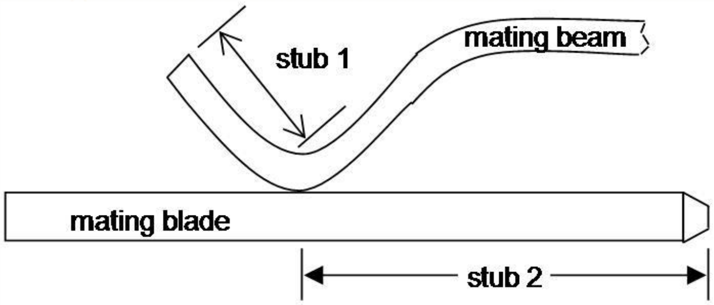
The ExaMAX® Connector

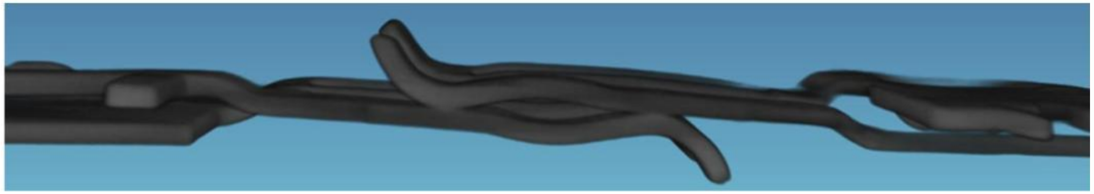
- Excellent Z_0, R.L., I.L., PSXT, and mode conversion
- Zero in-pair skew
- Absence of resonance

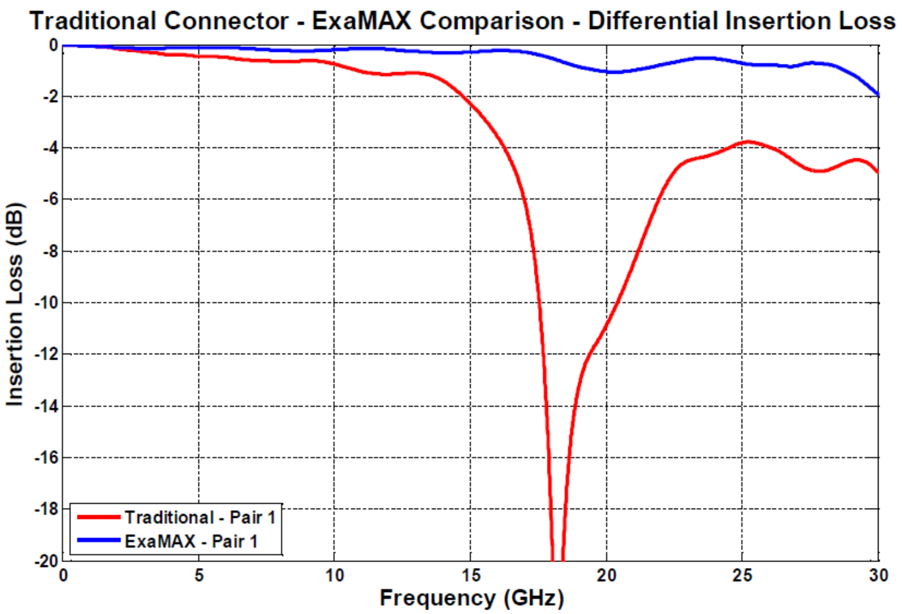
Types of Resonance

- Stub resonance
  - Typically avoided in pc boards by backdrilling
  - Can occur in connector separable mating interfaces
- Ground-mode resonance
  - Occurs when there are multiple grounds / return paths
- "Mixed" (Combination of the two)
  - Happens when there is a stub present on a ground/return path
  - Might behave like a stub and/or a ground-mode resonance

Stub Resonance





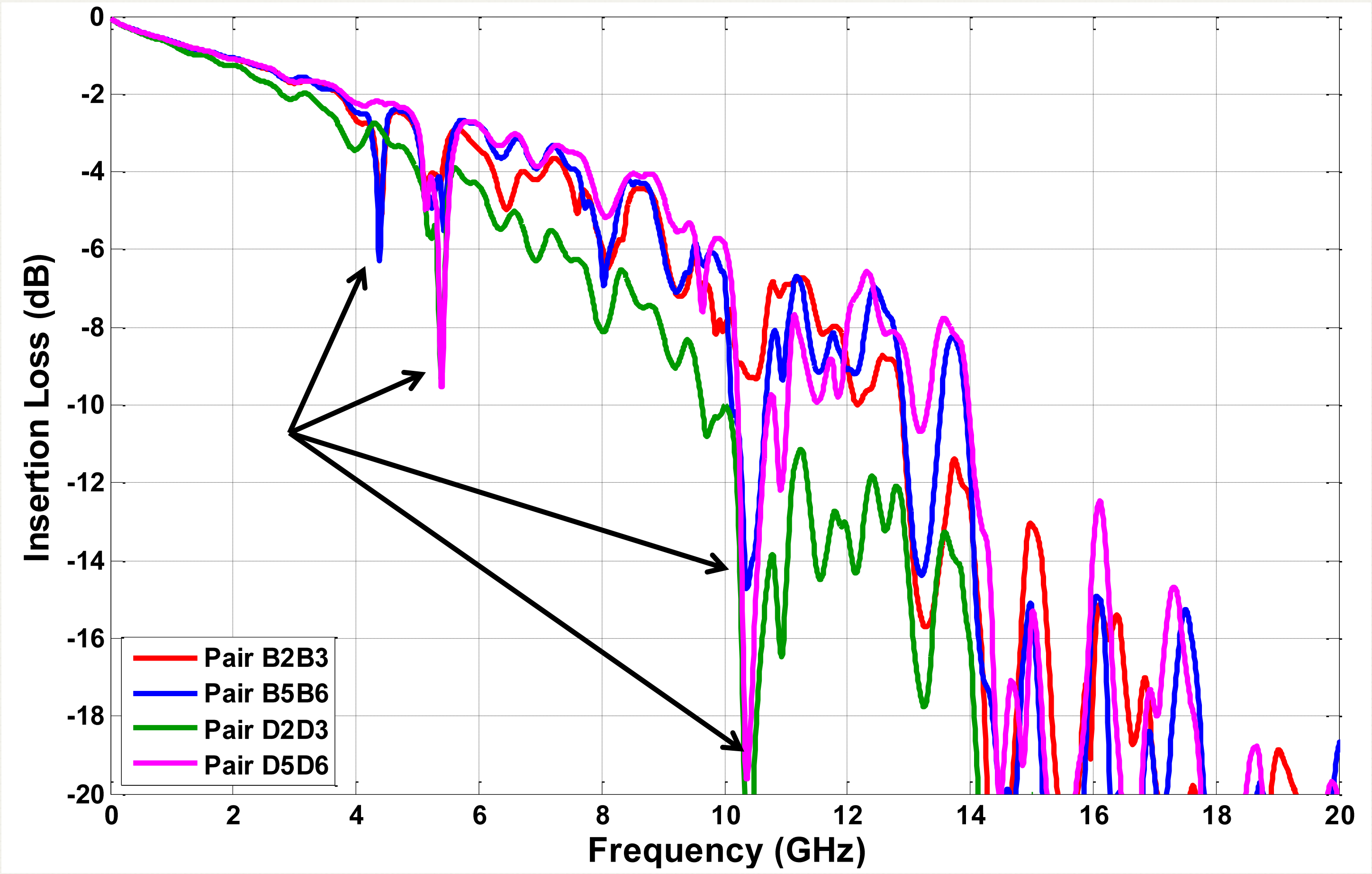


Traditional connector interface (shown above left) has two stub which resonate as shown in red.

Interface making two points of contact (shown above right) does not resonate below 30 GHz.

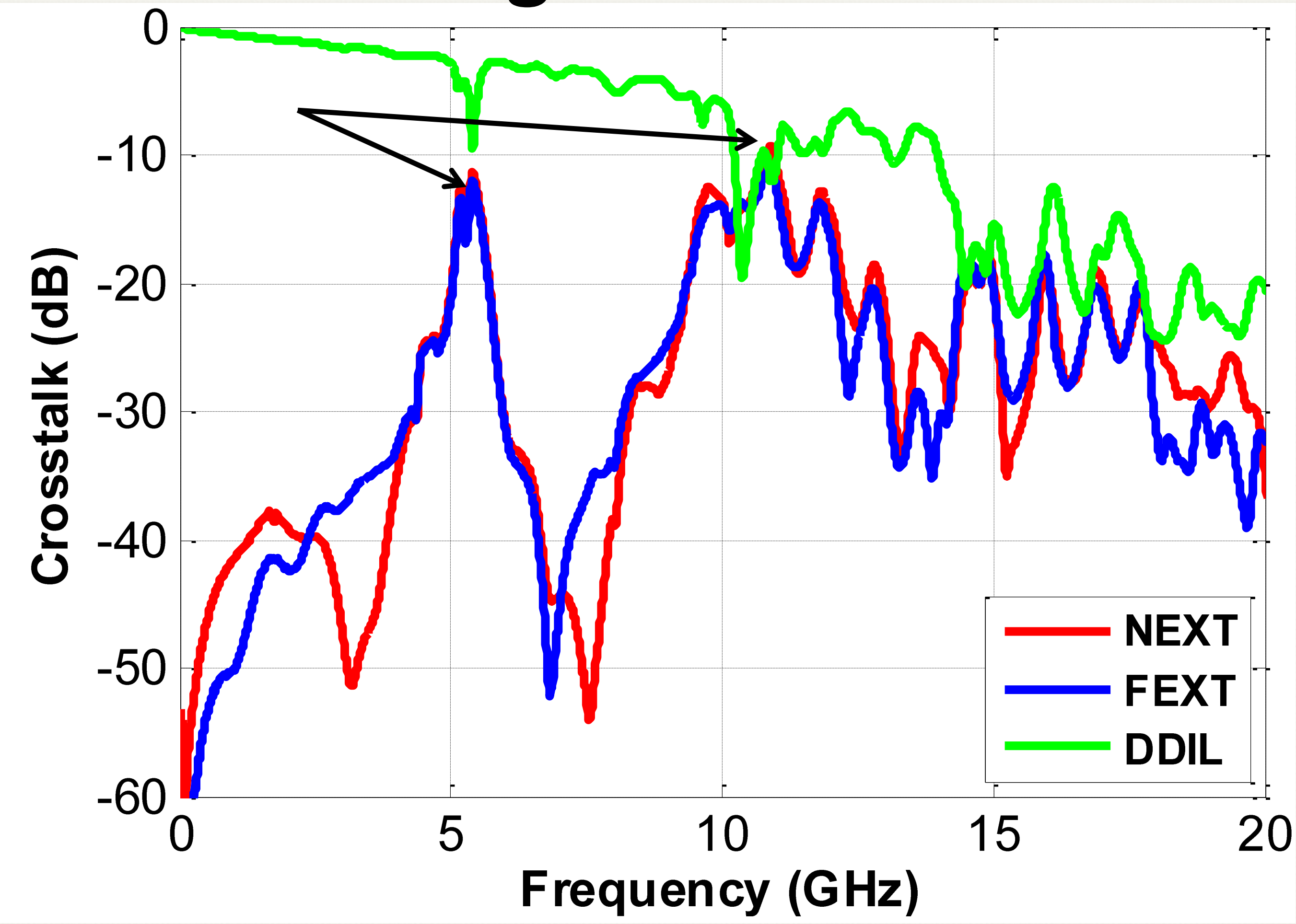
Effects of Ground-Mode Resonance

Ugly Insertion Loss



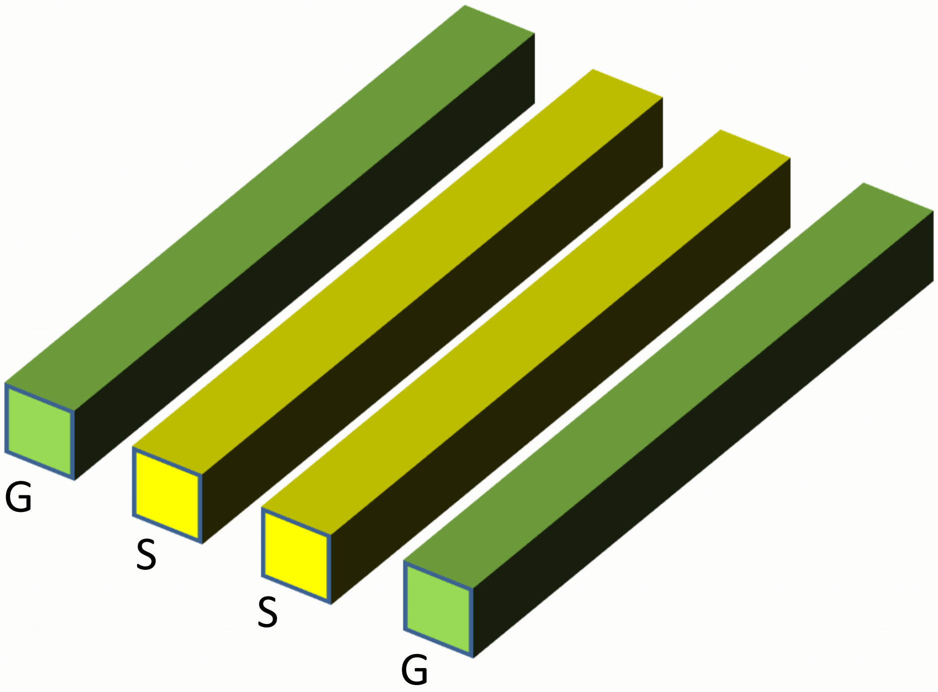
Effects of Ground-Mode Resonance

Even Uglier Crosstalk



Primer on Ground-Mode Resonance

- Modal Analysis:



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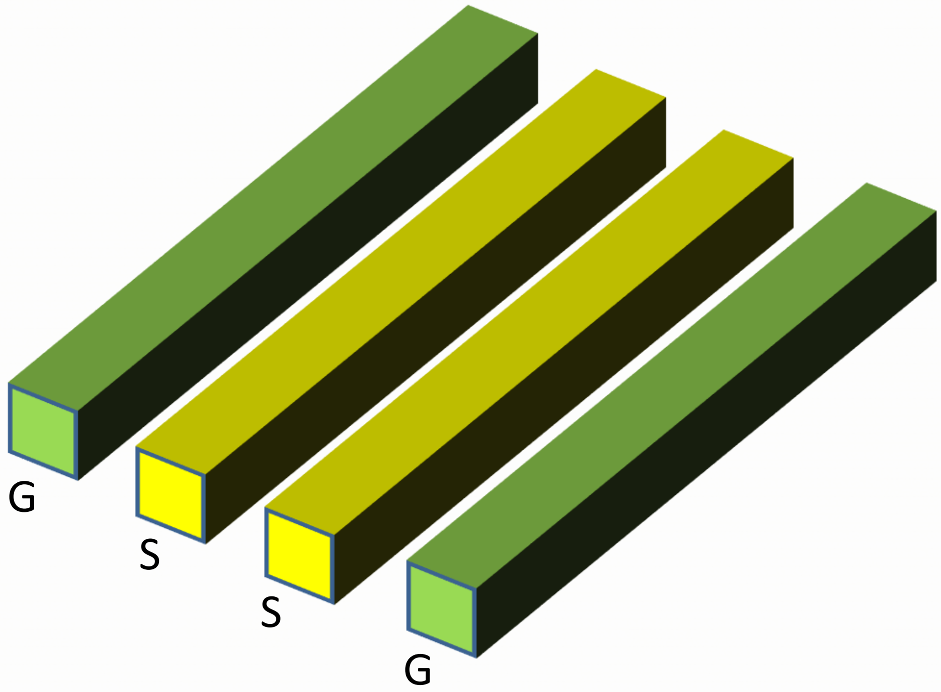

“Time-Domain Response of Multiconductor Transmission Lines”
Antonije R. Djordjevic, Tapan K. Sarkar, Senior Member, IEEE, and Roger F. Harrington, Fellow, IEEE
PROCEEDINGS OF THE IEEE, VOL. 75, NO. 6, JUNE 1987

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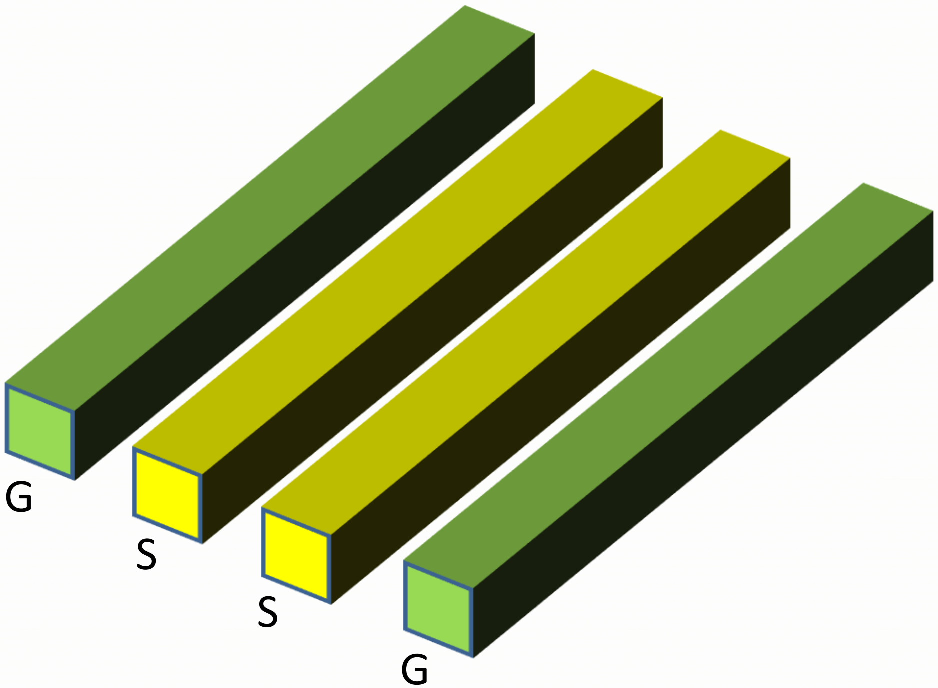

$$\frac{\partial[v(x,t)]}{\partial x} = -[R][i(x,t)] - [L]\frac{\partial[i(x,t)]}{\partial t}$$

$$\frac{\partial[i(x,t)]}{\partial x} = -[G][v(x,t)] - [B]\frac{\partial[v(x,t)]}{\partial t}$$

$$\frac{d[V(x)]}{dx} = -[R][I(x)] - j\omega[L][I(x)],$$

$$0 < x < D$$

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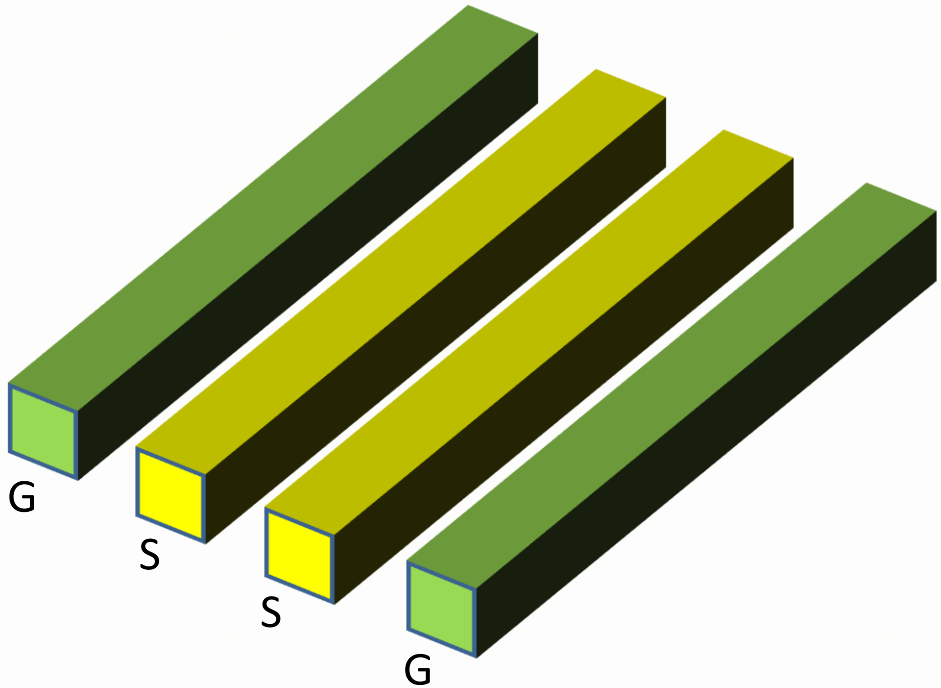

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$[Z] = [R] + j\omega[L]$
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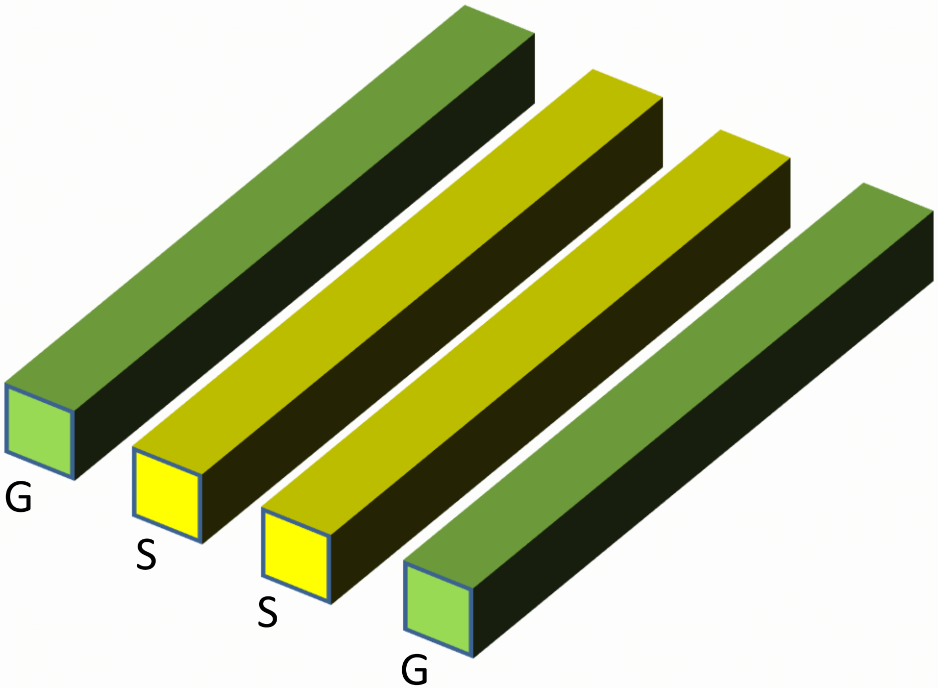

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[Z] = [R] + jω[L]
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det $\{\gamma_m^2\ [U] - [Z]\ [Y]\} = \mathbf{0}$
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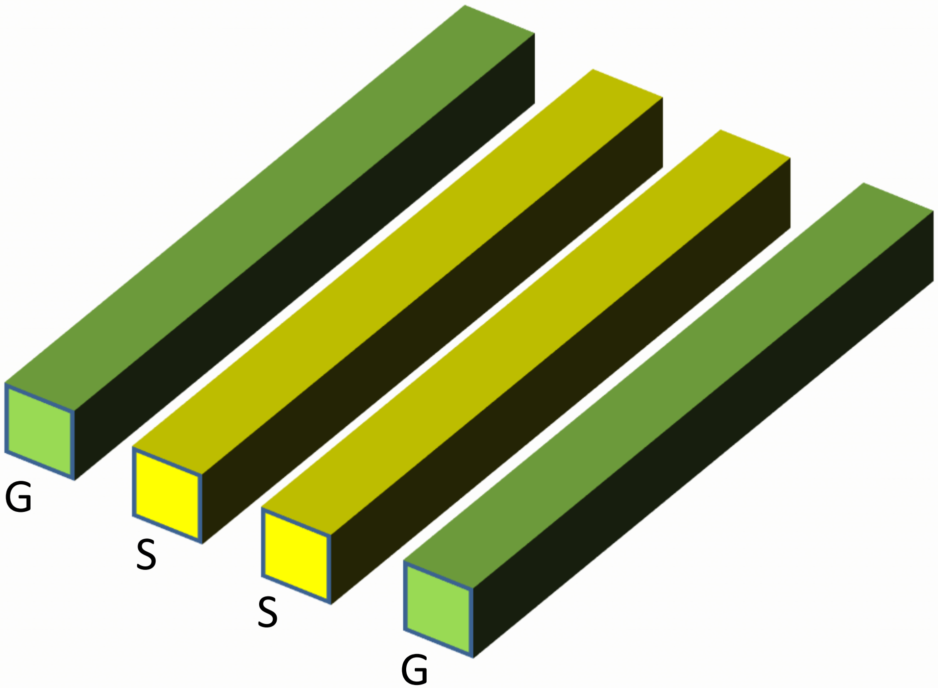

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$\det\{\gamma_m^2 [U] - [Z][Y]\} = \mathbf{0}$

$\det\{\gamma_m^2 [U] - [Y][Z]\} = \mathbf{0}$

$[S_I] = [Z]^{-1} [S_V] [\Gamma]$

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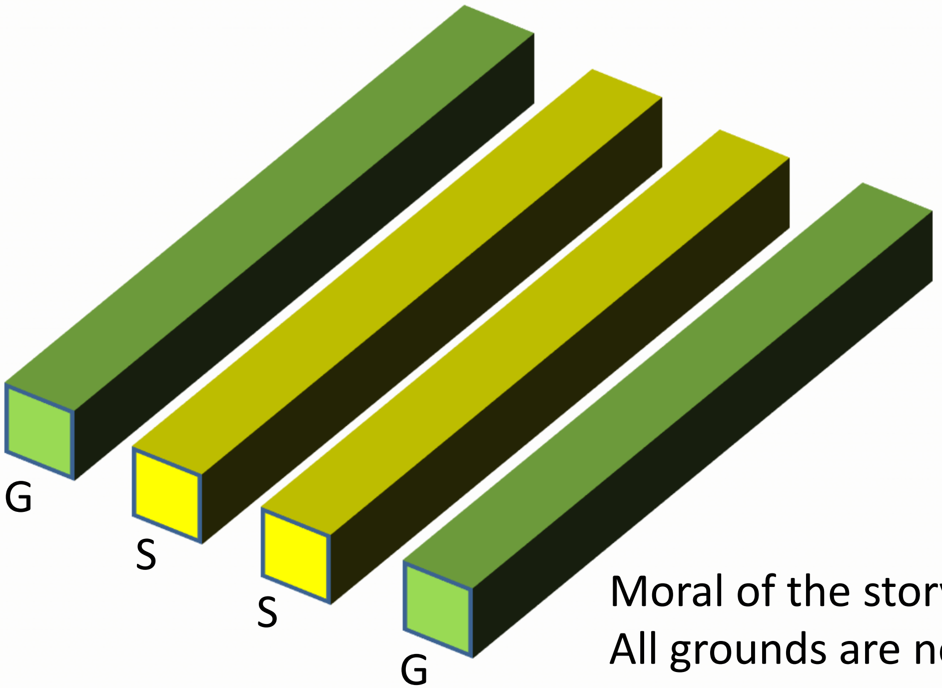

$[Z] = [R] + j\omega[L]$
$[Y] = [G] + j\omega[B]$

$\det\{\gamma_m^2 [U] - [Z][Y]\} = \mathbf{0}$
$\det\{\gamma_m^2 [U] - [Y][Z]\} = \mathbf{0}$

Moral of the story:
All grounds are not created equal.

$[S_I] = [Z]^{-1} [S_V] [\Gamma]$

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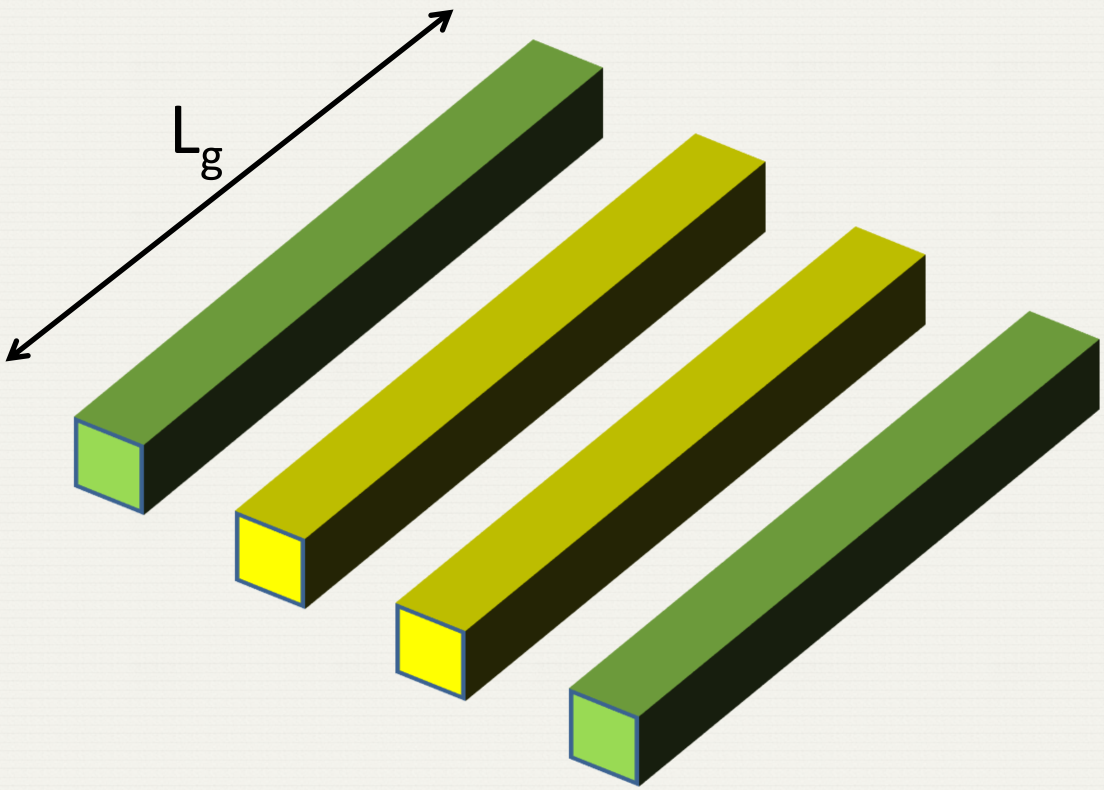
Why Multiple Resonant Frequencies?



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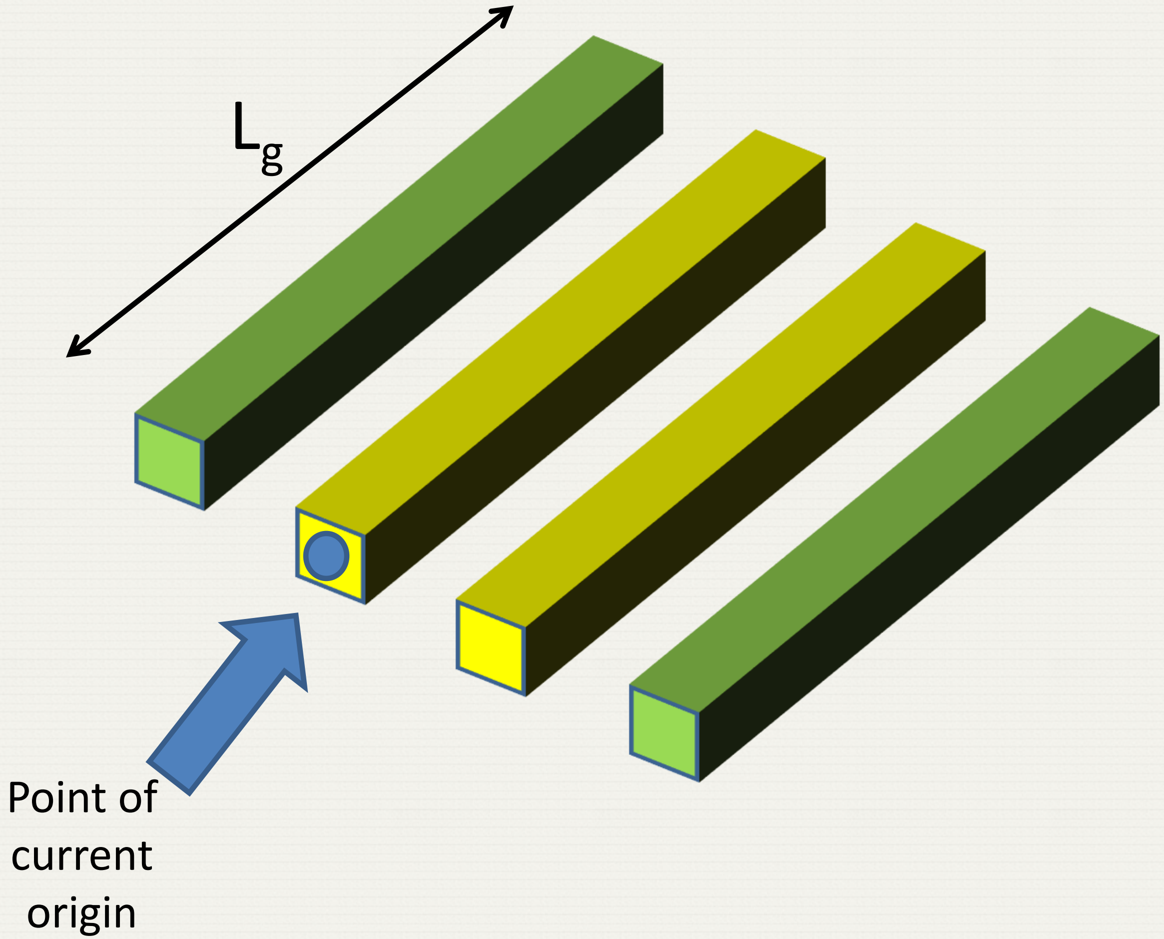

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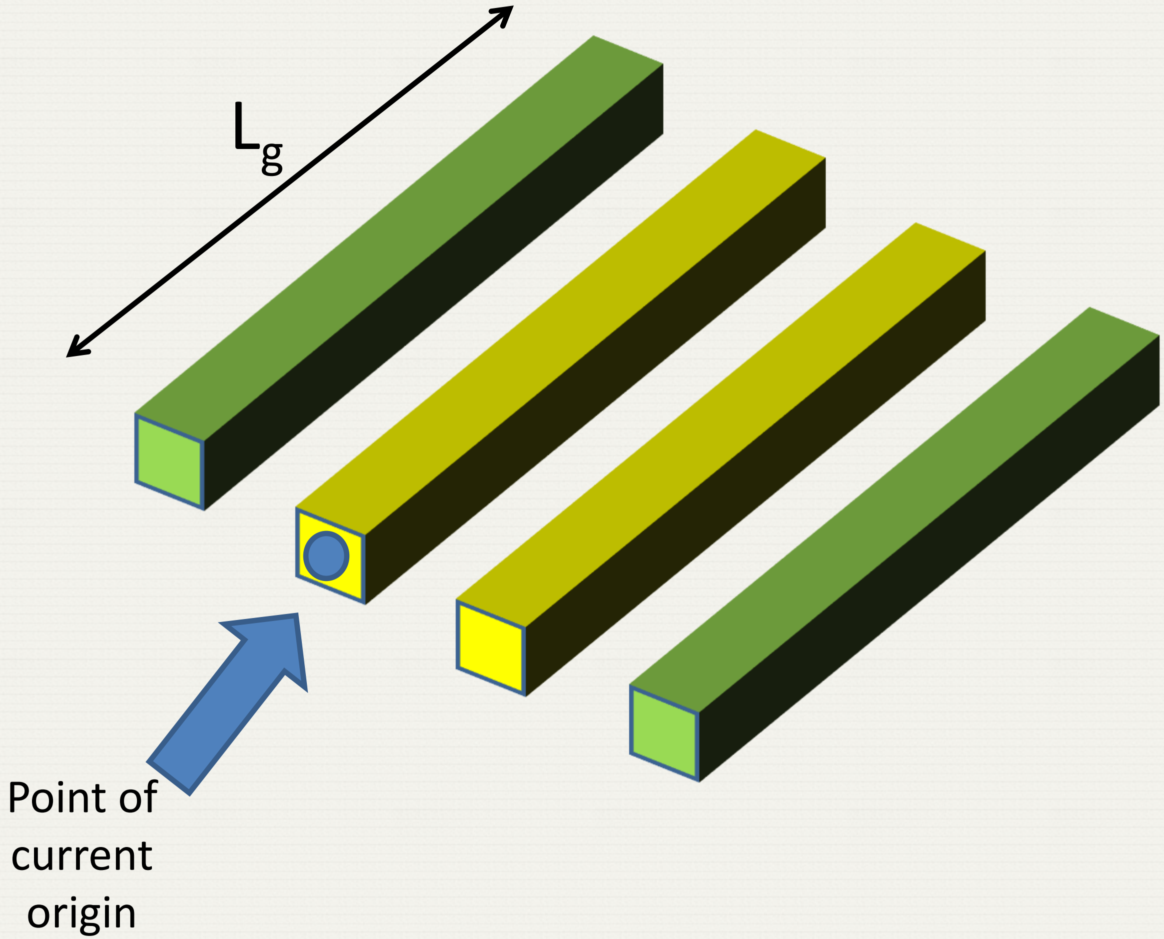

Total return path electrical length is what determines the frequency of resonance.

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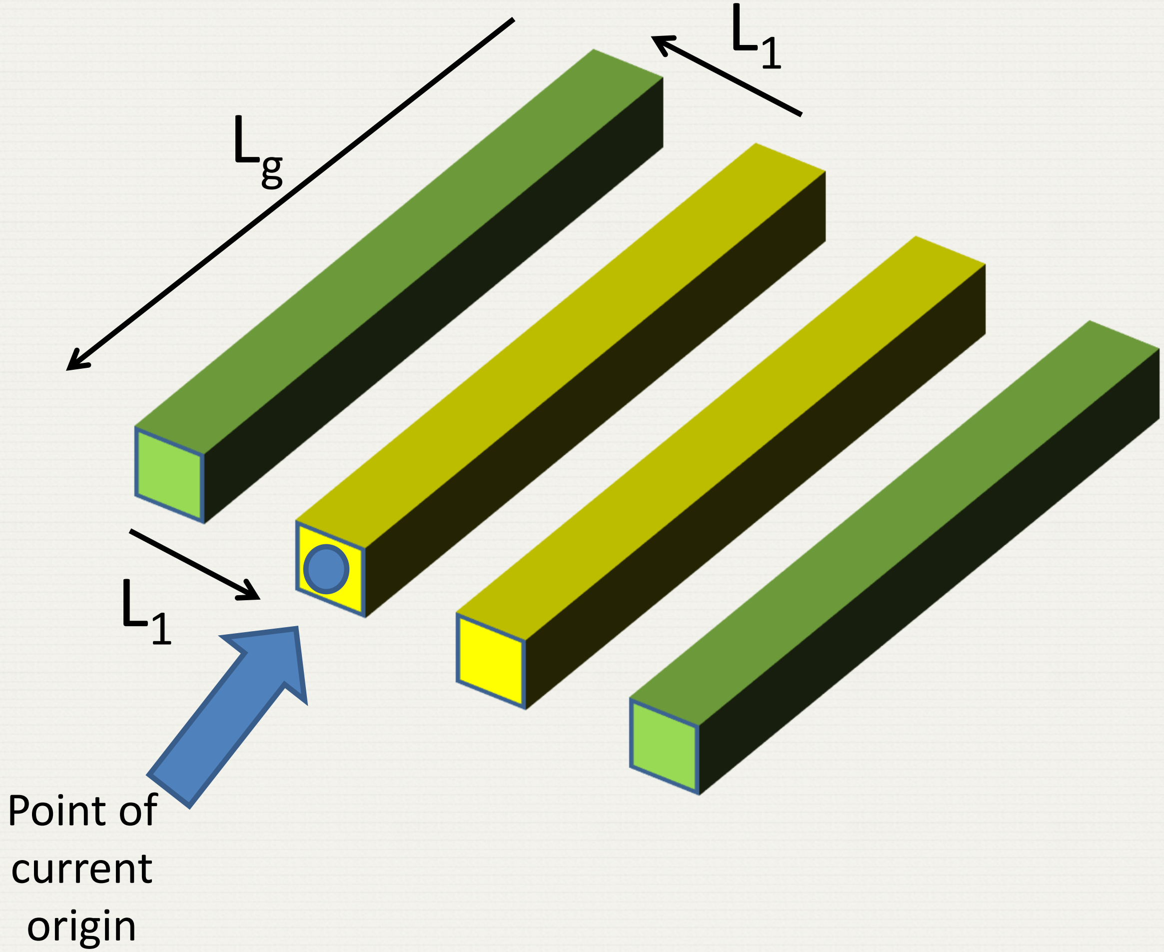

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In this case, $L_1+L_g+L_1$

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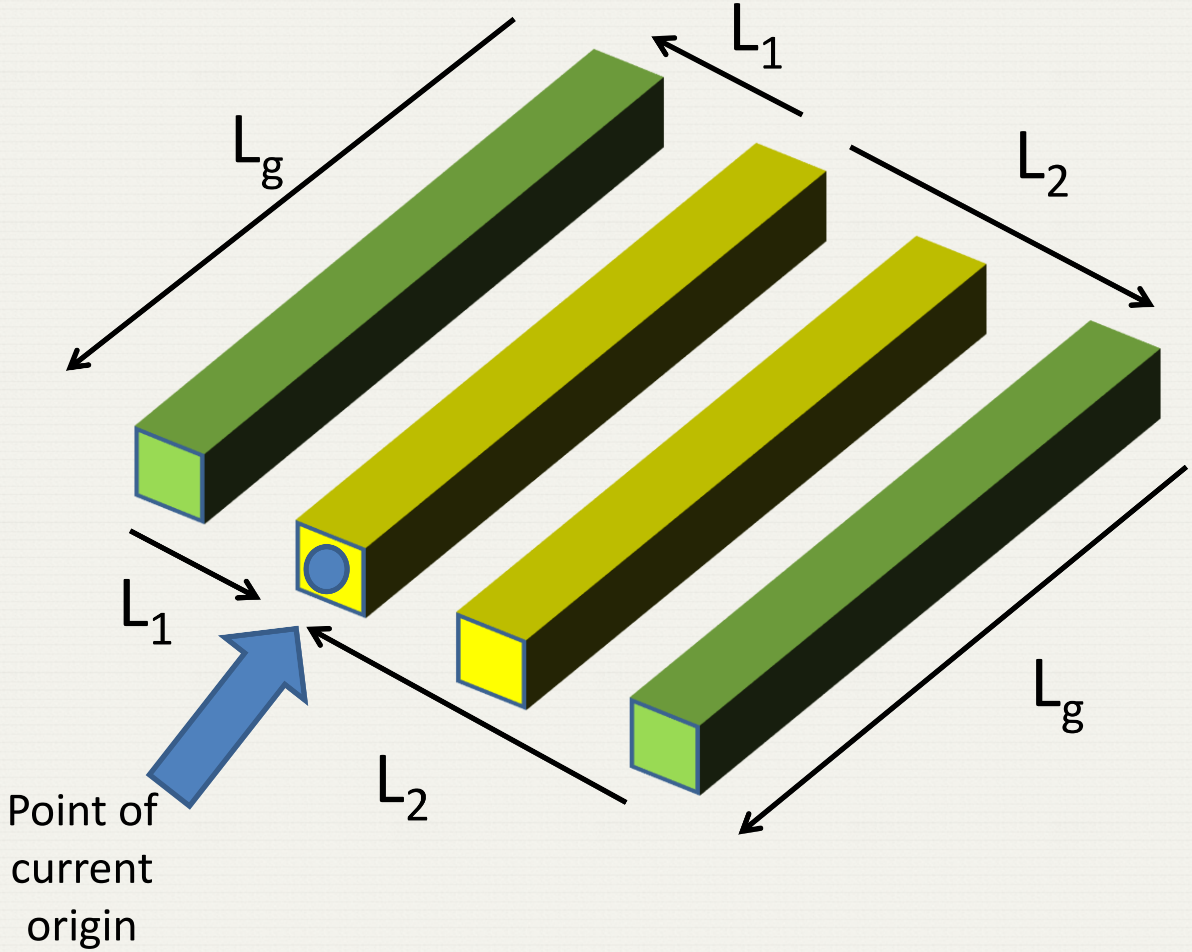


Total return path electrical length is what determines the frequency of resonance.

In this case,

$L_1+L_g+L_1$

or

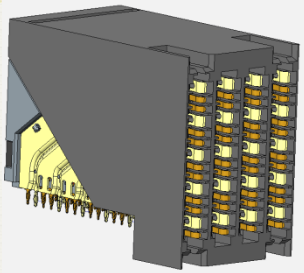
$L_2+L_g+L_2$

Minimizing Ground-Mode Resonance

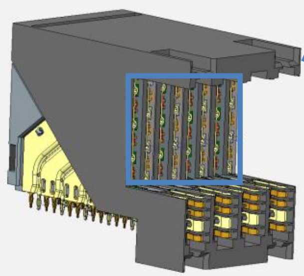
- When possible, use ground planes rather than discrete ground pins.
- Try to make the inductance of all discrete ground/return-paths similar if not equal.
- Prevent inductance “pinch points”, (i.e. particularly high-inductive ground paths).

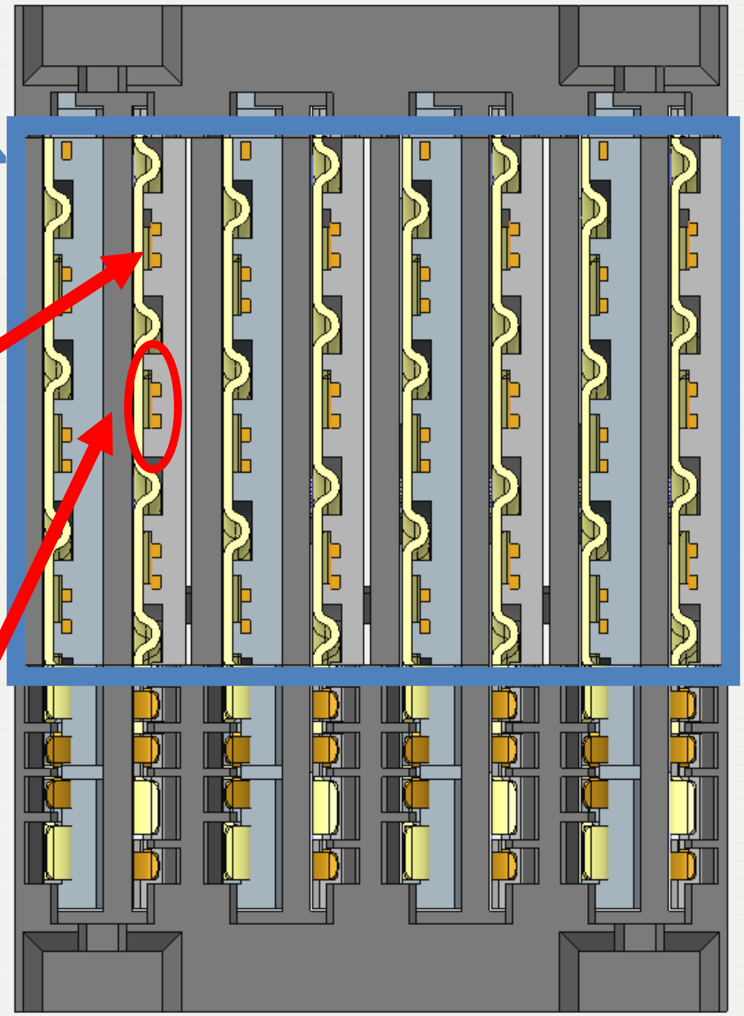
In-Pair Skew Prevention

no cut



with cut

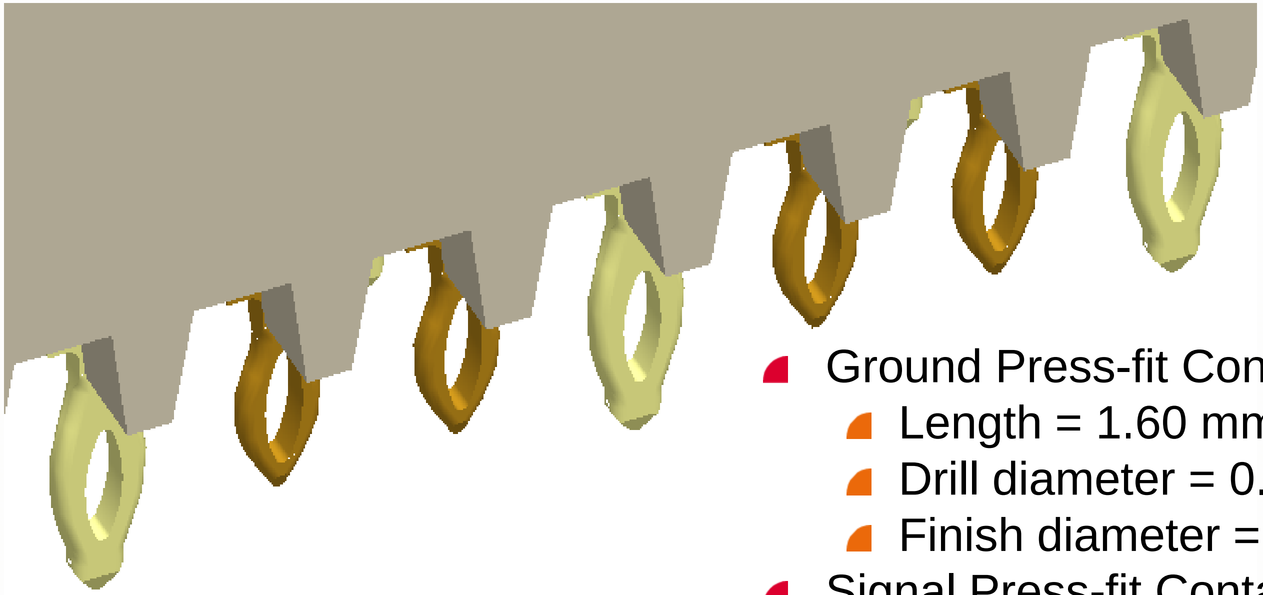




air pocket between signals and ground plane is offset to minimize skew

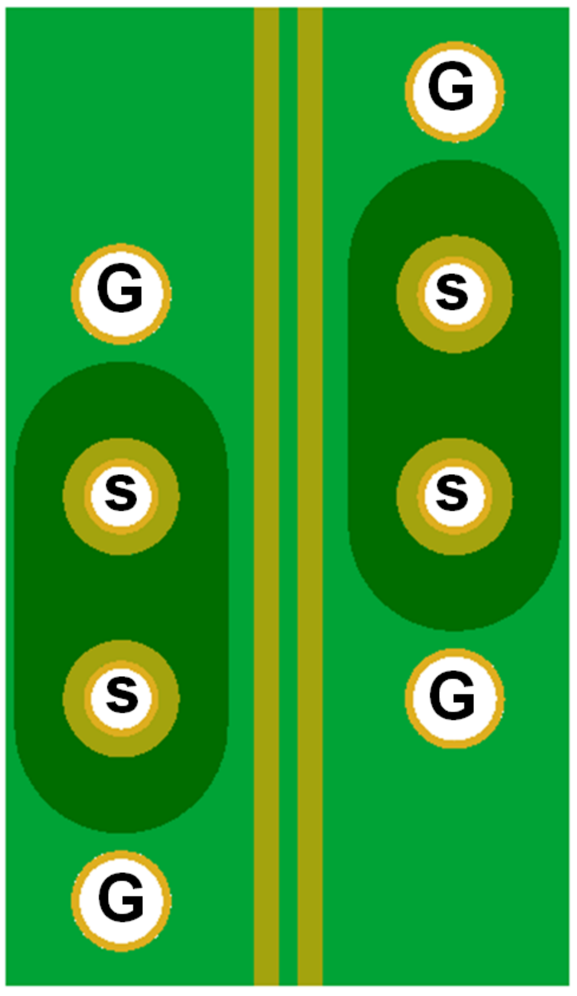
signal pair

EON Sizes and Footprint Dimensions



- Ground Press-fit Contact
  - Length = 1.60 mm
  - Drill diameter = 0.60 mm
  - Finish diameter = 0.50 mm
- Signal Press-fit Contact
  - Length = 1.40 mm
  - Drill diameter = 0.45 mm
  - Finish diameter = 0.36 mm

EON Sizes and Footprint Dimensions



	mils	mm
trace width	6	0.1524
trace-to-trace separation	4.3	0.1092
trace-to-antipad separation	6	0.1524
signal via drill Ø	17.7	0.45
signal via finish Ø	14	0.36
signal via pad Ø	27.7	0.70
ground via drill Ø	23.6	0.60
ground via finish Ø	20	0.50
antipad width	50.4	1.28
row pitch		1.2
column pitch		2.0

Daughter Cards

- Single-ended (50-ohm) routing to SMA connectors
- 16 channels (32 traces)
  - Explicit effort made to minimize trace crosstalk
- Megtron-6 substrate (minimize loss)
- Board thickness = 0.1 inch
- Backdrilling done such that maximum stub length was 6 ±3 mils

Daughter Card Stack Up

- Traces:
  - Width = 9.8 mils
  - Length = 5 inches
- Signals routed on layers 7 and 10
- Unused connector signal pins routed on layer 12 to 50-ohm terminations

Cu #	Impedance Required	Via Struct.	Cu %	Lyr. Thick. (in)	Materials	Core Only Thick. (in)	Supplier	Resin System
1			100	0.0006	1/2 oz			
				0.0050	1035		Panasonic	Megtron6
					1035		Panasonic	Megtron6
2			81		1/2 oz			
				0.0092		0.0080	Panasonic	Megtron6
3			81		1/2 oz			
				0.0102	2116		Panasonic	Megtron6
					2116		Panasonic	Megtron6
4			81		1/2 oz			
				0.0092		0.0080	Panasonic	Megtron6
5			81		1/2 oz			
				0.0102	2116		Panasonic	Megtron6
					2116		Panasonic	Megtron6
6			90		1/2 oz			
				0.0092		0.0080	Panasonic	Megtron6
7	✓		11		1/2 oz			
				0.0098	2116		Panasonic	Megtron6
					2116		Panasonic	Megtron6
8			90		1/2 oz			
				0.0092		0.0080	Panasonic	Megtron6
9			90		1/2 oz			
				0.0098	2116		Panasonic	Megtron6
					2116		Panasonic	Megtron6
10	✓		11		1/2 oz			
				0.0092		0.0080	Panasonic	Megtron6
11			90		1/2 oz			
				0.0050	1035		Panasonic	Megtron6
					1035		Panasonic	Megtron6
12	✓		100	0.0006	1/2 oz			

Lamination Thickness (in): Desired: **0.1000** Estimated: **0.0972** Actual: ____________

Wiring Assignment

N	M	L	K	J	I	H	G	F	E	D	C	B	A	
TER	X	TER	TER	X	TER	TER	X	TER	TER	X	TER	TER	X	6
X	TX8-	TX8+	X	TX7-	TX7+	X	RX8-	RX8+	X	RX7-	RX7+	X	TER	5
TER	X	TX6-	TX6+	X	RX5-	RX5+	X	RX6-	RX6+	X	TX5-	TX5+	X	4
X	TX4-	TX4+	X	TX3-	TX3+	X	RX4-	RX4+	X	RX3-	RX3+	X	TER	3
TER	X	TX2-	TX2+	X	RX1-	RX1+	X	RX2-	RX2+	X	TX1-	TX1+	X	2
X	TER	TER	X	TER	TER	X	TER	TER	X	TER	TER	X	TER	1

The First Backplane

- Differential (100-ohm) routing
- Megtron-6 substrate (minimize loss)
- HVLP Cu roughness
- Board thickness = 0.23 inch
- Backdrilling done such that maximum stub length was 6 ±3 mils (same as daughter cards)

Backplane Stack Up

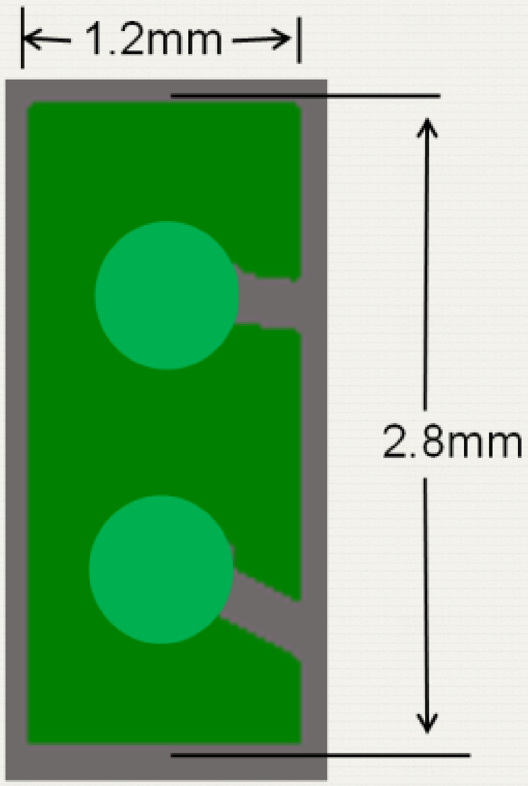
- Traces:
  - Width and separation: 10/11/10 (mils)
  - 7.5/5.5/7.5 in footprint
  - Length = 17 inches (OIF)
- Signals routed on layers 4, 6, 9 and 11
- Dielectric layers were fairly thick (≈10 mils)

Cu #	Impedance Required	Via Struct.	Cu %	Lyr. Thick. (in)	Supplier	Resin System	Core Only Thick. (in)	Materials
1			100	0.0006				1/2 oz
					Panasonic	Megtron6		2116
				0.0207	Panasonic	Megtron6		2116
					Panasonic	Megtron6		2116
					Panasonic	Megtron6		2116
2			86					1/2 oz
				0.0172	Panasonic	Megtron6	0.0160	
3			87					1/2 oz
					Panasonic	Megtron6		2116
				0.0105	Panasonic	Megtron6		1080
					Panasonic	Megtron6		1080
4	✓		20					1/2 oz
				0.0112	Panasonic	Megtron6	0.0100	
5			87					1/2 oz
					Panasonic	Megtron6		1080
				0.0105	Panasonic	Megtron6		1080
					Panasonic	Megtron6		2116
6	✓		20					1/2 oz
				0.0112	Panasonic	Megtron6	0.0100	
7			87					1/2 oz
				0.0051	Panasonic	Megtron6		2116
				0.0390	Isola	370 HR	0.0390	
				0.0051	Panasonic	Megtron6		2116
8			86					1/2 oz
				0.0112	Panasonic	Megtron6	0.0100	
9	✓		20					1/2 oz
					Panasonic	Megtron6		2116
				0.0105	Panasonic	Megtron6		1080
					Panasonic	Megtron6		1080
10			86					1/2 oz
				0.0112	Panasonic	Megtron6	0.0100	
11	✓		20					1/2 oz
					Panasonic	Megtron6		1080
				0.0105	Panasonic	Megtron6		1080
					Panasonic	Megtron6		2116
12			86					1/2 oz
				0.0172	Panasonic	Megtron6	0.0160	
13			87					1/2 oz
					Panasonic	Megtron6		2116
				0.0207	Panasonic	Megtron6		2116
					Panasonic	Megtron6		2116
					Panasonic	Megtron6		2116
14			100	0.0006				1/2 oz

Lamination Thickness (in): Desired: 0.2300 Estimated: 0.2132 Actual: ______________

Antipad Design

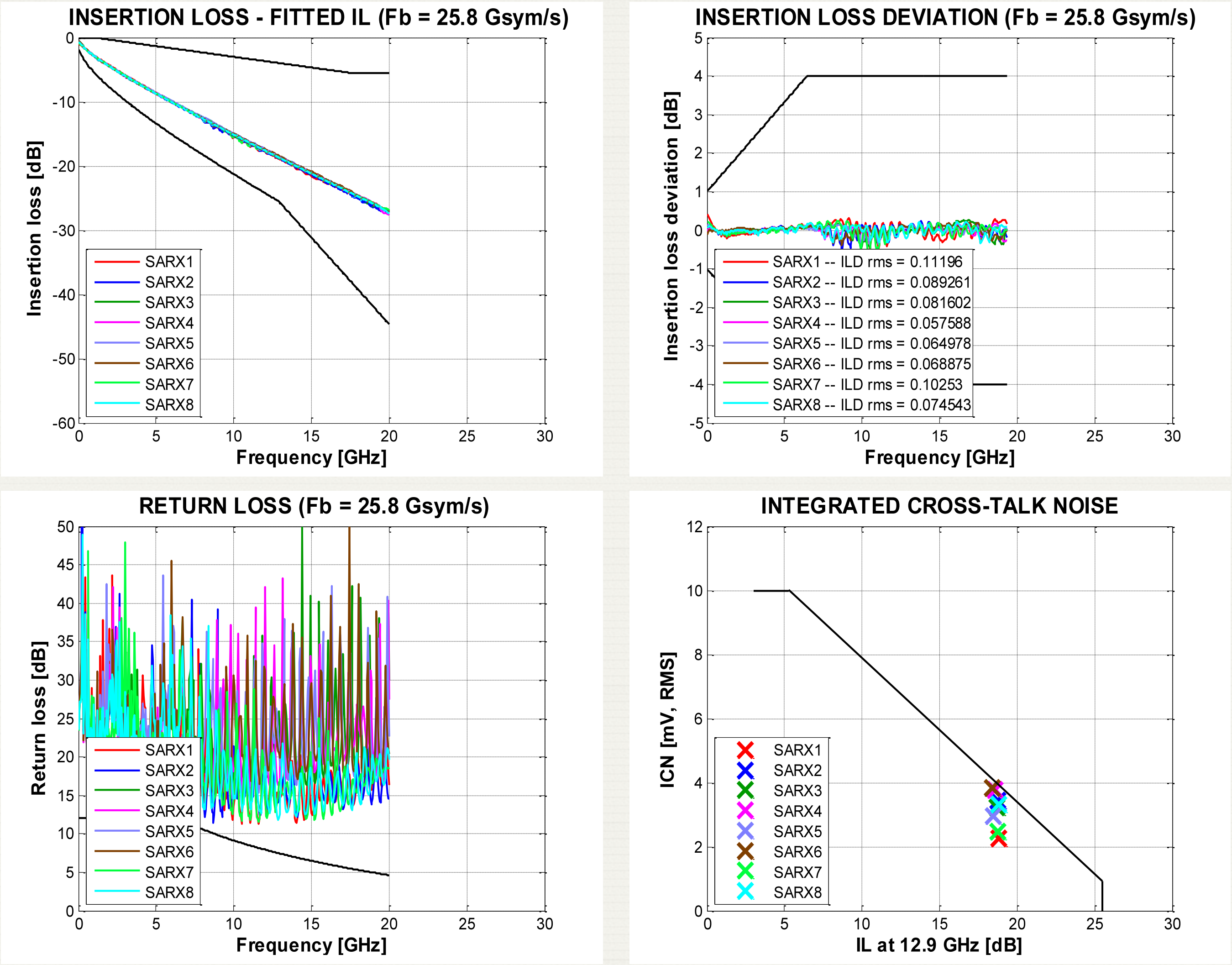
- Fairly large antipad designed to minimize impedance (capacitive) mismatch in footprint
- “Diving boards” implemented underneath traces in antipad to reduce ground starvation



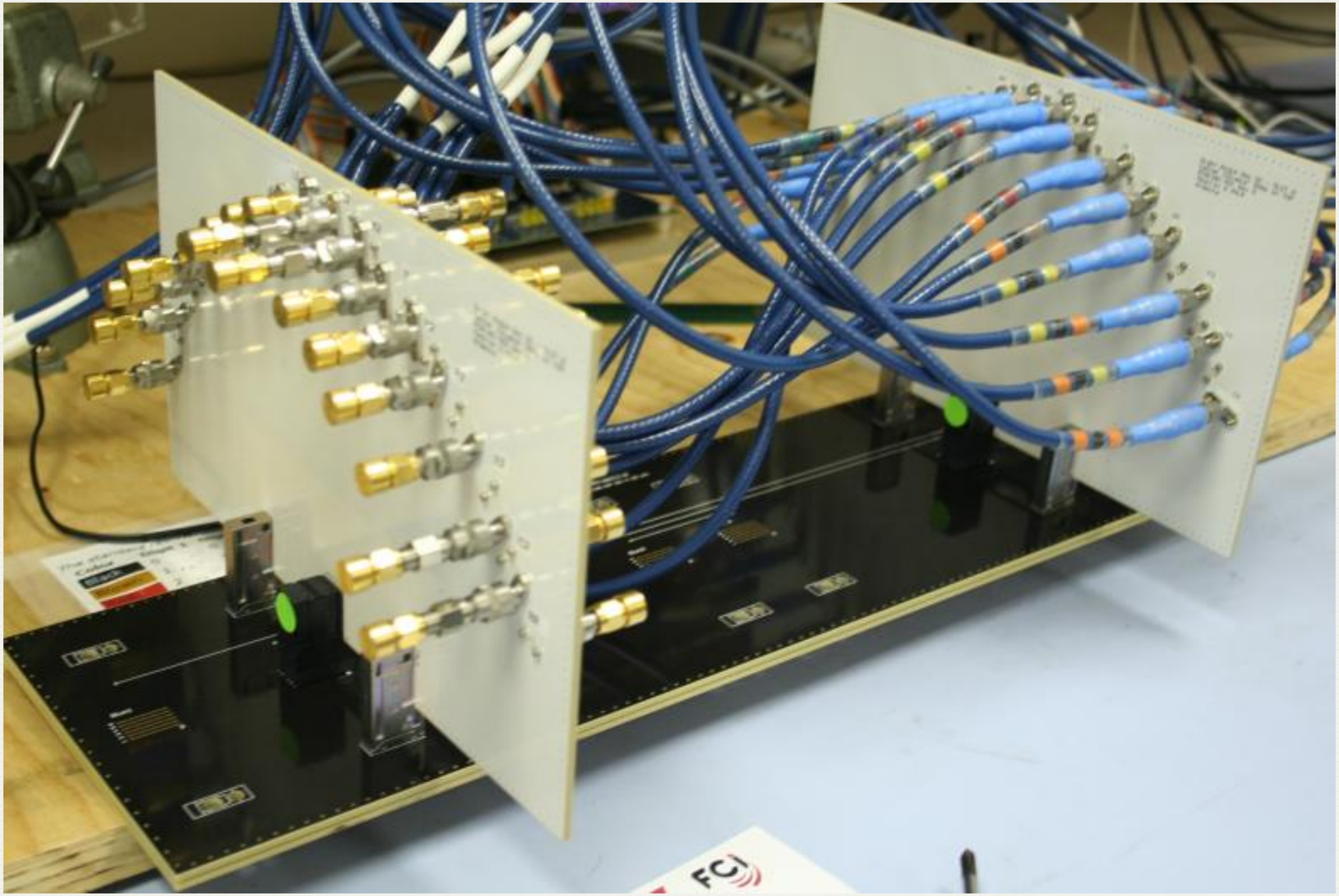
Summary of OIF Requirements

- CEI-25G-LR Specification places limits on channel
  - Insertion Loss (I.L.)
  - Insertion Loss Deviation (ILD)
  - ILD RMS (must be <0.3)
  - Return Loss (R.L.)
  - Integrated Crosstalk Noise (ICN)
    - Plotted against Insertion Loss at Nyquist frequency (12.9 GHz for 25 Gb/s)
- Maximum channel length = 27 inches (686 mm)

Channel Simulation Results

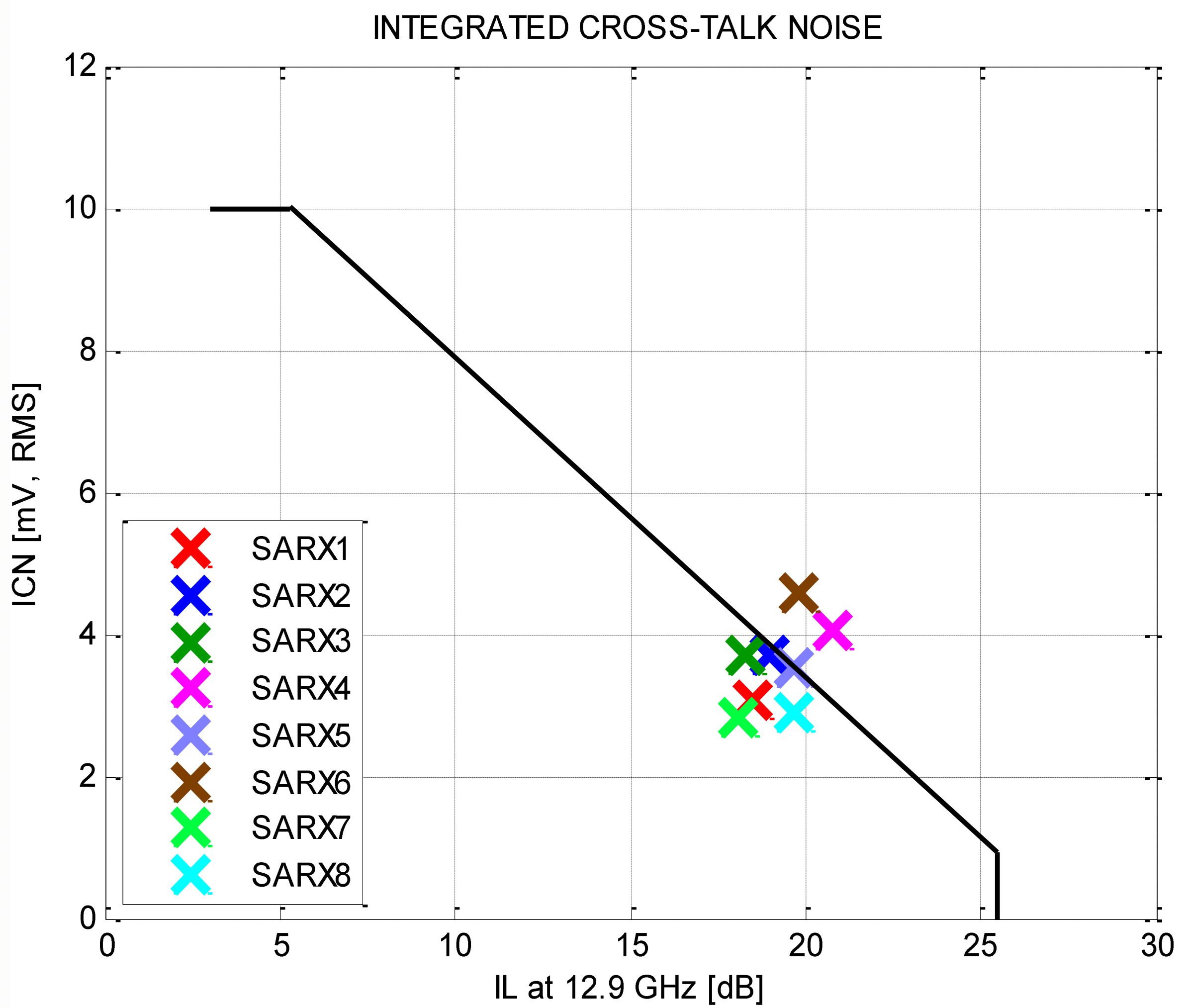


The Backplane System



Failure of Measurements

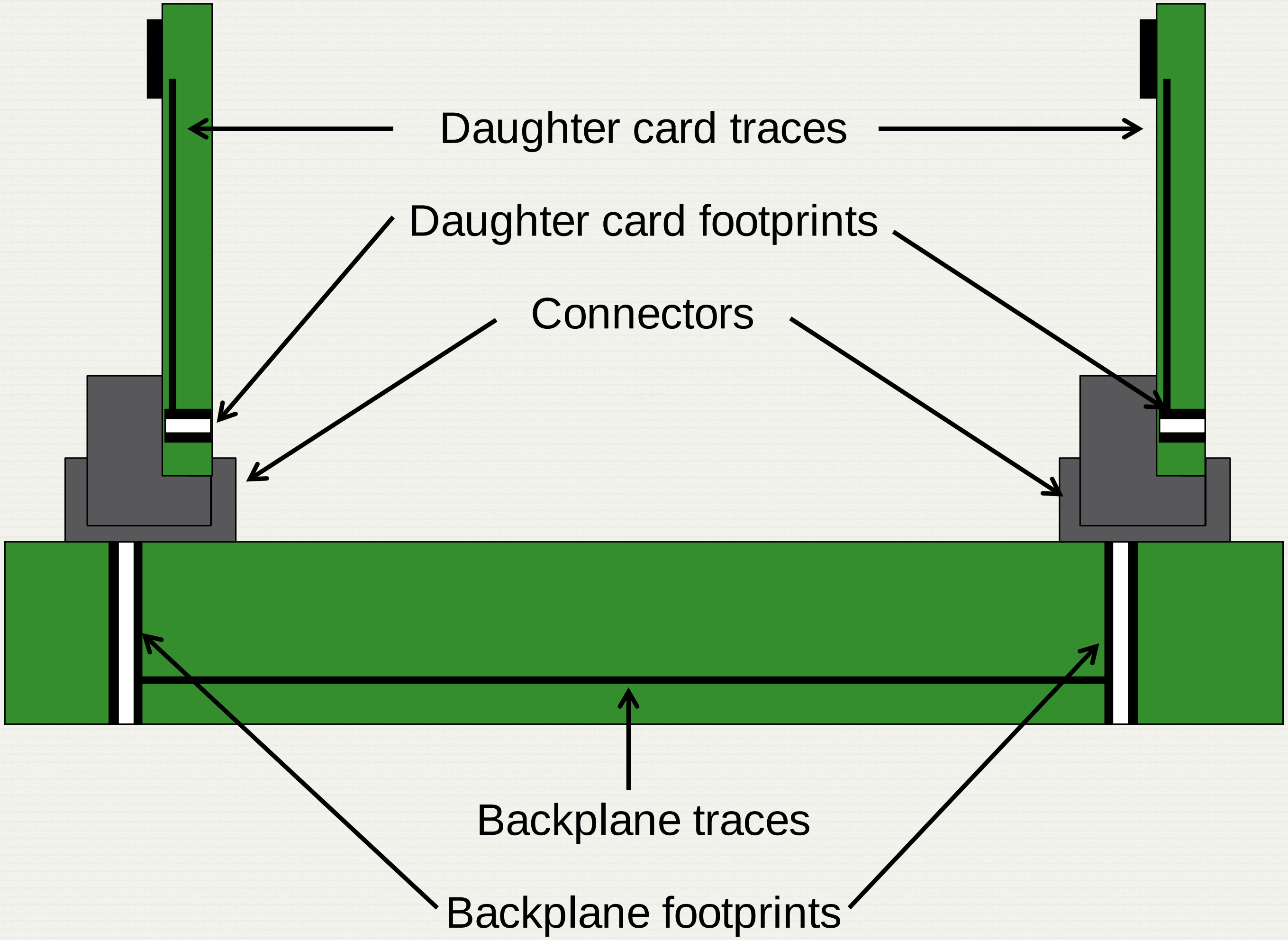
- One quarter of the channels failed the ICN requirement



Debugging of Simulation

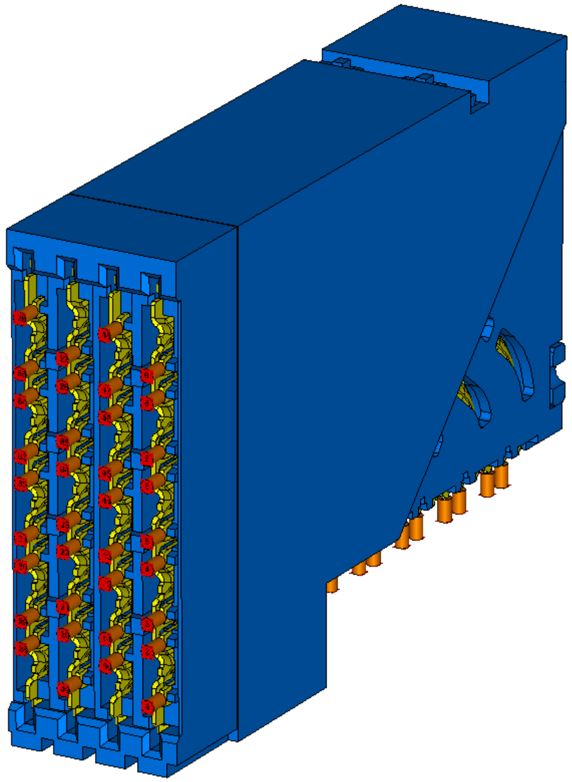
- Simulation consisted of obtaining and cascading together S-parameter (Touchstone) models of each of the channel components
  - Two sets of daughter card traces
  - Two sets of daughter card connector footprints
  - Two connectors
  - Two sets of backplane connector footprints
  - One set of backplane traces

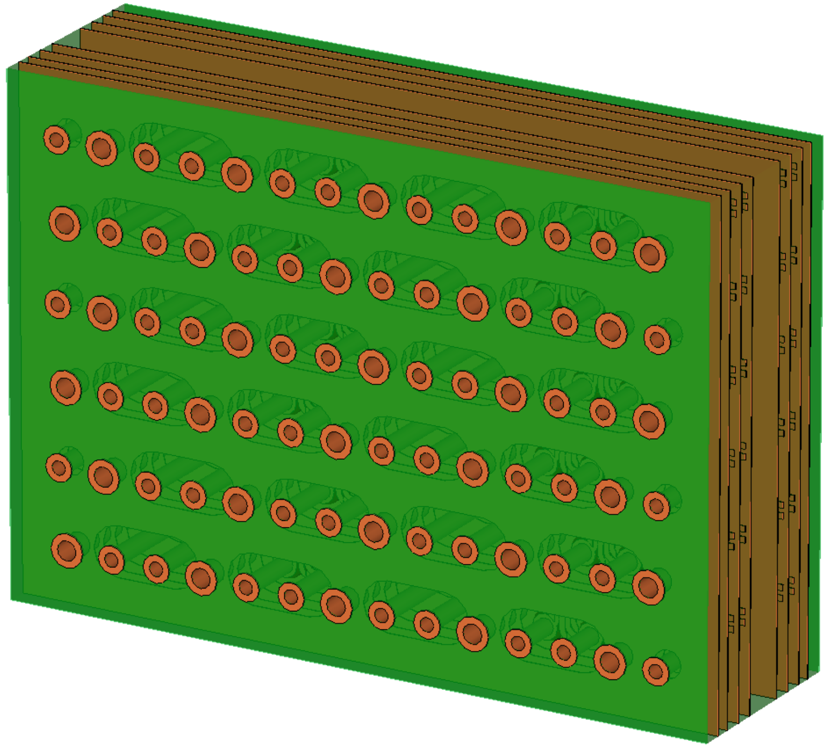
Diagram of Link



Explanation of Component Models

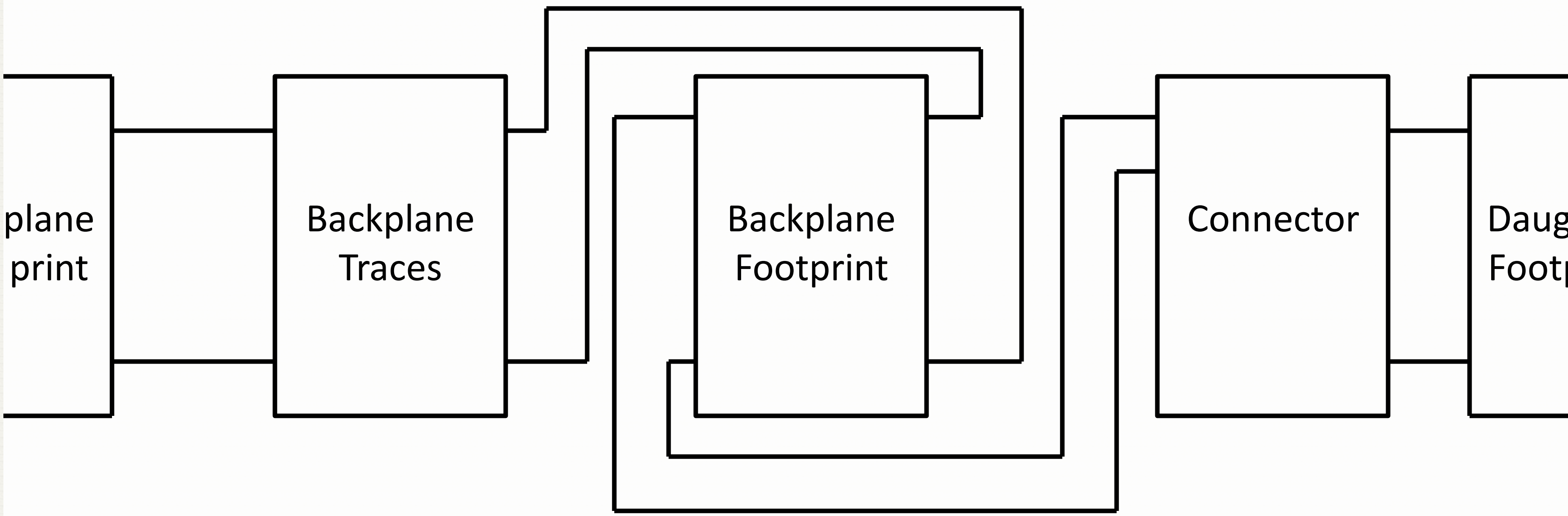
- Traces were frequency-dependent RLGC models
- Connectors and footprints models from CST MWS



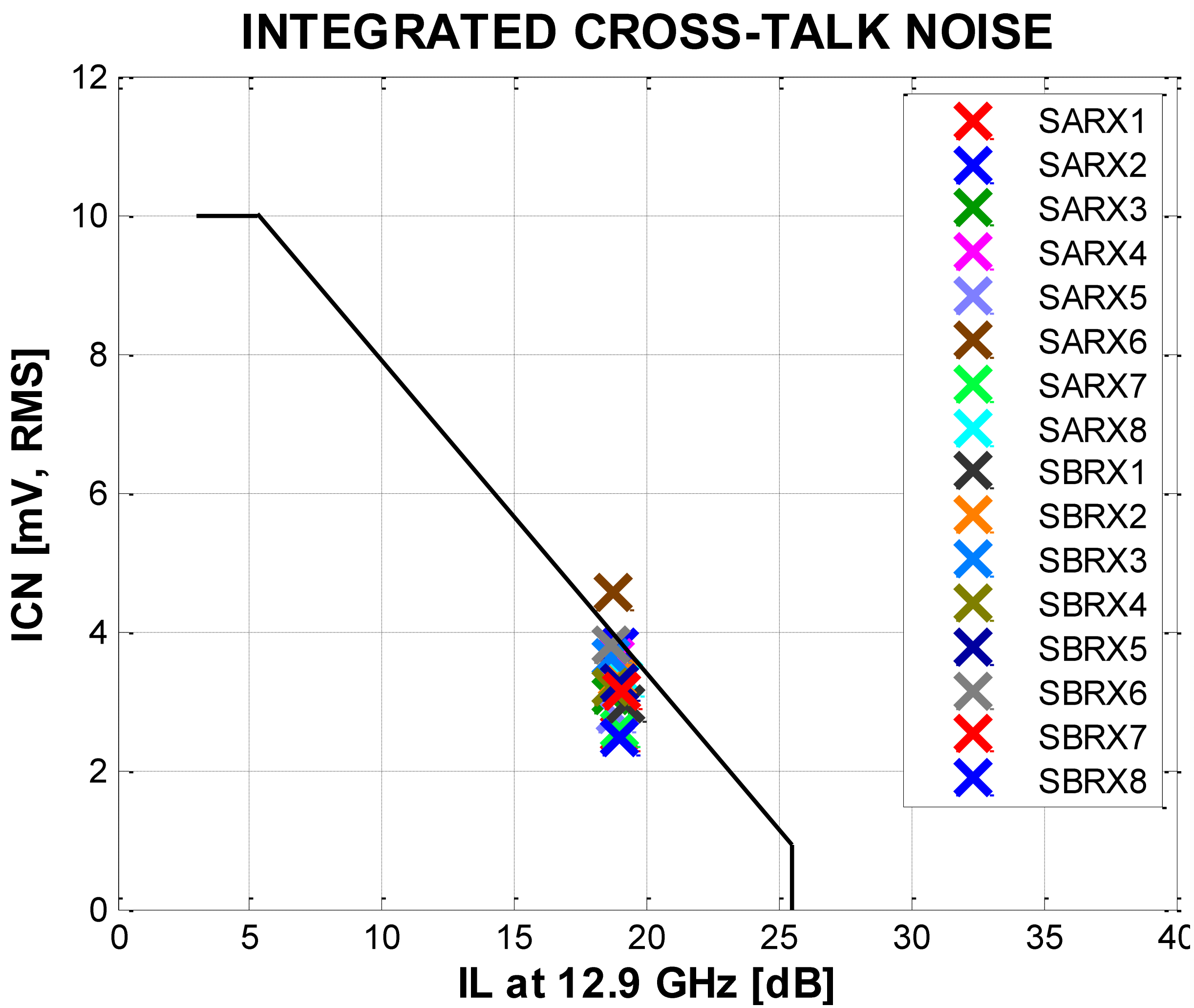


Explanation of Mistake

- The far-side backplane footprint model was connected backwards, (i.e. miswired)



Corrected Simulation

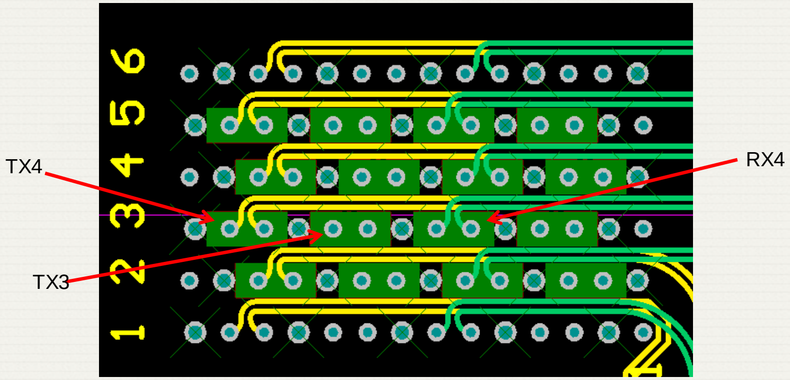


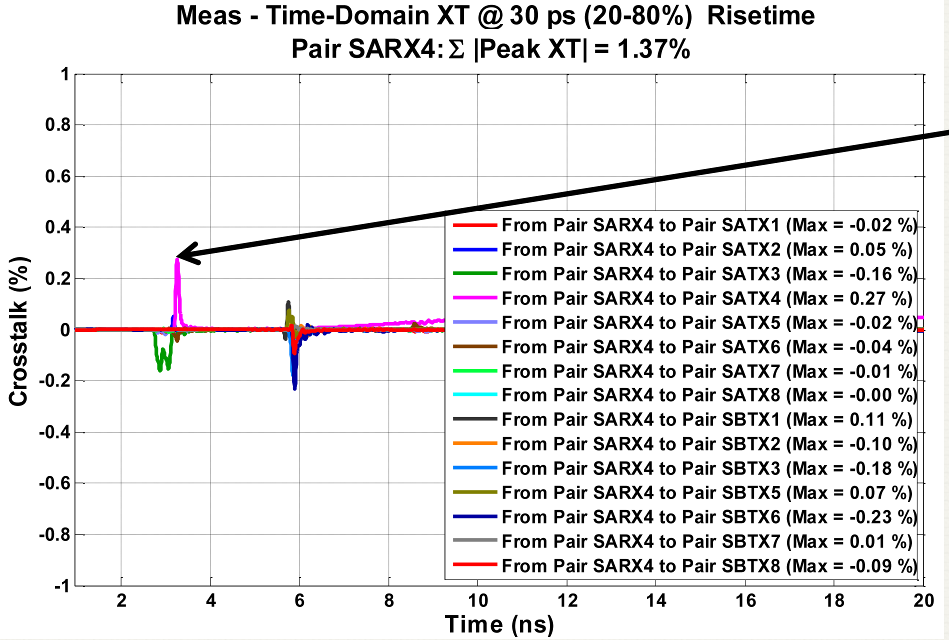
The corrected simulation failed just like the measurements.

Hooray!?!

Failure Mechanism

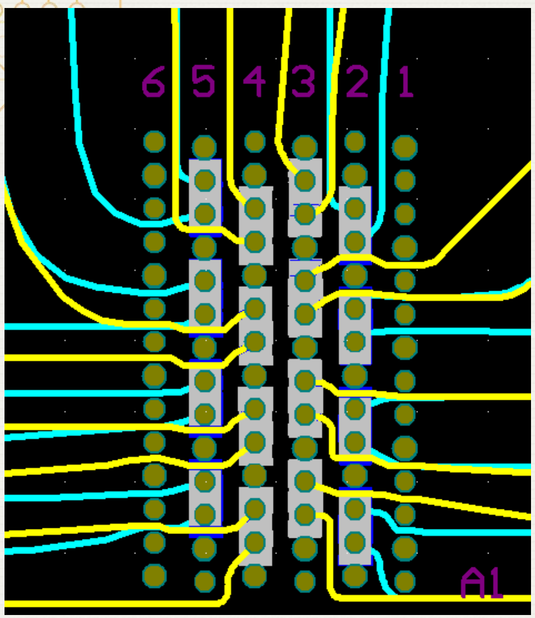
	N	M	L	K	J	I	H	G	F	E	D	C	B	A
6	TER	X	TER	TER	X	TER	TER	X	TER	TER	X	TER	TER	X
5	X	TX8-	TX8+	X	TX7-	TX7+	X	RX8-	RX8+	X	RX7-	RX7+	X	TER
4	TER	X	TX6-	TX6+	X	RX5-	RX5+	X	RX6-	RX6+	X	TX5-	TX5+	X
3	X	TX4-	TX4+	X	TX3-	TX3+	X	RX4-	RX4+	X	RX3-	RX3+	X	TER
2	TER	X	TX2-	TX2+	X	RX1-	RX1+	X	RX2-	RX2+	X	TX1-	TX1+	X
1	X	TER	TER	X	TER	TER	X	TER	TER	X	TER	TER	X	TER

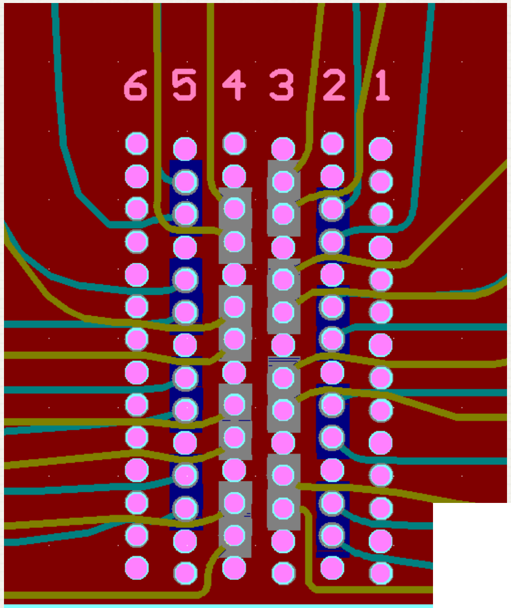




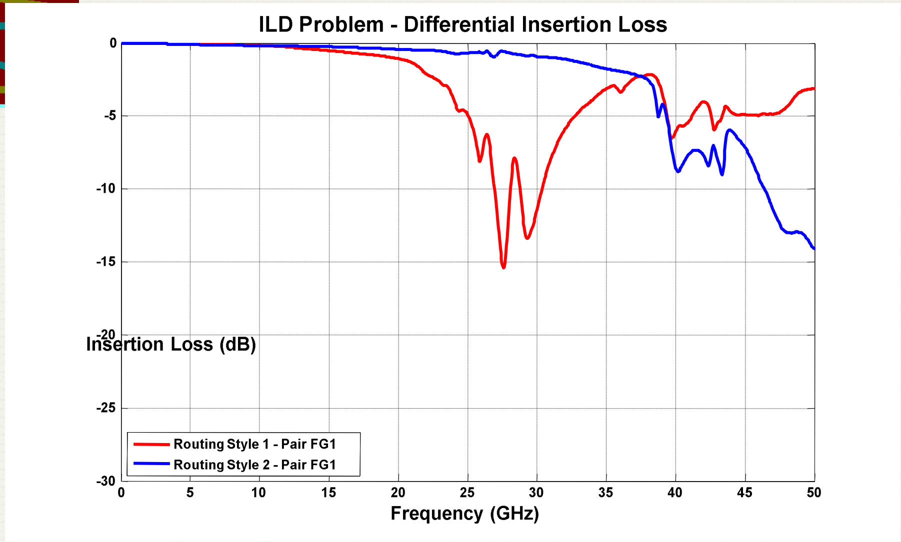
Layer-to-layer crosstalk in the footprint

Ancillary Fix to Daughter Cards

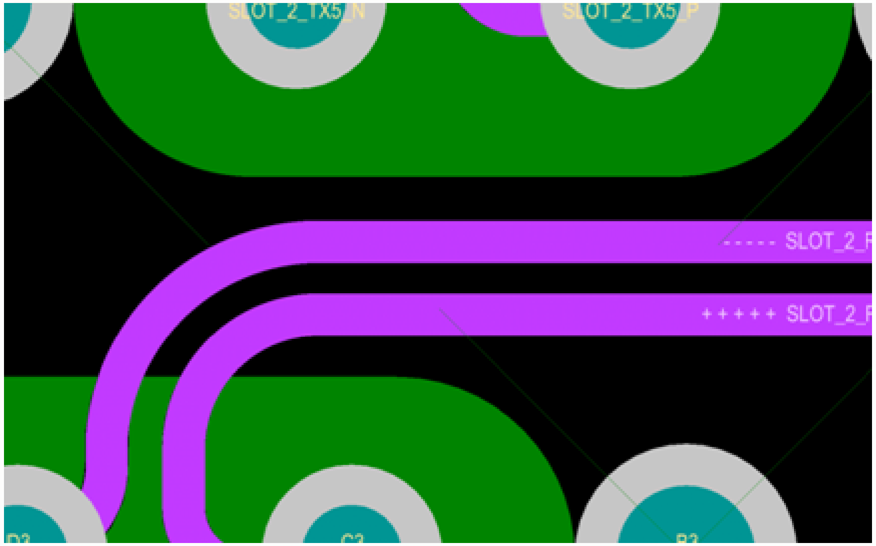




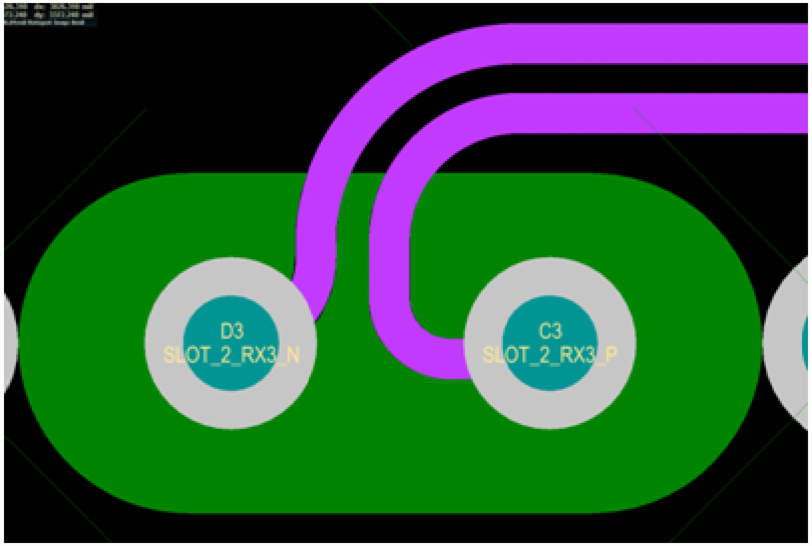
Asymmetrical wiring around signal vias caused problems with ILD.



The Second Backplane



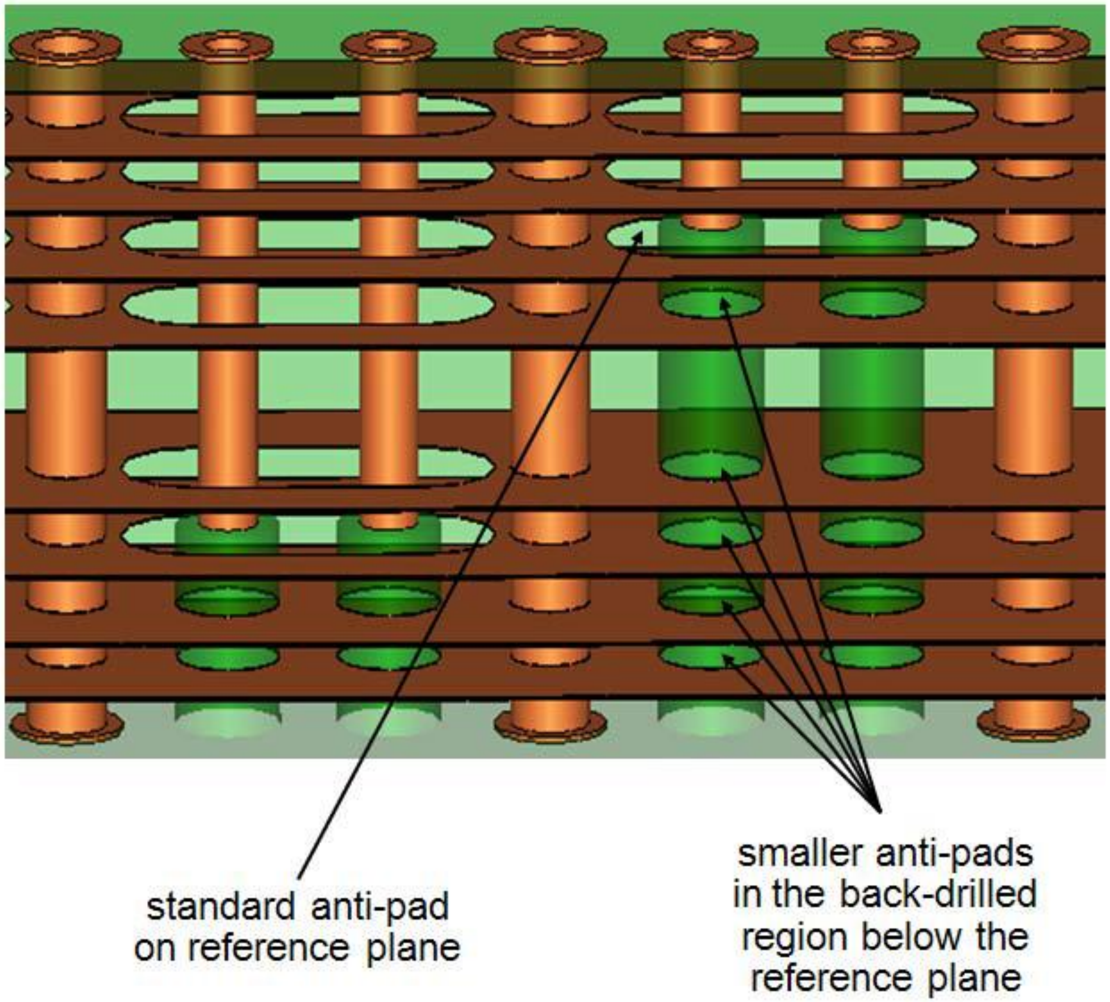
6 mil antipad-to-trace gap



Zero-skew breakout in the backplane footprint region

- Maintaining 6-mil gap reduced between-layer XT
- Zero skew was implemented in the FP routing

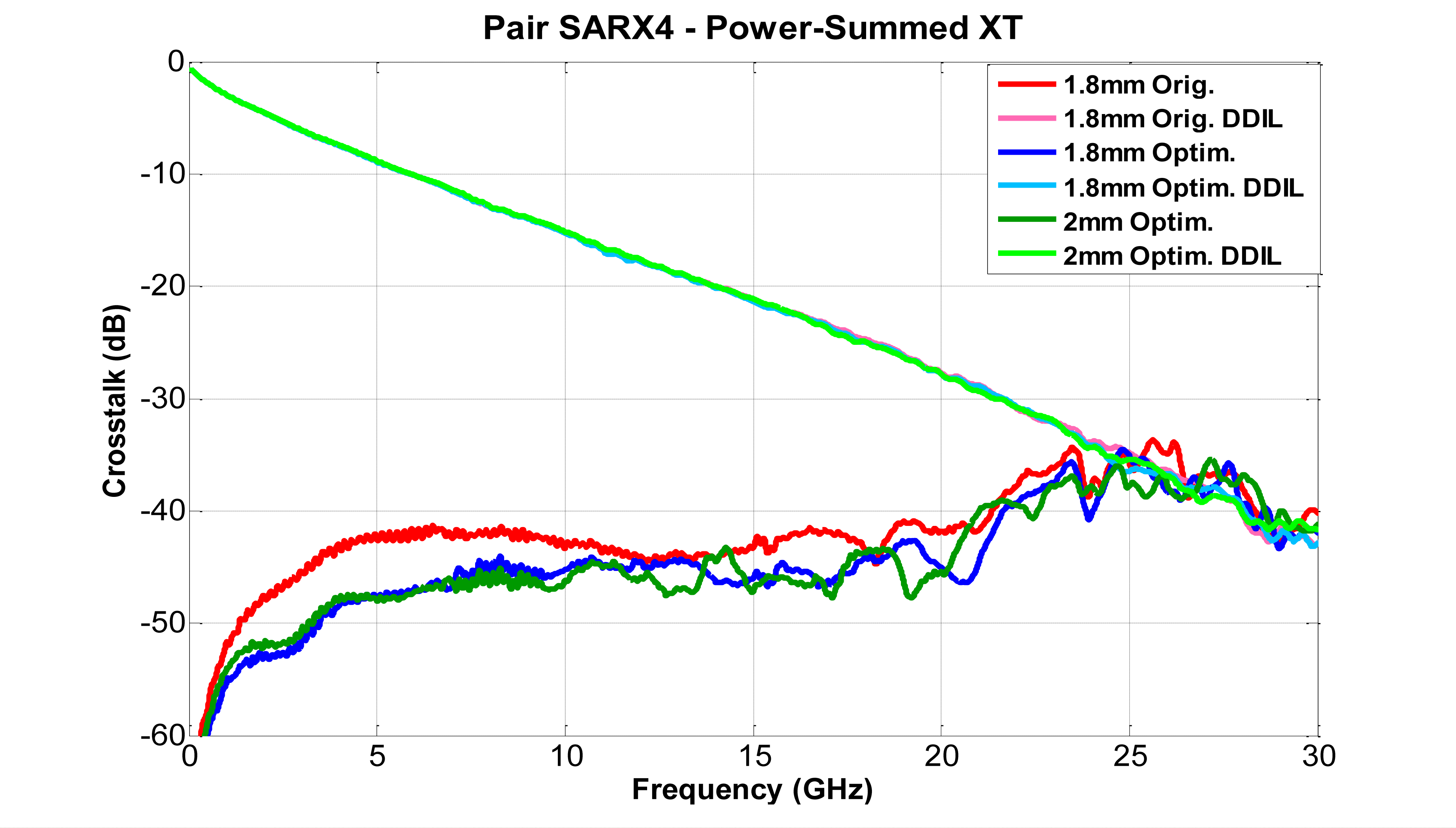
The Second Backplane



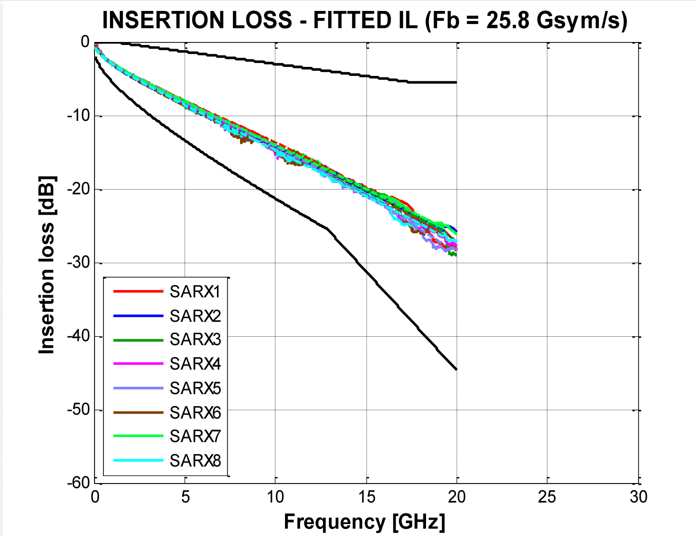
Antipad size was reduced in lower layers where backdrilling was done.

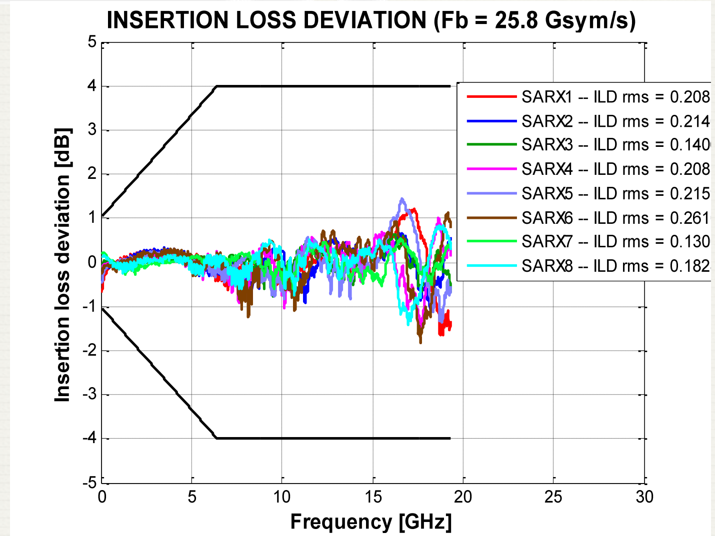
Yet more between-layer crosstalk reduction

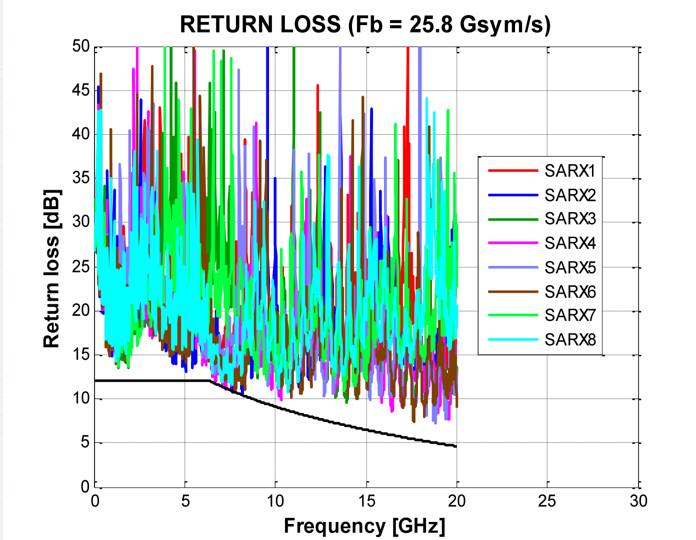
The Second Backplane

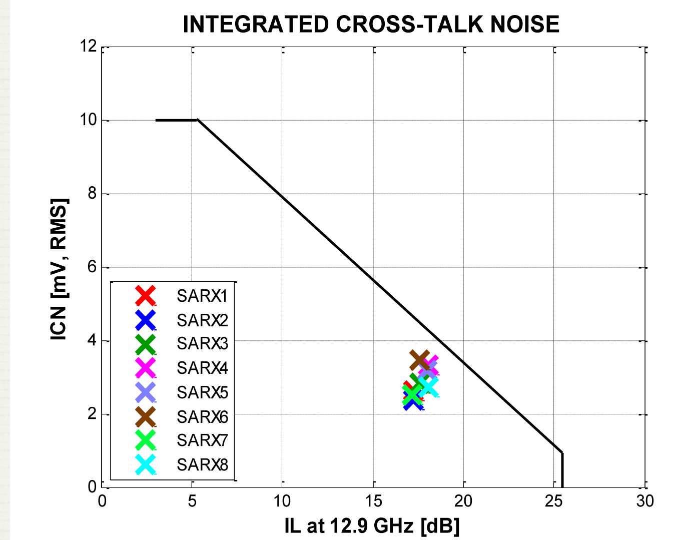


Compliance with OIF Specification









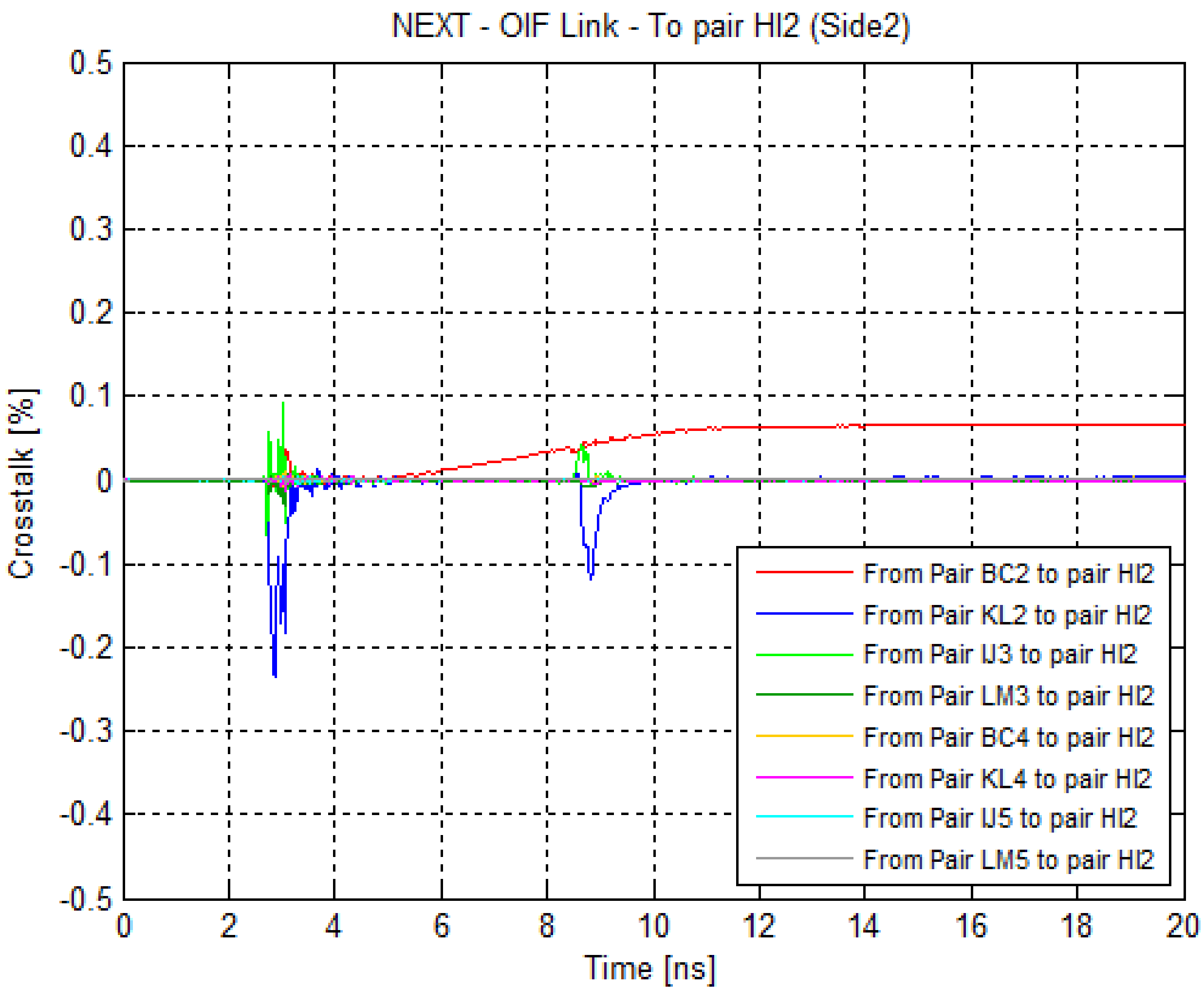
Compliance with IEEE Specification

- The backplane system included 16 channels of length 1 meter to test against the requirements of the IEEE 802.3bj (Post Draft 2.1v2 release) Channel Operating Margin (COM) Tool.

- Additionally, it worked (error-free) with 25 Gb/s SerDes from three different chip manufacturers.

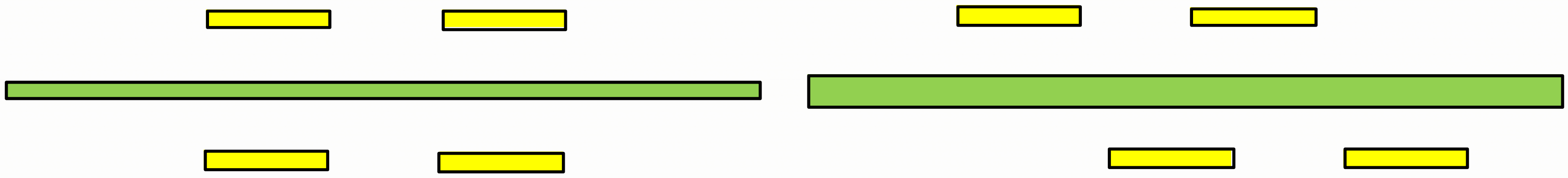
ExaMAX 1m IEEE Link - NRZ Config 1	
	COM
Pr 1 to Pr 17	6.39
Pr 2 to Pr 18	6.15
Pr 3 to Pr 19	5.89
Pr 4 to Pr 20	5.93
Pr 5 to Pr 21	5.70
Pr 6 to Pr 22	5.99
Pr 7 to Pr 23	6.72
Pr 8 to Pr 24	6.21
Pr 25 to Pr 9	6.43
Pr 26 to Pr 10	6.17
Pr 27 to Pr 11	5.76
Pr 28 to Pr 12	5.89
Pr 29 to Pr 13	6.02
Pr 30 to Pr 14	6.01
Pr 31 to Pr 15	6.81
Pr 32 to Pr 16	6.30

Unexpected Low-Frequency Crosstalk



Low-frequency crosstalk (plotted in red) occurring throughout the entire routing of the backplane for some of the channels

Unexpected Low-Frequency Crosstalk

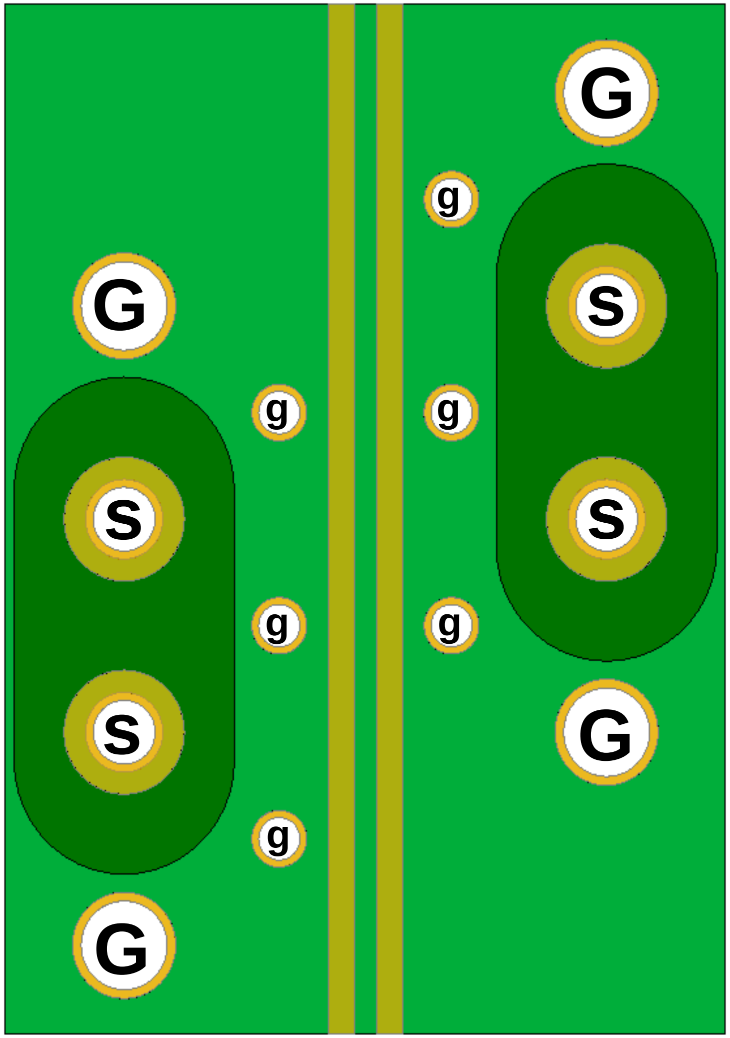


- Reduce magnetic coupling between adjacent signal layers by:
  - Increasing the thickness of the separating ground plane to at least 1-oz. Cu
  - Staggering traces on adjacent layers such that they are not in perfect registration with each other

Errata

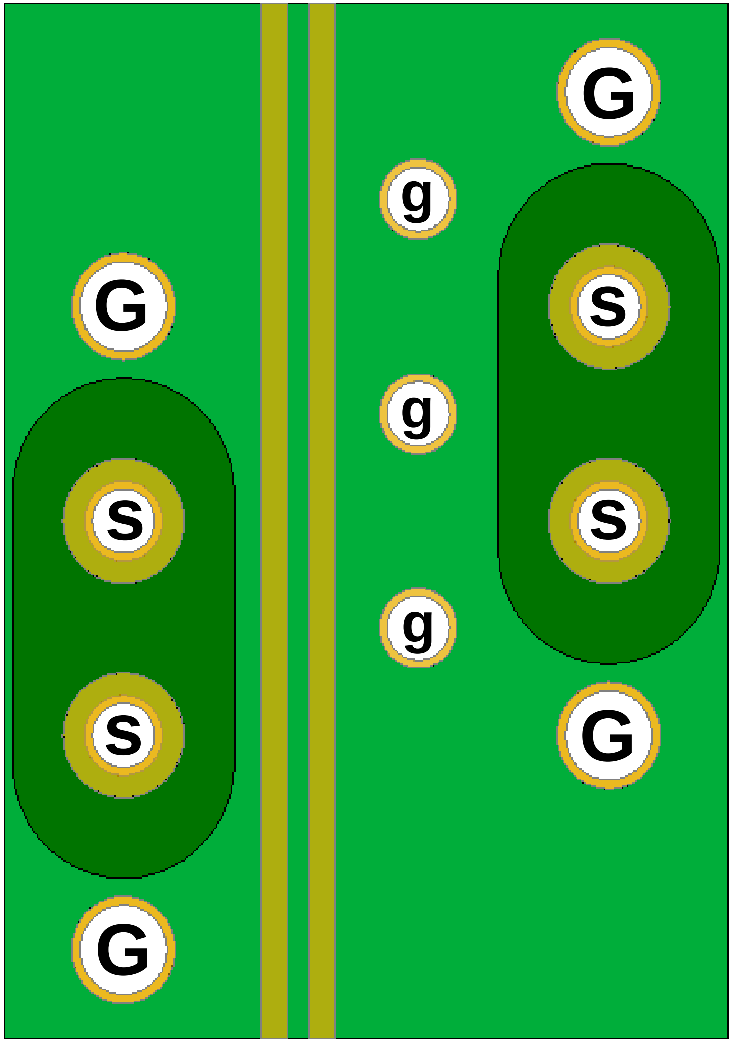
- In the paper, the minimum margin requirement for the IEEE 802.3bj Channel Operating Margin (COM) tool when using PAM4 modulation is listed as being 5 dB. This is incorrect.
- The correct minimum margin requirement is 3 dB, (i.e. the same as for NRZ modulation.)

Beyond 25 Gb/s



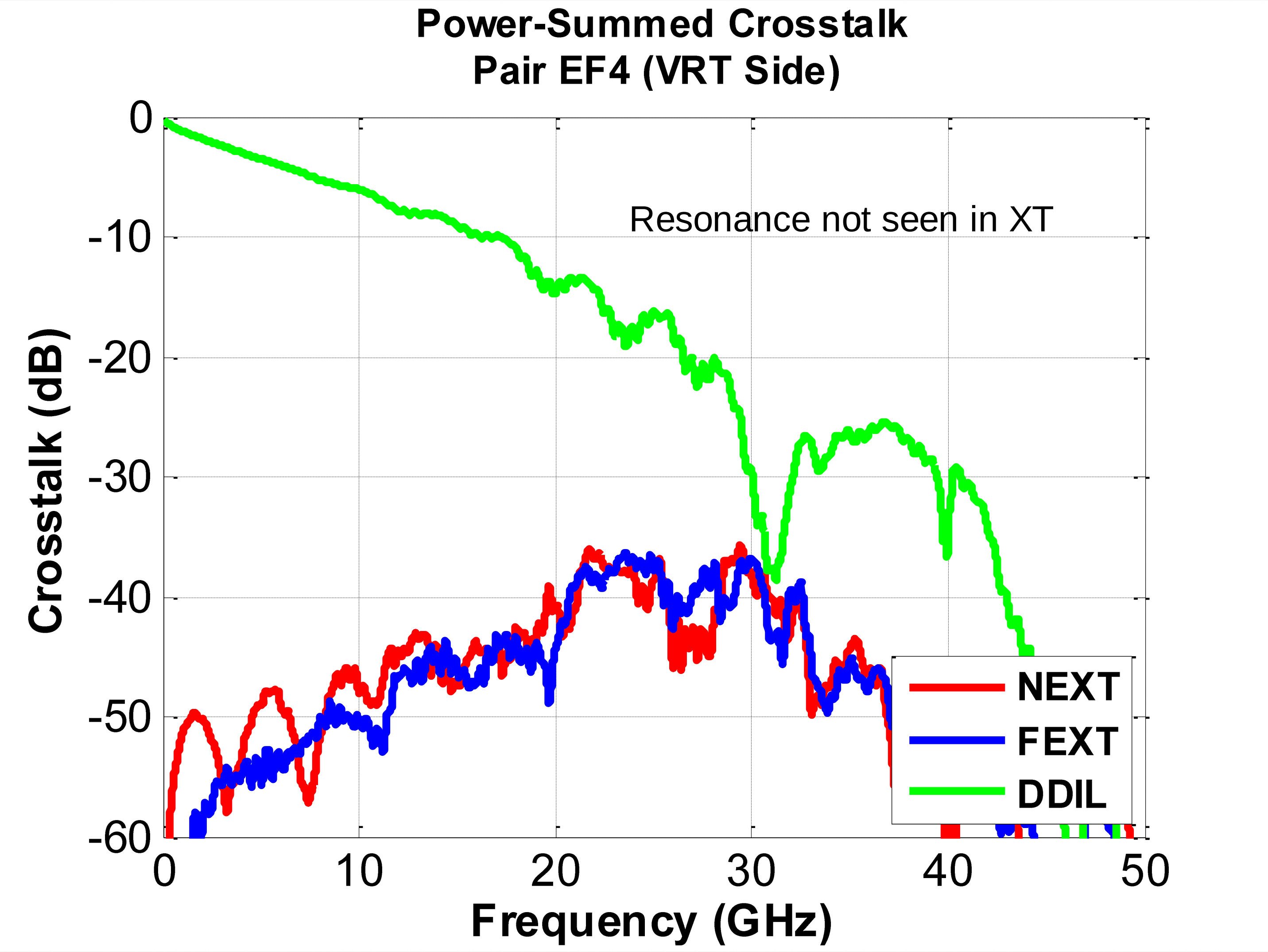
	mils	mm
trace width	6	0.1524
trace-to-trace separation	5	0.127
trace-to-antipad separation	21.4	0.5441
signal via drill Ø	17.7	0.45
signal via finish Ø	14	0.36
signal via pad Ø	27.7	0.70
small ground via drill Ø	12.6	0.32
small ground via finish Ø	9.4	0.24
large ground via drill Ø	23.6	0.60
large ground via finish Ø	20	0.50
antipad width	50.4	1.28
row pitch		1.20
column pitch		2.80

Beyond 25 Gb/s



	mils	mm
trace width	6	0.1524
trace-to-trace separation	5	0.127
trace-to-antipad separation	6	0.1524
signal & small ground via drill Ø	17.7	0.45
signal & small ground via finish Ø	14	0.36
signal via pad Ø	27.7	0.70
large ground via drill Ø	23.6	0.60
large ground via finish Ø	20	0.50
antipad width	50.4	1.28
row pitch		1.20
column pitch		2.80

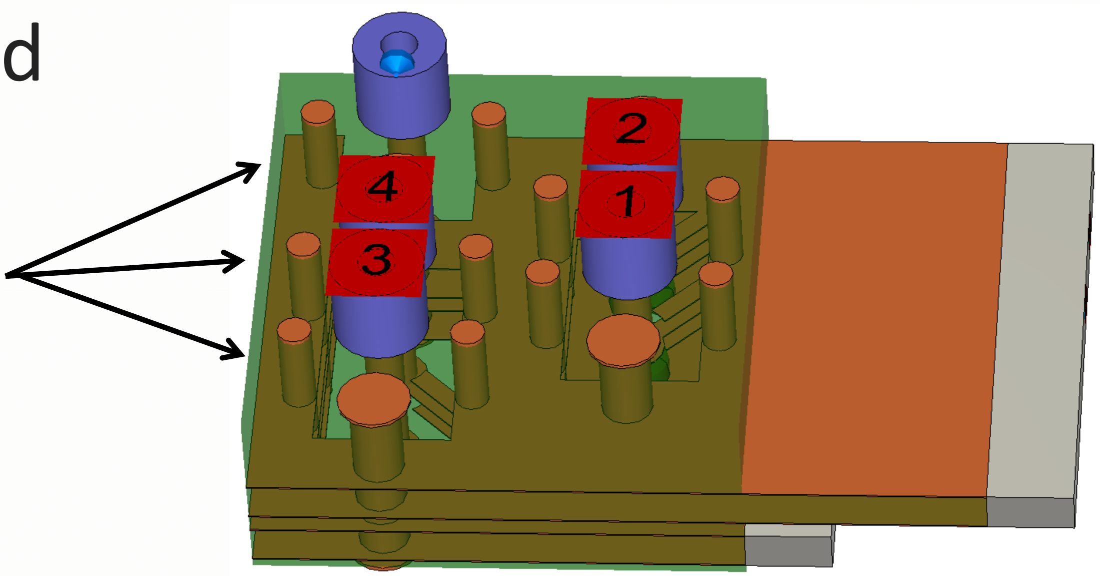
Resonance Reappeared



Cause of New Resonance

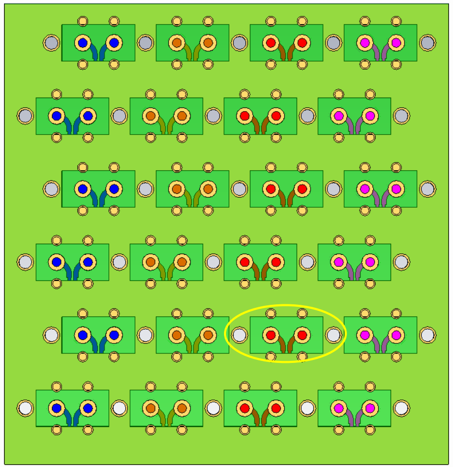
- There was not a ground layer on the top of the new daughter cards.
- All of the ground vias formed little stubs.
- Fixed by conductive paint on the surface of the board

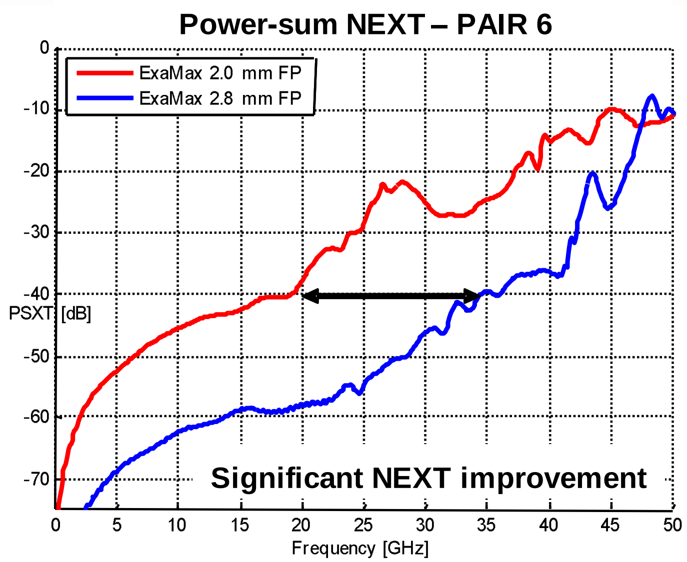
Little ground stubs

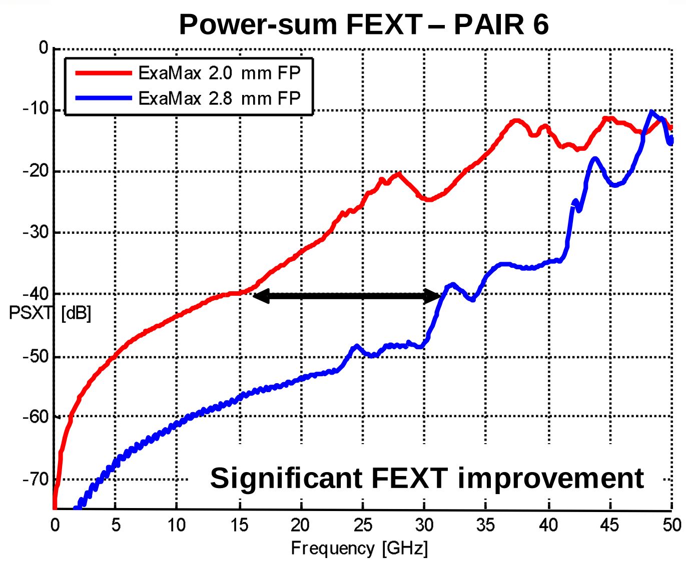


Beyond 25 Gb/s (40 Gb/s)

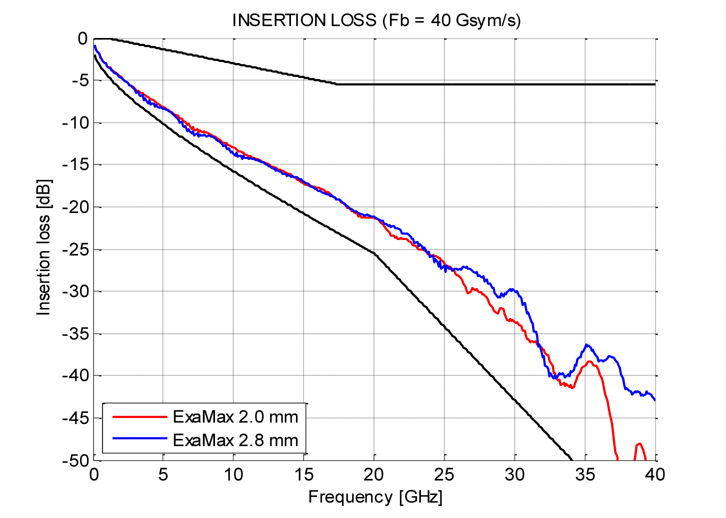
Simulation of footprint with larger column pitch

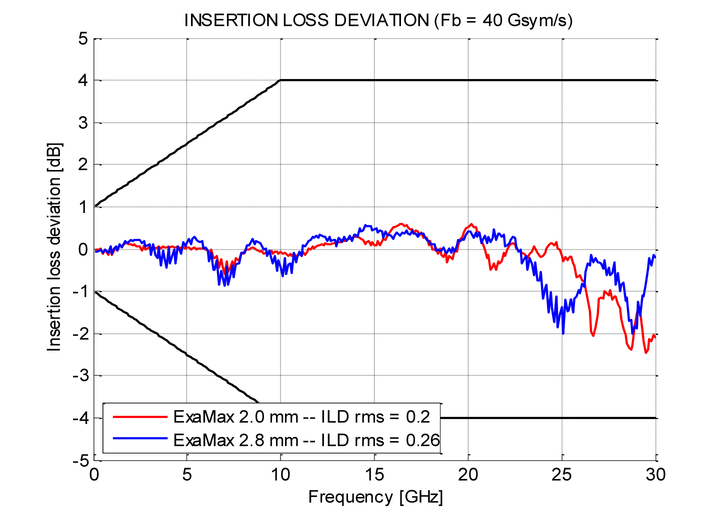


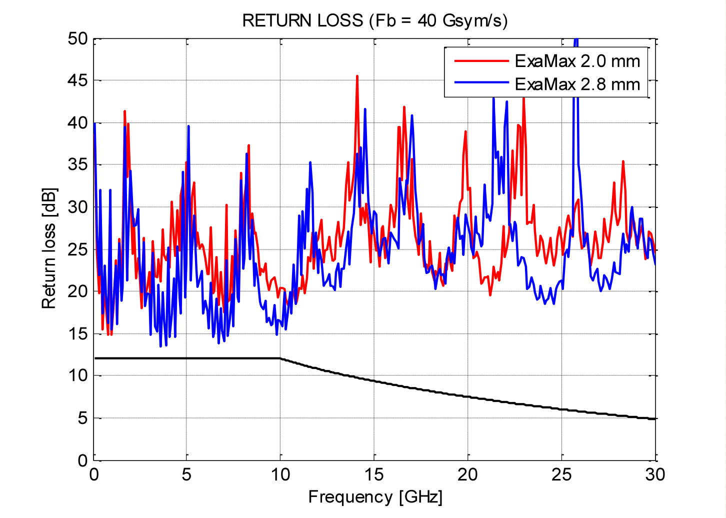


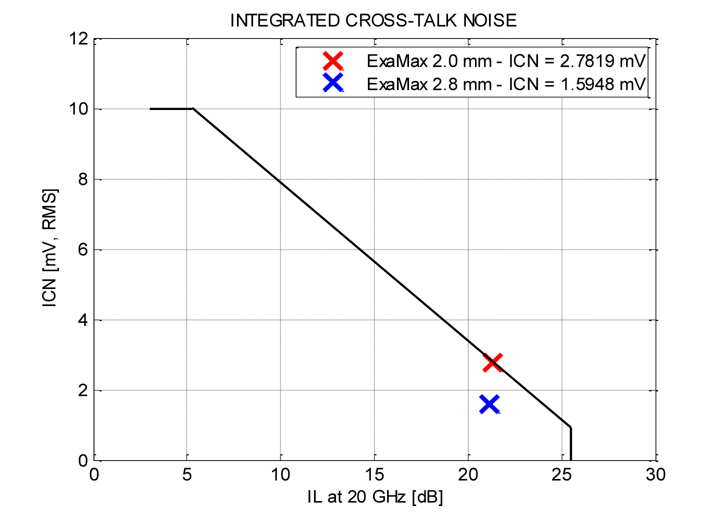


Beyond 25 Gb/s (40 Gb/s)









Conclusions / Summary

- To build a channel that works at 25+ Gb/s:
  - Use an appropriate connector that has…
    - Excellent Z_0, R.L., I.L., crosstalk, and mode conversion
    - Zero skew
    - Absence of resonance
  - Design a connector footprint that has…
    - Features to reduce ground starvation
    - Zero skew routing
    - Adequate separation between trace and antipad edges
    - Smaller antipads for ground layers that are backdrilled away

Conclusions / Summary (cont.)

- To build a channel that works at 25+ Gb/s:
  - Design a backplane that…
    - Implements the aforementioned connector footprint features
    - Meets the required loss characteristics
    - Prevents magnetic coupling between differential traces on adjacent signal layers
  - Avoid having stubs in both connector and all boards

References

- D. M. Pozar, Microwave Engineering, 2nd ed., John Wiley & Sons, Inc.,1998, pp. 154-167.
- S. Sercu and L. Martens, "Accurate de-embedding of the contribution of the test boards to the high-frequency characteristics of backplane connector," Proc. of the 6th Topical Meeting on Electrical Performance of Electronic Packages, San Jose, Ca. October 27-29, 1997, pp. 177-180.
- S. Sercu and L. Martens, "Characterizing N-port packages and interconnections with a 2-port network analyzer," Proceedings of the 6th Topical Meeting on Electrical Performance of Electronic Packages, San Jose, CA., October 27-29, 1997, pp. 163-166.
- S. Sercu and L. Martens, "N-port characterisation techniques with applications to multi-port connectors an IC-packages,".28th EuMC Workshop Proceedings, 1st EuMW Amsterdam, October 9, 1998, pp. 202-216.
- OIF Common Electrical Interface 25 Gb/s Long Reach (CEI-25G-LR) Specification, First Edition, Optical Internetworking Forum, 2011.
- CEI/IEC 1076-4-101 Hard Metric Specification, First Edition, International Electrotechnical Committee, 1995-2005.
- H. Johnson and M. Graham, High-Speed Digital Design (A Handbook of Black Magic), Prentice Hall PTR, 1993, pp. 295-98.
- V. Balasubramanian, S. Smith, and S. Agili, "Comparison of S-Parameter Concatenation to Full-Wave Simulation for High-Speed Interconnect Analysis," Proceedings of DesignCon 2007, San Jose, CA, January 29 – February 1, 2007.