SIGNAL INTEGRITY:PCB & INTERCONNECT TEST
“FOCUS ON DEEMBEDDING”

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ROHDE&SCHWARZ
Make ideas real

SYLLABUS

PART 1: PCB AND INTERCONNECT TEST CHALLENGES

- CHANNEL IMPAIRMENTS
- SURVEY OF BANDWIDTH REQUIREMENTS

PART 2: DEEMBEDDING - HIGH-SPEED DIGITAL AND RF APPLICATIONS

- BRIEF OVERVIEW OF SCATTERING PARAMETERS
- DEEMBEDDING TYPES

PART 3: DEEMBEDDING: COMMON USE CASES

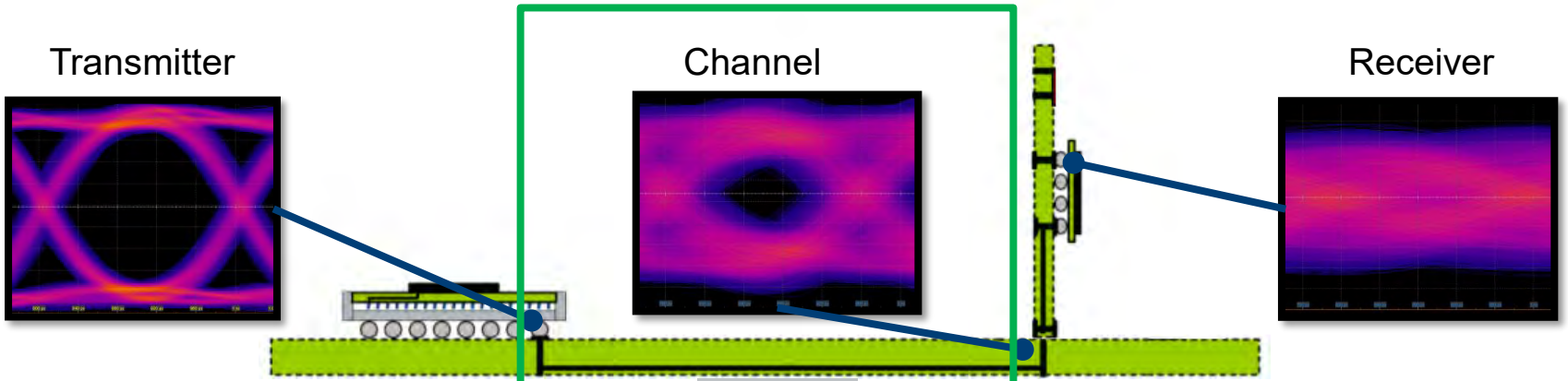
- FIVE TYPES OF DEEMBEDDING
- EZD (EAZY DEEMBEDDING) - (K210) IMPLEMENTATION AND RESULTS

PART 4: PCB AND INTERCONNECT: SIGNAL INTEGRITY TESTS

- MODEL CHANNEL IMPAIRMENT WITH CORRECTED DATA
- SUMMARY & CONCLUSION

PART1 - PCB AND INTERCONNECT TEST CHALLENGES

HIGH-SPEED DIGITAL DESIGN: TX – CHANNEL – RX



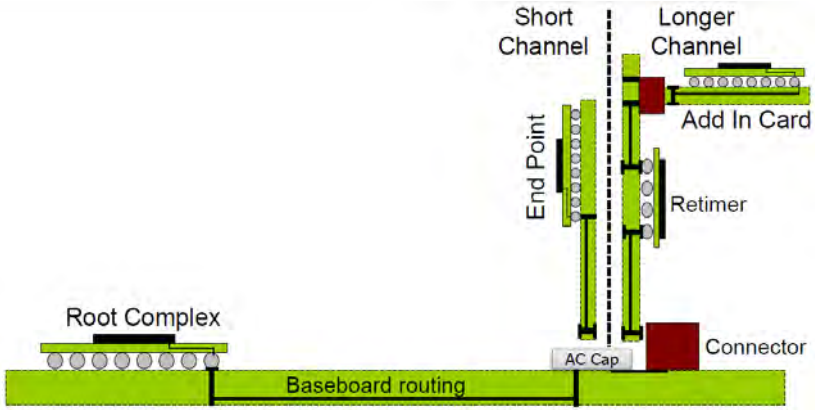
Measurements:

- Return Loss, Insertion Loss
- Mode Conversion, Skew
- Crosstalk
- Impedance over time
- Eye Diagram

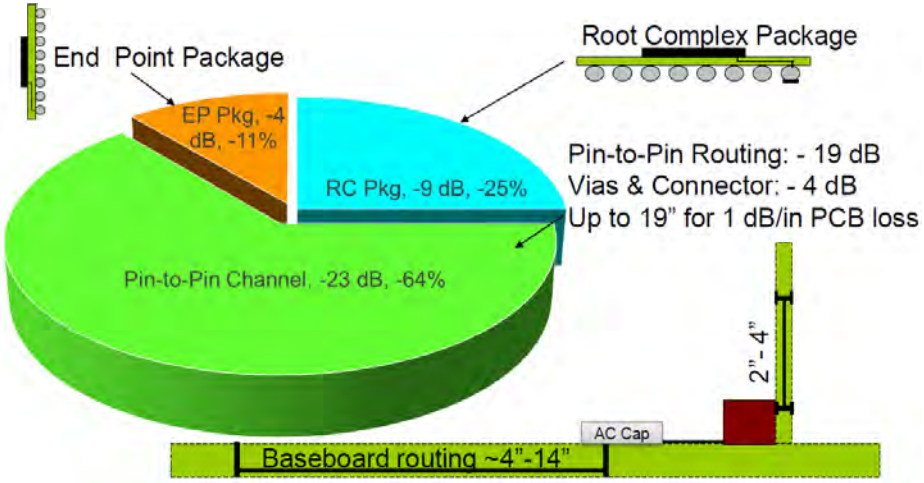
CHALLENGES FOR PCBS AND INTERCONNECTS IN HIGH-SPEED DIGITAL DESIGNS

- impedance mismatches - discontinuities at packages, vias, connectors

Example: PCIe 5.0
discontinuities on signal path
between Root Complex and End Point



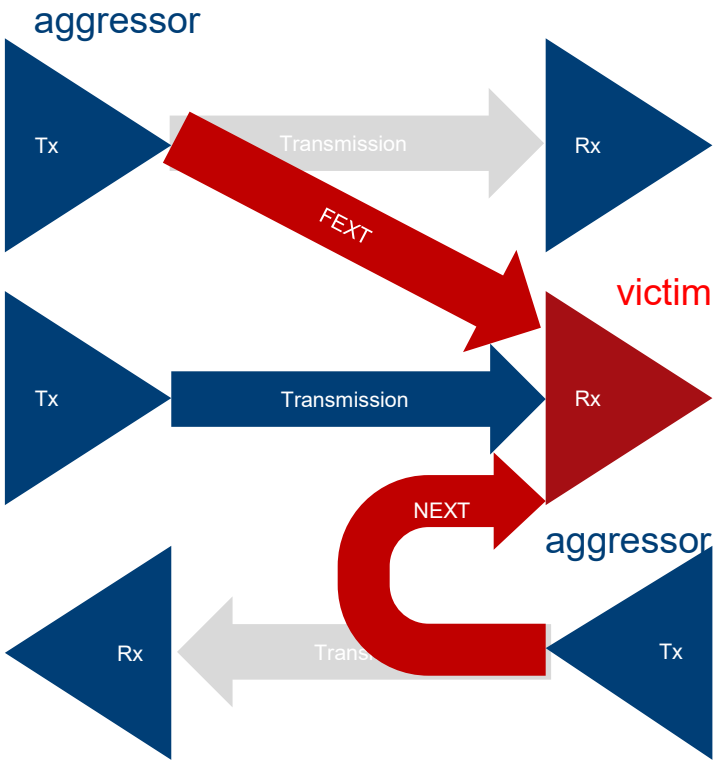
Example: PCIe 5.0
total loss budget: 36 dB @ 16GHz



Source: PCI-SIG Developers Conference 2019; PCIe®5.0 Electrical Update

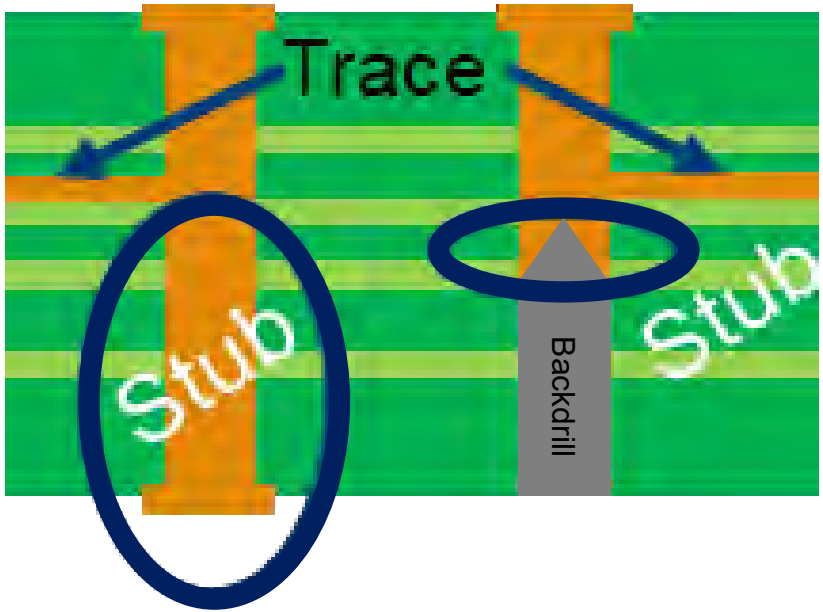
CHALLENGES FOR PCBS AND INTERCONNECTS IN HIGH-SPEED DIGITAL DESIGNS

- impedance mismatches - discontinuities at packages, vias, connectors, interposers
- losses and frequency response of PCB material
  - for 112 Gbps and above: PCB signal traces will be by-passed by cables
- crosstalk: NEXT, FEXT



CHALLENGES FOR PCBS AND INTERCONNECTS IN HIGH-SPEED DIGITAL DESIGNS

- Physical Structures
  - impedance mismatches - discontinuities at packages, VIA's, connectors
  - losses and frequency response of PCB material
  - crosstalk: NEXT, FEXT
  - multiple resonant structures, e.g. via stubs (backdrill), fiber weave effects, etc.
  - Manufacturing Issues



HIGH-SPEED DIGITAL DESIGN: PCIE
NETWORK INFRASTRUCTURE, DATA CENTERS, …

PCIe Spec.	Raw Bandwidth (per Lane)	Data Rate (Total)	NRZ / PAM	VNA BW requirement SOC test	VNA BW requirement (PCBs, Interconnects)
…					
Gen 3	8.0Gbps	8.0GT/s	NRZ		
Gen 4	16.0Gbps	16.0GT/s	NRZ	25GHz	20GHz (system performance)
Gen 5	32.0Gbps	32.0GT/s	NRZ	50GHz	40GHz (system performance)
Gen 6	64.0Gbps	64.0GT/s	PAM4	50GHz (spec. in progress)	40GHz (spec. in progress)

Note:

- GT/s = Gtransfers / sec
- Gbps = Gbit / sec

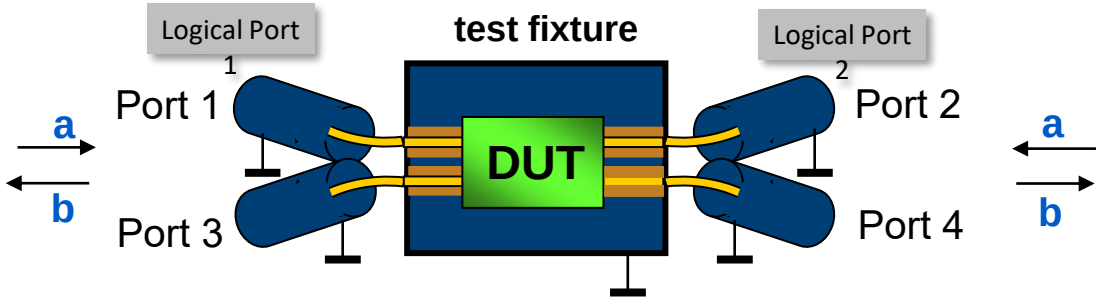
HIGH-SPEED DIGITAL DESIGN: IEEE802.3
NETWORK INFRASTRUCTURE, DATA CENTERS, …

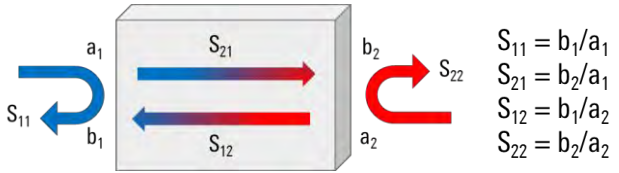
IEEE Spec.	Copper Cables	Backplanes	Signalling Bandwidth (per Lane)	NRZ / PAM	VNA BW requirement (PCBs, Interconnects)
…	…	…	…		
802.3by 802.3bj	25GBASE-CR 100GBASE-CR4	25GBASE-KR 100GBASE-KR4	25Gbps	NRZ	25GHz
802.3cd	50GBASE-CR1 100GBASE-CR2 200GBASE-CR4	50GBASE-KR1 100GBASE-KR2 200GBASE-KR4	50Gbps	PAM4	26.56GHz
802.3ck	100GBASE-CR1 200GBASE-CR2 400GBASE-CR4	100GBASE-KR1 200GBASE-KR2 400GBASE-KR4	100Gbps	PAM4	50GHz (spec. in progress)

PART 2: DEEMBEDDING:
HIGH-SPEED DIGITAL AND RF APPLCATIONS

TYPICAL PCB MEASUREMENTS IN DIGITAL SYSTEMS
S-PARAMETER BASICS

Principle:
1.) The VNA measures a differential 2-port device as single-ended 4-port device

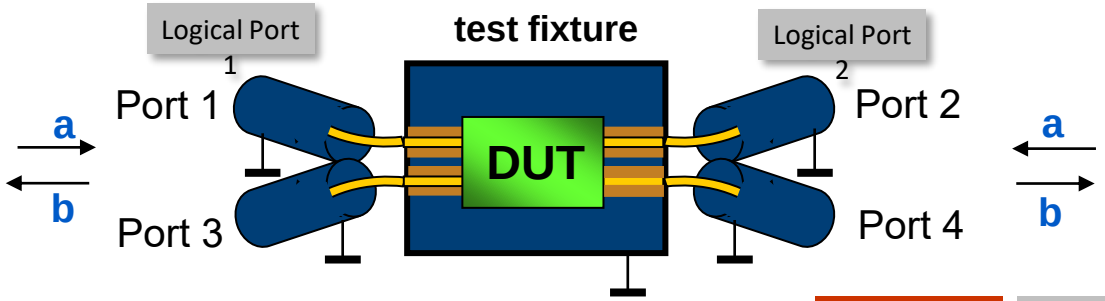


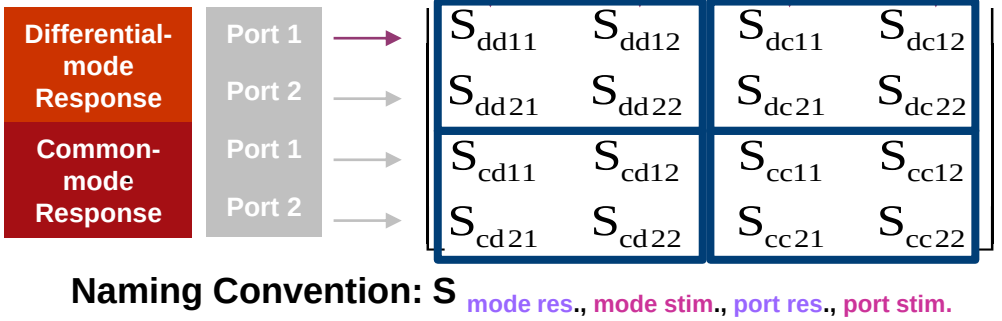


$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}$$

TYPICAL PCB MEASUREMENTS IN DIGITAL SYSTEMS
S-PARAMETER BASICS

Principle:
2.) The VNA calculates mixed mode S-Parameters out of measured single ended S-Parameters

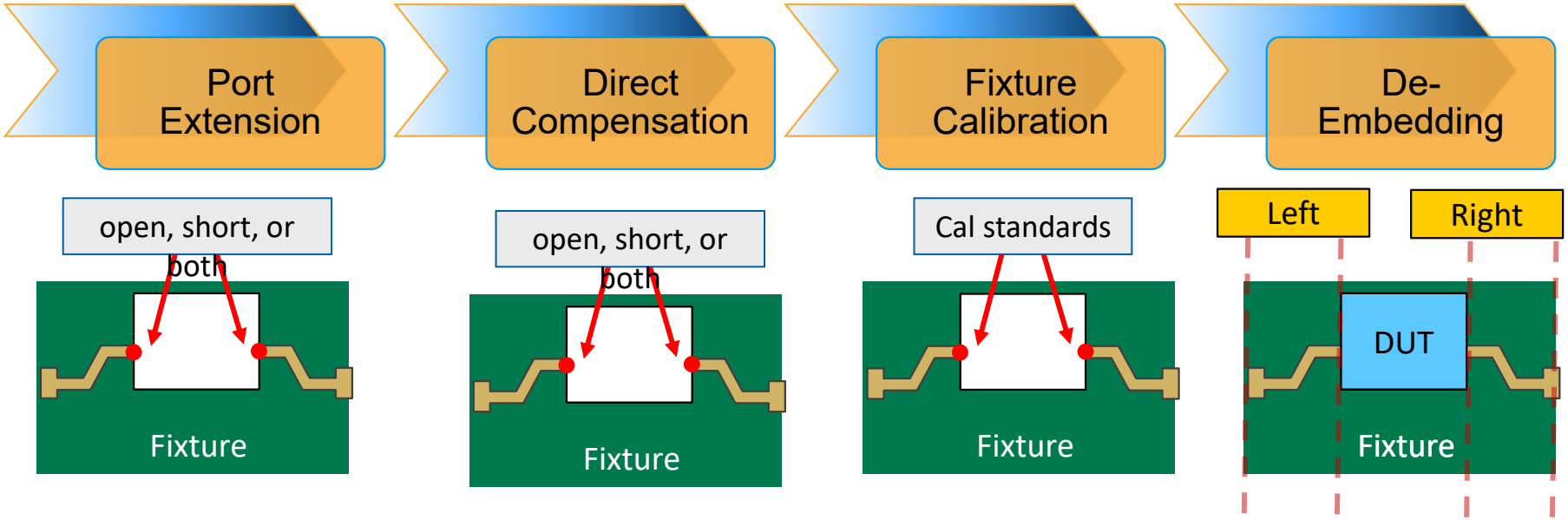




Naming Convention: S mode res., mode stim., port res., port stim.

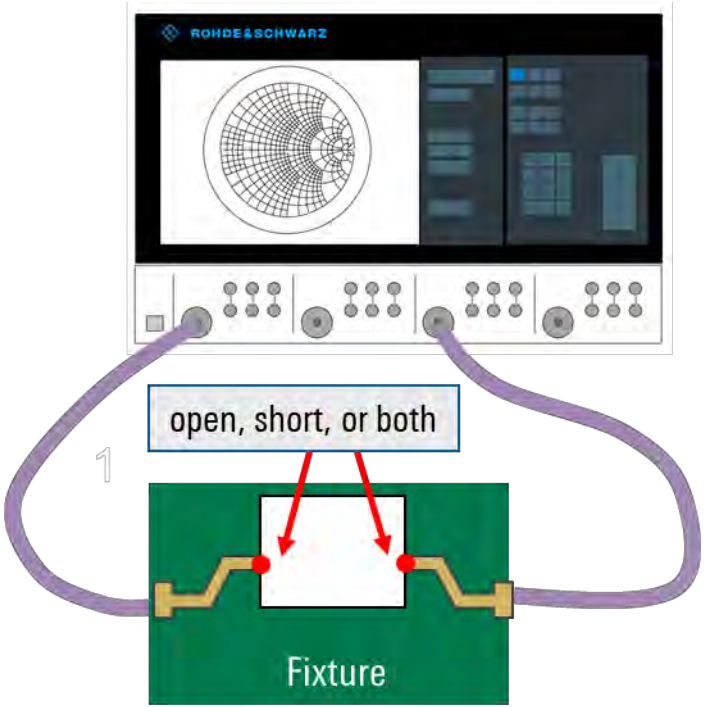
EXPLORE DE-EMBEDDING

FOUR TIERS OF DE-EMBEDDING



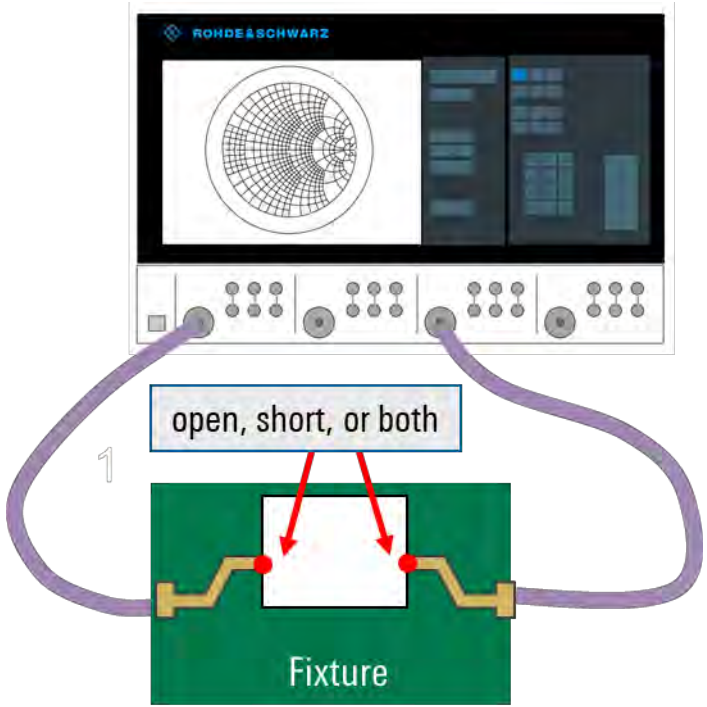
PORT EXTENSION (PORT OFFSET)

- Assume text fixture is perfectly matched and behaves like a ideal transmission line
  - Defined delay
  - Defined loss
- Delay and loss can be
  - Manually entered by the user
  - Automatically determined
- Standard feature on most VNAs
- Easy configuration, but limited accuracy
  - Real world effects such as reflections, crosstalk, etc. are not well represented



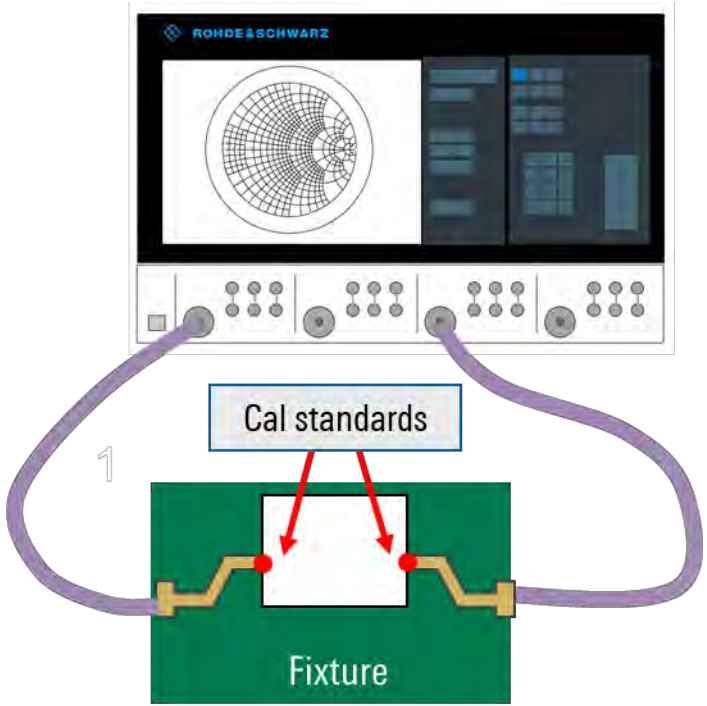
DIRECT COMPENSATION

- Doesn’t assume that the fixture behaves like ideal transmission line
- Measures **frequency dependent** transmission characteristics of fixture
  - Fixture terminated with open, short, or both
  - Best results when open and short are used
- Like port extension, only works well at lower frequencies (several GHz and below)
- Enforces Passivity
- Displays a “DOT” on Smith Chart



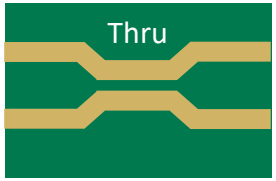
FIXTURE CALIBRATION

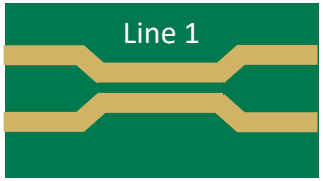
- Directly characterize the fixture
- Full calibration at DUT connection point
  - Moves the calibration plane to the DUT
  - “Calibrate out” the fixture
- More accurate solution
- Requires characterized calibration standards
  - Usually quite difficult to implement

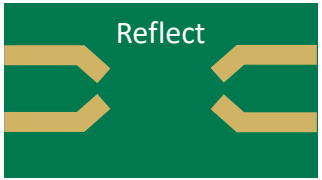


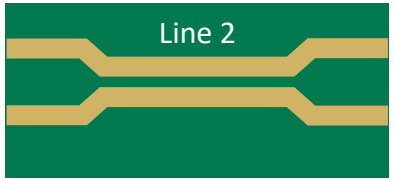
TRL (THROUGH, REFLECT, LINE)

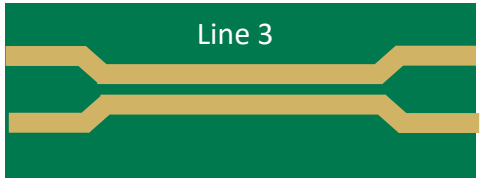
- Directly characterize the fixture
- Full calibration at DUT connection point
  - Moves the calibration plane to the DUT
  - “Calibrate out” the fixture
- More accurate solution
- Requires characterized calibration standards
  - Challenging to implement well





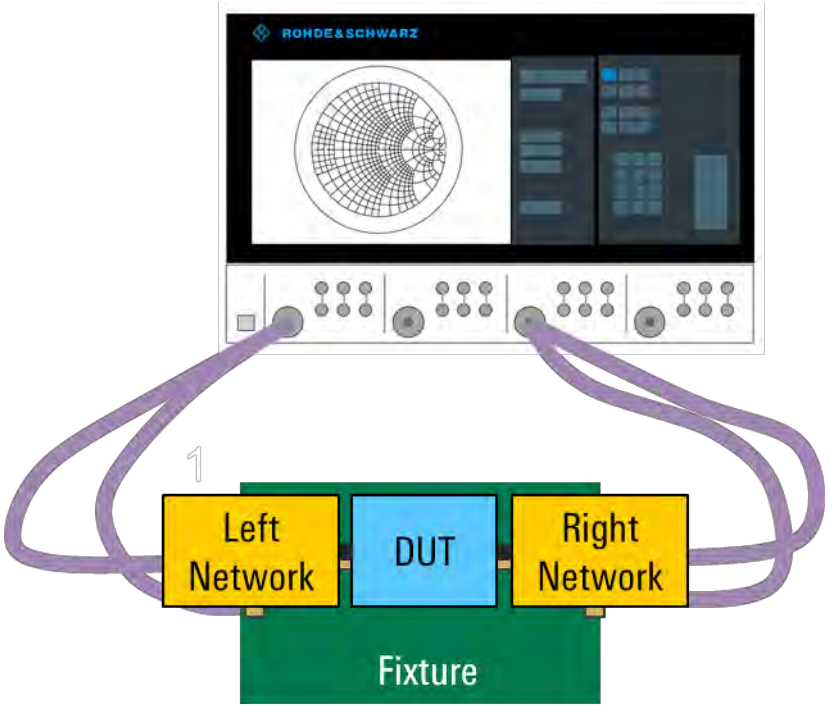






ALGORITHMIC BASED DE-EMBEDDING

- Directly characterize the fixture
- Full calibration at DUT connection point
  - Moves the calibration plane to the DUT
  - “Calibrate out” the fixture
- More accurate solution
- Requires defined calibration standard
  - Less difficult to implement



PART 3: DEEMBEDDING: COMMON USE CASES

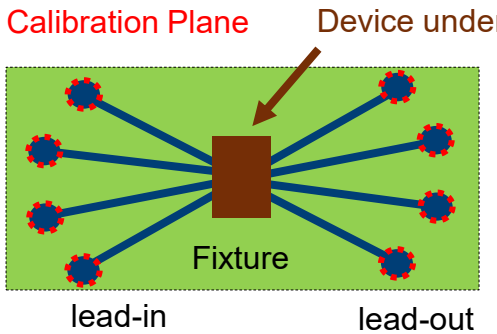
USE CASE #1: RF DEVICES WITHOUT COAXIAL CONNECTORS CHARACTERIZATION + MEASUREMENT WITH VNA

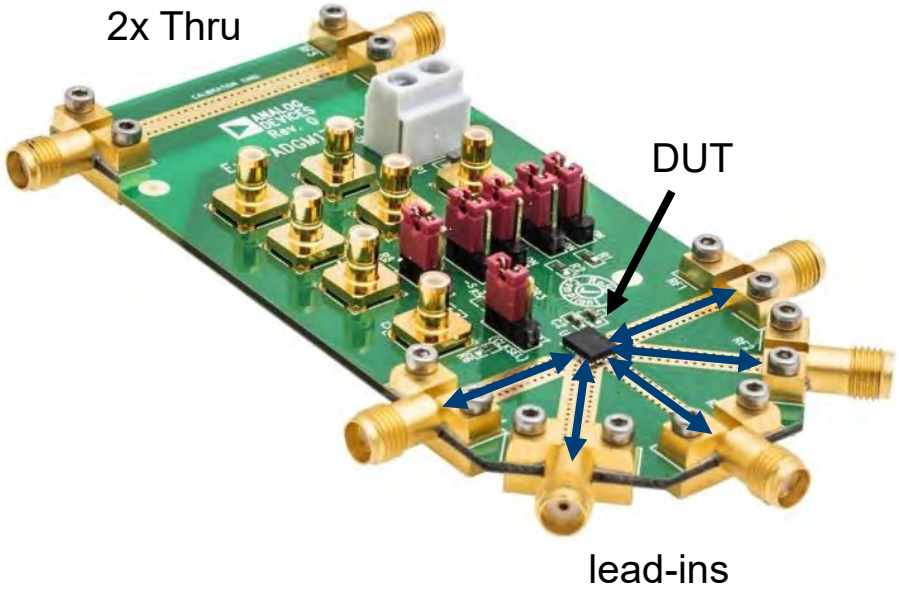
Lead-in / lead-out characterization with VNA:

step 1: calibration with coaxial standards
(→ calibration plane)

step 2: characterization and deembedding
of lead-in and lead-out
(→ reference plane at DUT)

all VNA measurements at new reference plane





USE CASE #2: SOC INTERFACE TEST W. DEEMBEDDING CHARACTERIZATION WITH VNA, MEASUREMENT WITH SCOPE

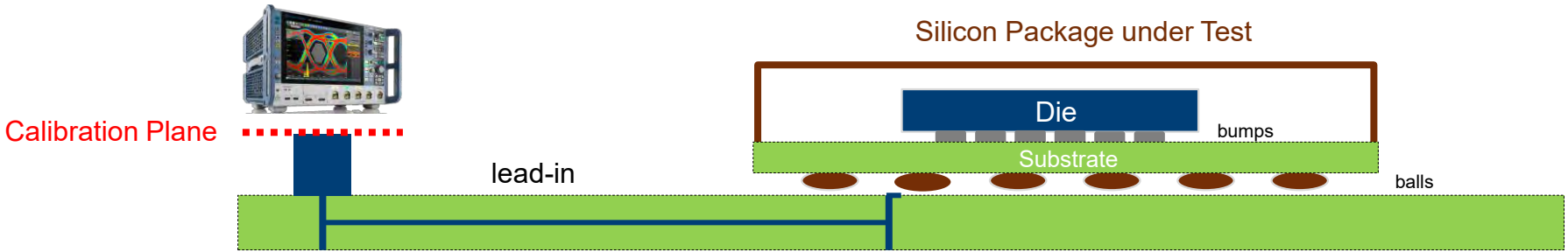
Lead-in / lead-out characterization with VNA:

step 1: calibration with coaxial standards
(→ calibration plane)

step 2: characterization of lead-in and extrapolation to DC

step 3: import to oscilloscope for deembedding
(→ reference plane at ball)

all scope measurements at new measurement plane (ball of SoC: System on Chip)



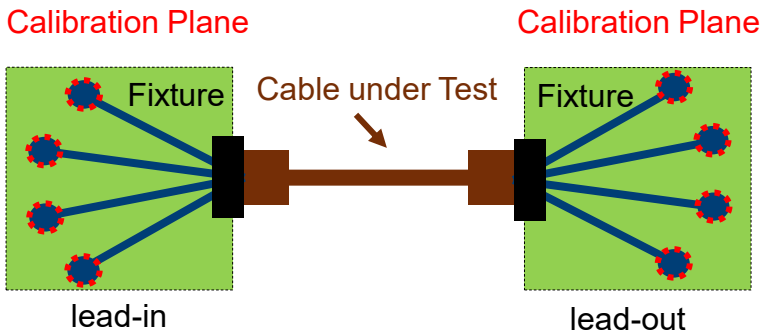
USE CASE #3: CABLE TEST WITH DEEMBEDDING CHARACTERIZATION + MEASUREMENT WITH VNA

Lead-in / lead-out characterization with VNA:

step 1: calibration with coaxial standards
(→ calibration plane)

step 2: characterization and deembedding
of lead-in and lead-out
(→ reference plane at cable)

all VNA measurements at new reference plane



USE CASE #4: PCB TEST WITH DEEMBEDDING CHARACTERIZATION + MEASUREMENT WITH VNA

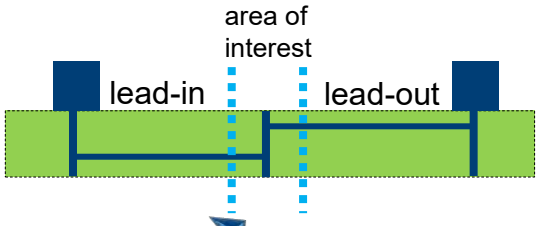
Lead-in / lead-out characterization with VNA:

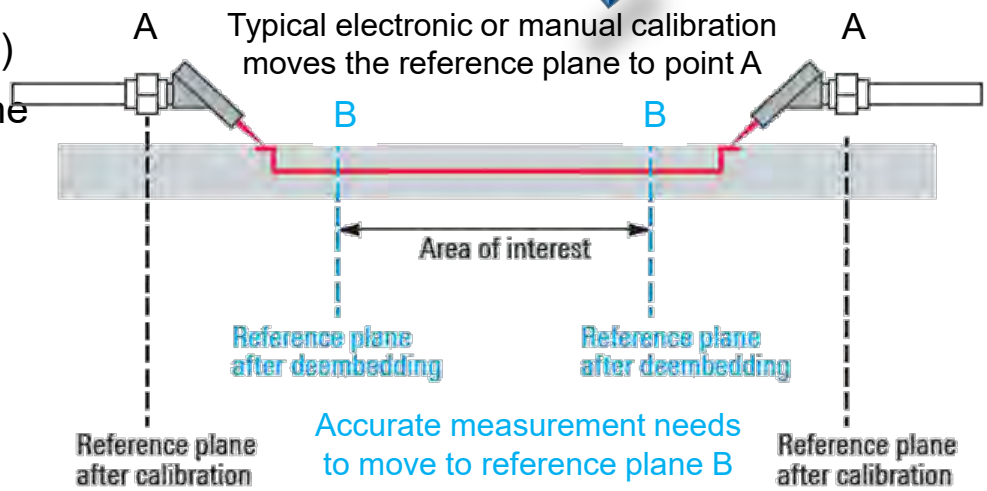
step 1: calibration with coaxial standards
(→ calibration plane)

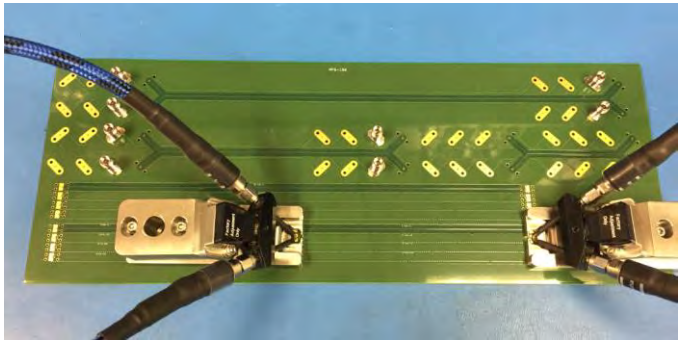
step 2: characterization and deembedding
of lead-in and lead-out
(→ reference plane at area of interest)

all VNA measurements at new reference plane

automatic calibration unit
e.g. R&S ZN-Z54







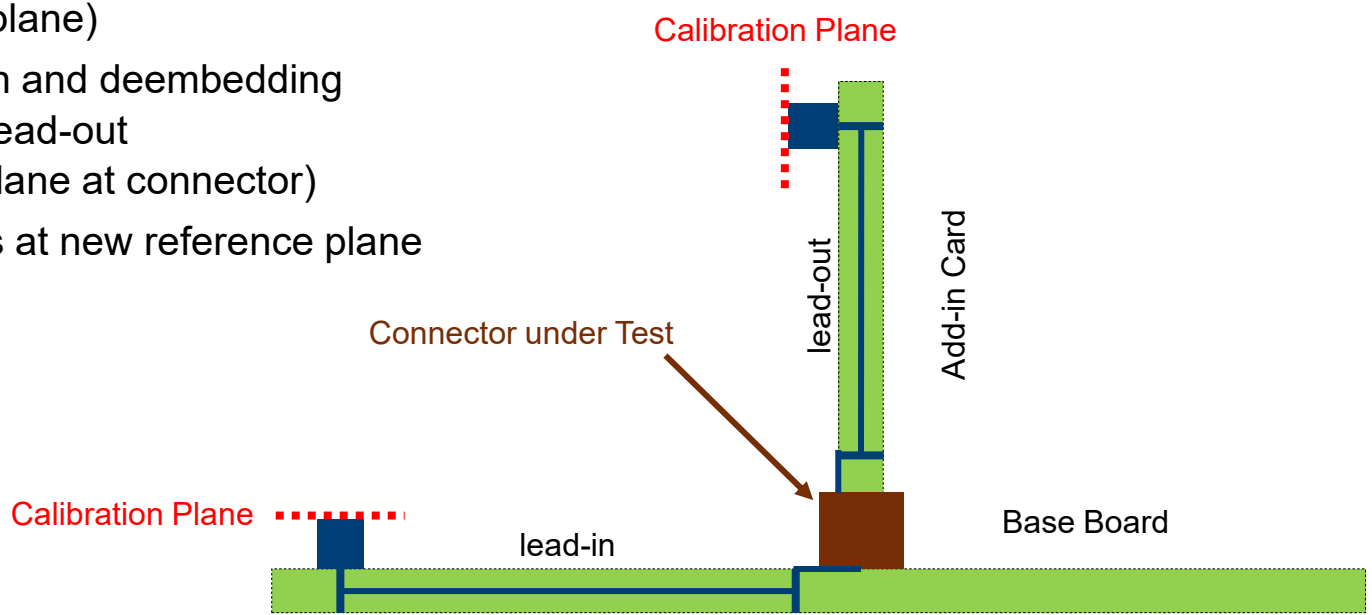
USE CASE #5: CONNECTOR TEST WITH DEEMBEDDING CHARACTERIZATION + MEASUREMENT WITH VNA

Lead-in / lead-out characterization with VNA:

step 1: calibration with coaxial standards
(→ calibration plane)

step 2: characterization and deembedding
of lead-in and lead-out
(→ reference plane at connector)

all VNA measurements at new reference plane



DEEMBEDDING OF LEAD-IN / LEAD-OUT TRACES

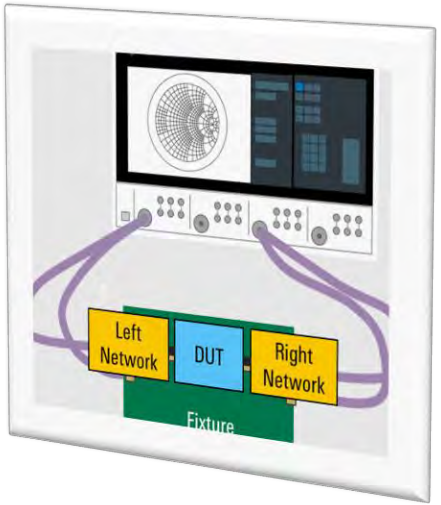
Deembedding Method Integrated into R&S ZNA / R&S ZNB:

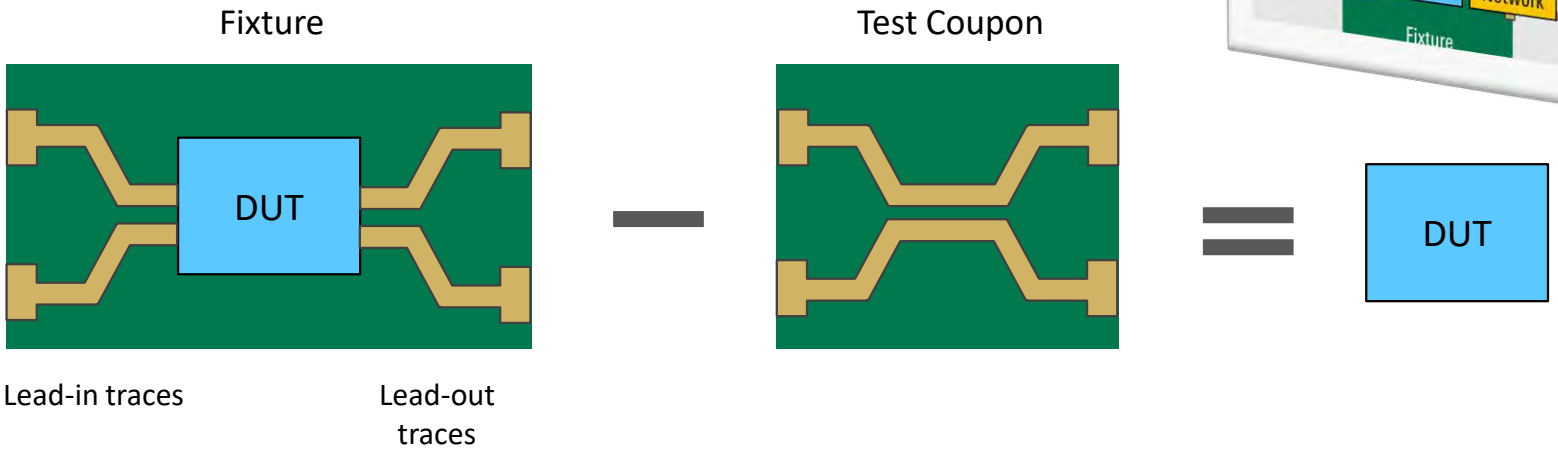
- EZD: Eazy Deembedding (ZNx-K210)

Deembedding Coupons:

- 2x Thru standard

Slide 18

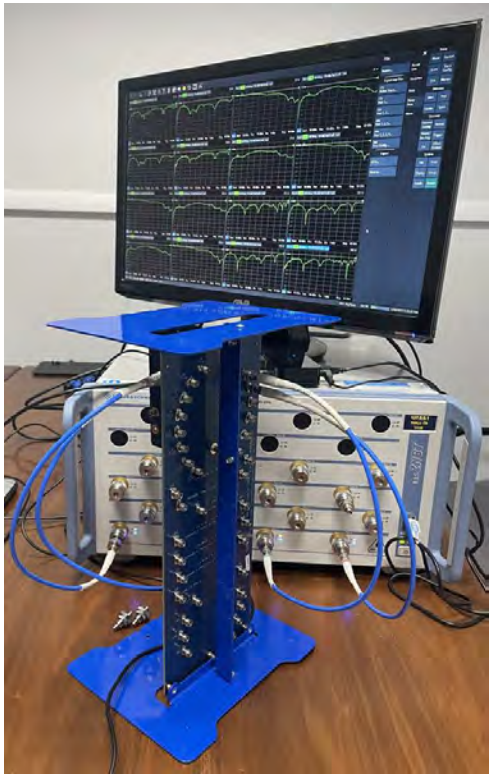




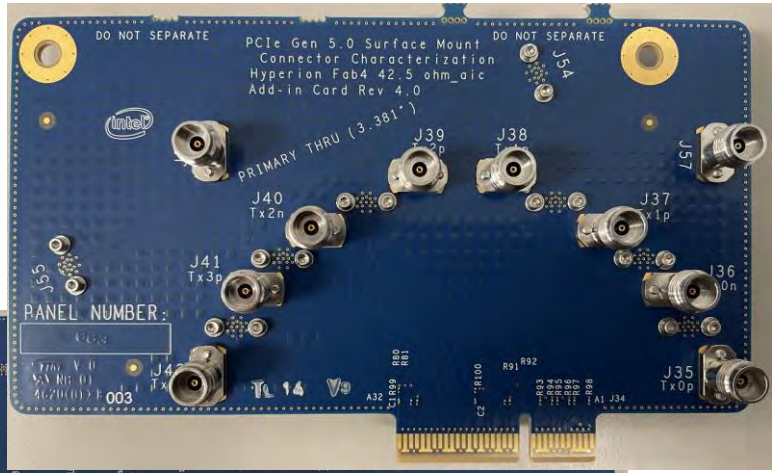
"ZNx-K210"

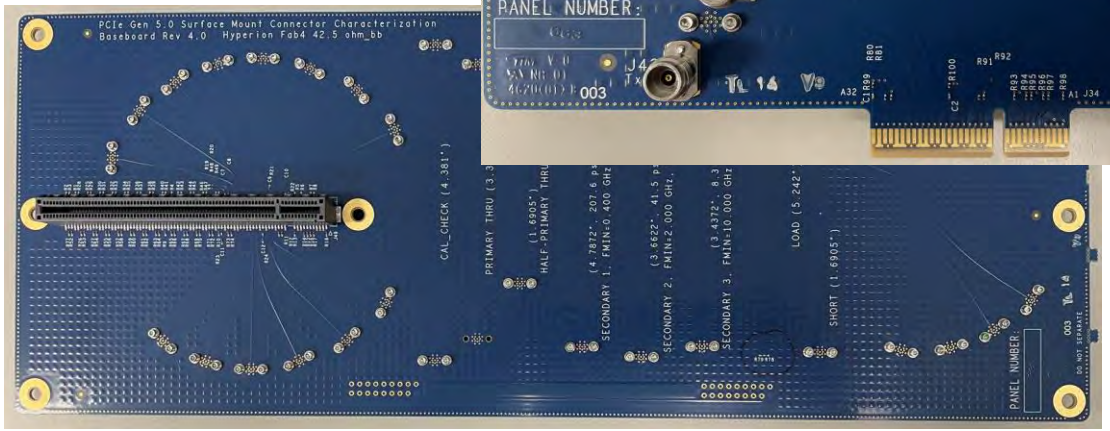
RESULTS OF EZD

MEASUREMENT OF PCIE GEN5 SMT - HYPERION BOARD



Daughter Card

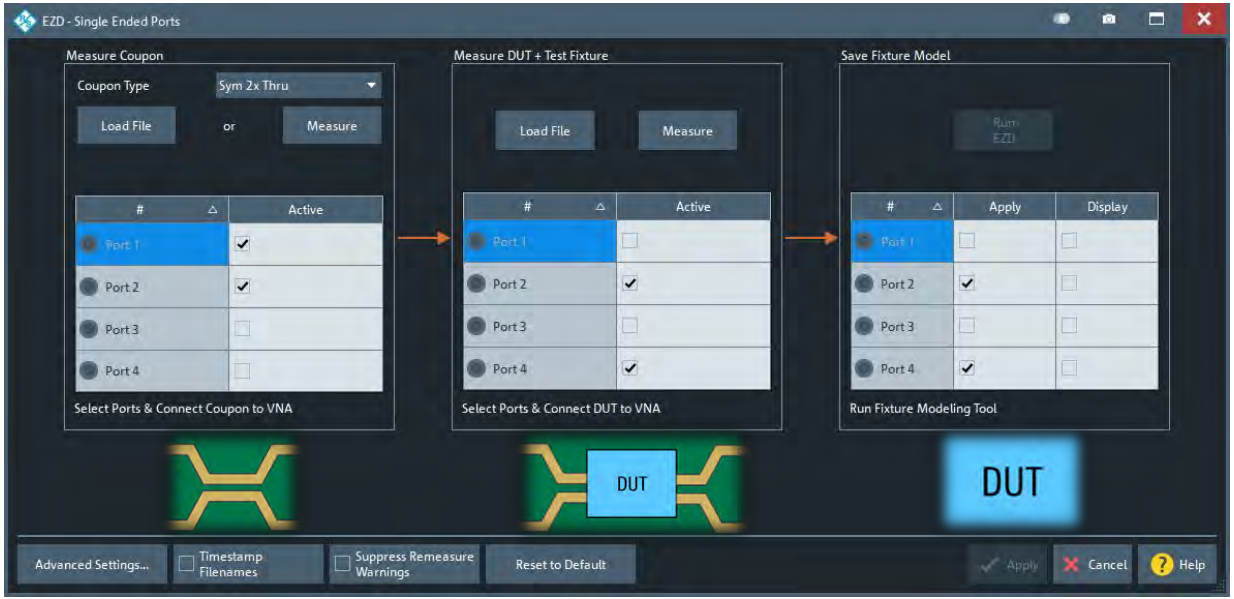




GENERAL REQUIREMENT: DEEMBEDDING OF LEAD-IN / LEAD-OUT TRACES

Implementation in R&S ZNA, R&S ZNB / ZNBT:

1: Load or measure 2 x Thru **2**: Measure DUT + Test Fixture **3**: Run Tool



BEFORE & AFTER EZD DE-EMBEDDING

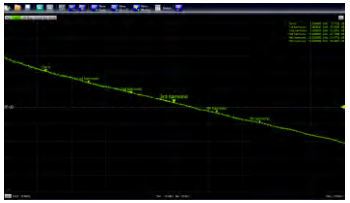
PCIe Gen5 SMT with Hyperion Board

- More than 3dB of insertion loss is recovered using the EZD tool
- Return Loss is “tamed” with the high frequency magnitude ripple mitigated.

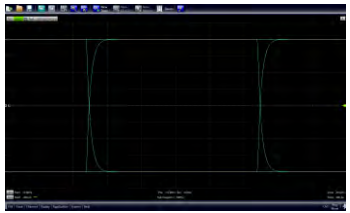
PART 4: PCB AND INTERCONNECT: SIGNAL INTEGRITY TESTS

TYPICAL PCB MEASUREMENTS IN DIGITAL SYSTEMS EXAMPLE: EYE DIAGRAM

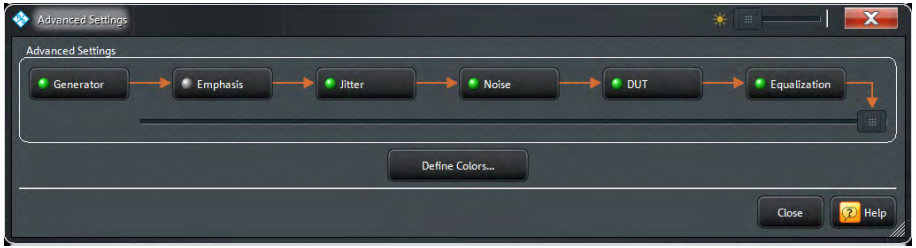
Measured DUT RF Channel



Simulated Ideal PRBS15 signal

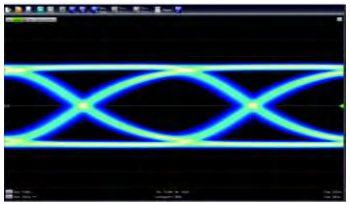


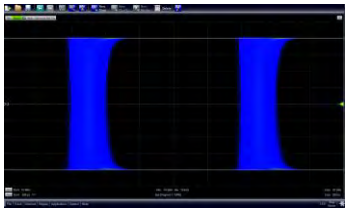
TX



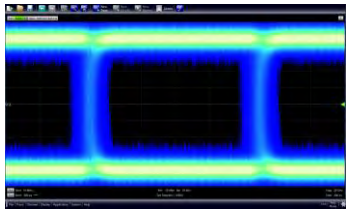
RX

Equalised Eye response

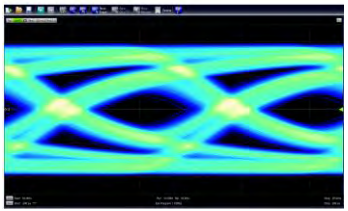




Add Jitter

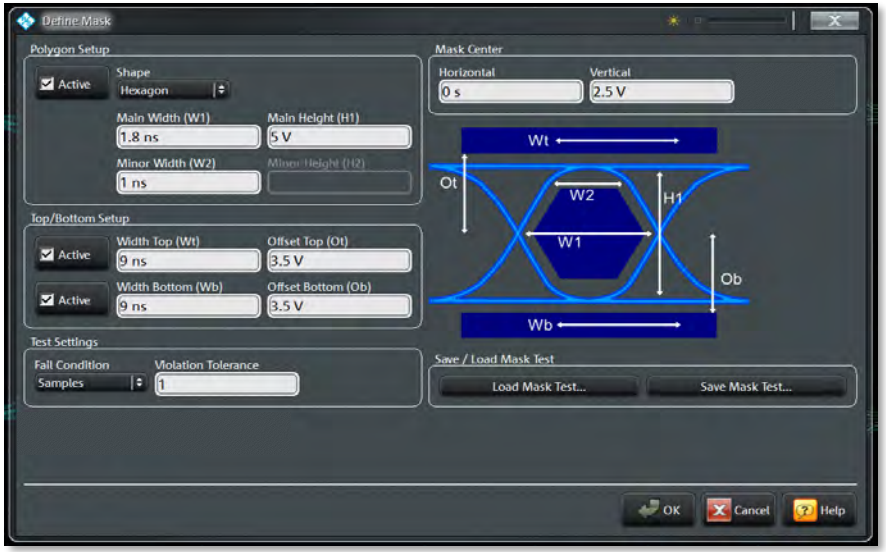


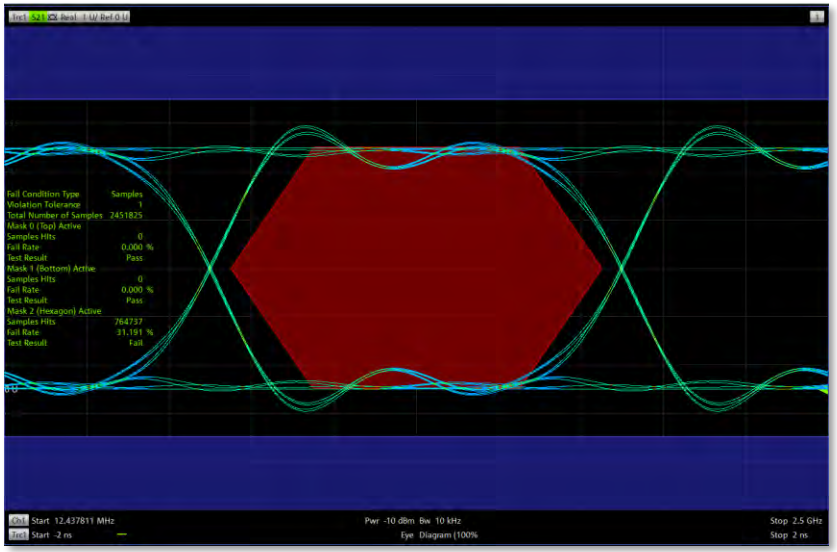
Add Amplitude Noise



Output Eye response from DUT

TYPICAL PCB MEASUREMENTS IN DIGITAL SYSTEMS
EYE DIAGRAM





Define pass/fail areas to ensure a proper eye opening

SUMMARY

Frequency Domain VNA:

- return loss, insertion loss
- mode conversion
- crosstalk: NEXT, FEXT
- derived values, e.g.: COM / ERL
  Channel Operating Margin
  Effective Return Loss
- **De-Embed Lead-In and Lead-Out Structures**
- Model Channel Impairments
  - Convolve Serial Data with Frequency Domain Data

R&S ZNA

R&S ZNB

R&S ZNBT

CONCLUSION

- A TECHNIQUE WAS DESCRIBED WHICH UTILIZES A VNA AND THE EZD (P370) UTILITY TO REMOVE OR DEEMBED THE EFFECTS OF FIXTURES UPON A DATA CHANNEL
- THIS TECHNIQUE REQUIRES ONLY A 2X THRU
- SUBSEQUENTLY, CHANNEL MODELING CAN BE EXPLORED USING TRUE DUT BEHAVIOR