A Practical Guide to Signal Integrity: From Simulation to Measurement

Keysight Technologies	2018.1.31

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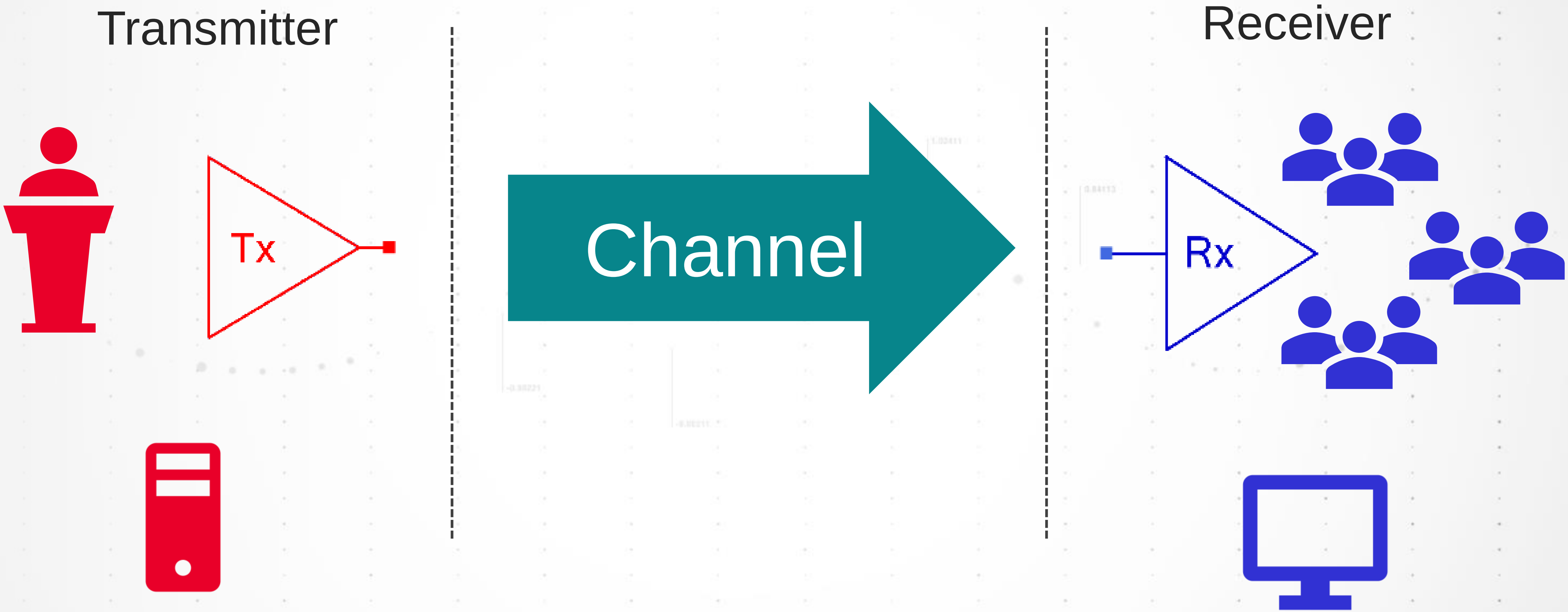
KEYSIGHT TECHNOLOGIES

Signal Integrity Is All Around Us



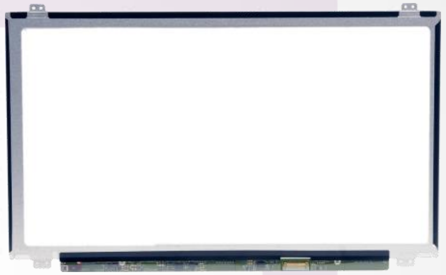
Signal Integrity in Digital Communication Channel

CPU

Graphic card

Cable

On board video processor

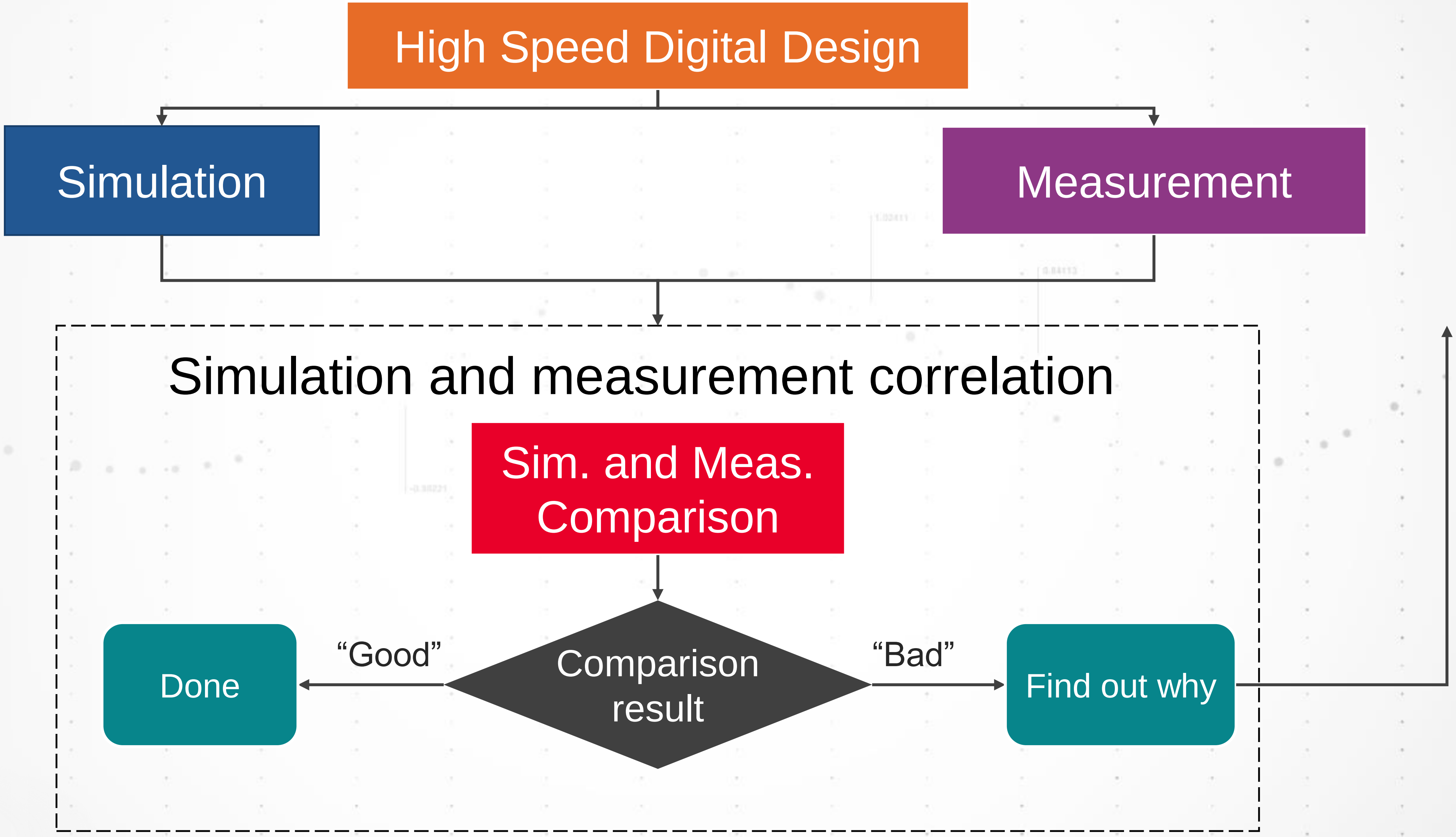


LED display

Interconnects

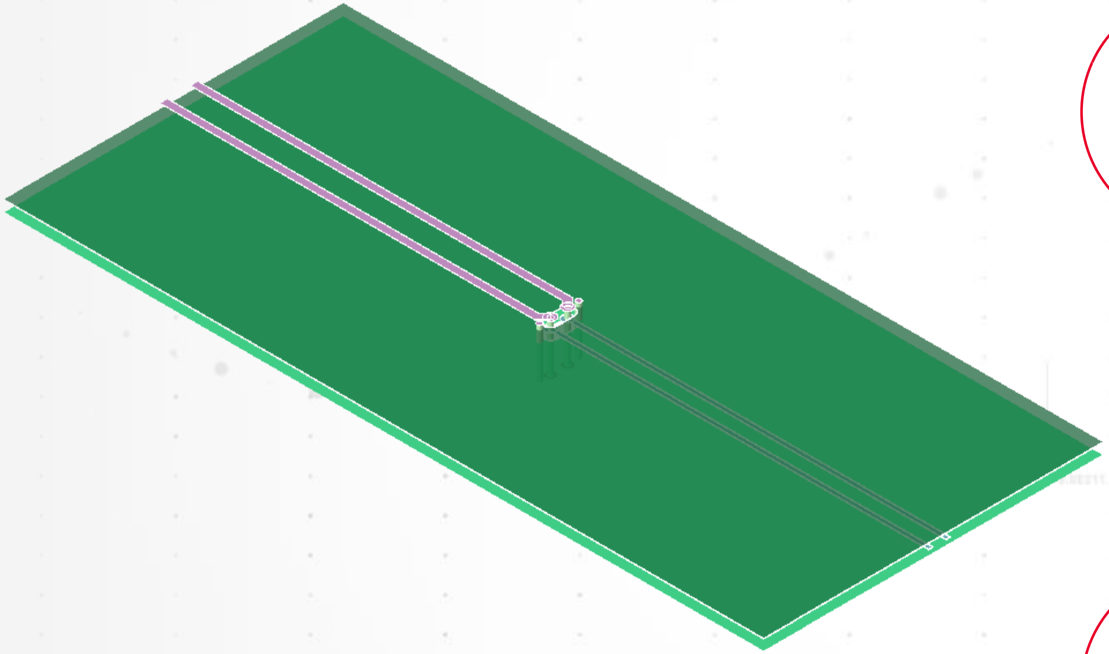
> “Signal integrity is about the problems interconnects introduce and how to avoid them.
>
> – Dr. Eric Bogatin

Guide to Signal Integrity in Simulation and Measurement



Understand Signal Integrity Analyses with a Case Study

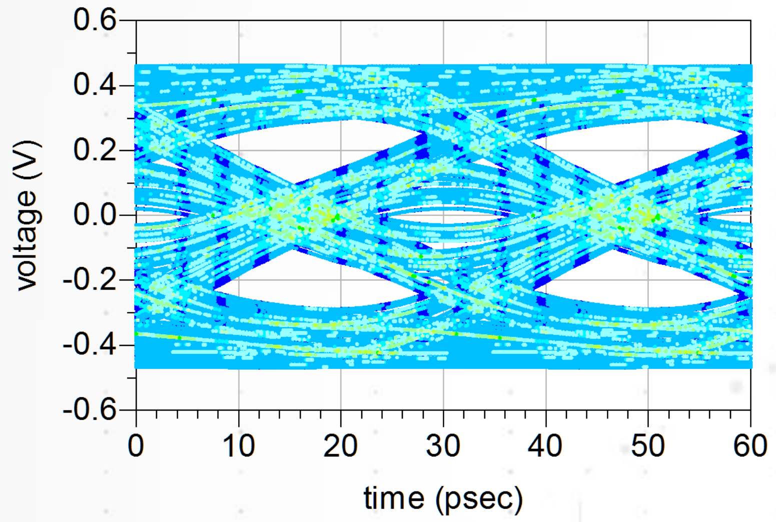
The case of the failing virtual channel



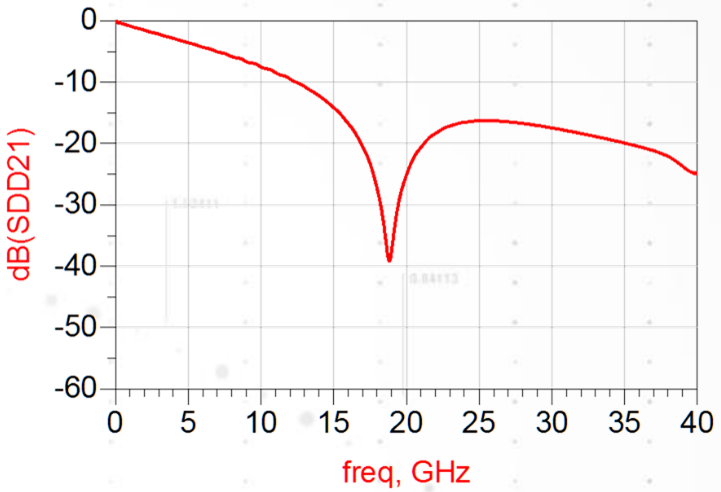
1. Simulate the channel
2. Find the root cause of degradation
3. Explore design solutions

Essential Signal Integrity Analyses in Simulation

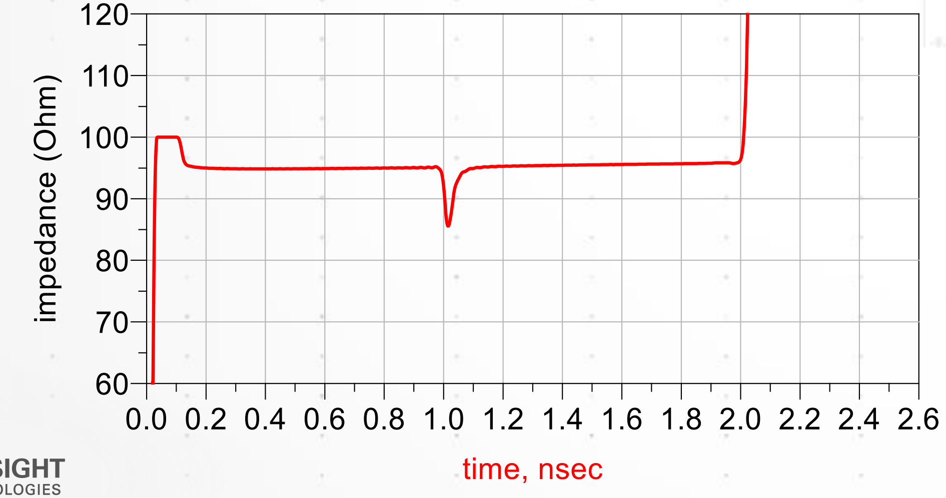
Eye diagram



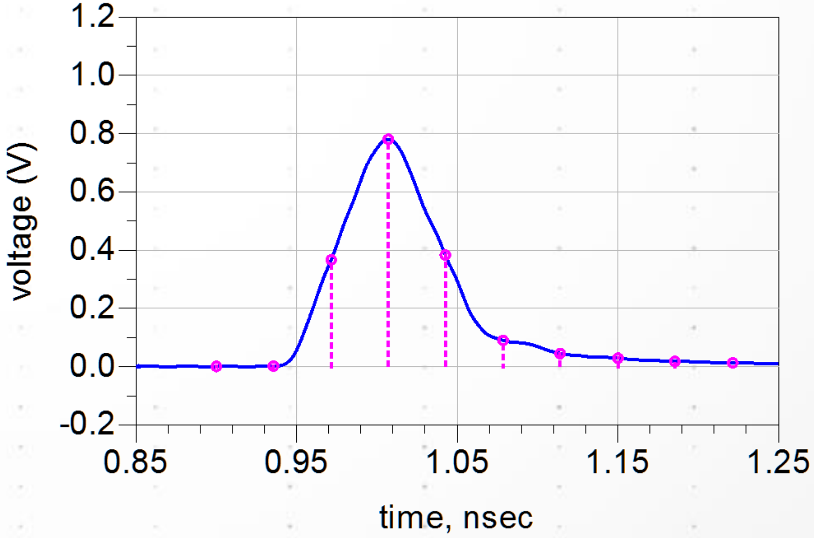
Mixed-mode S-parameters



Time domain reflectometry



Single pulse response



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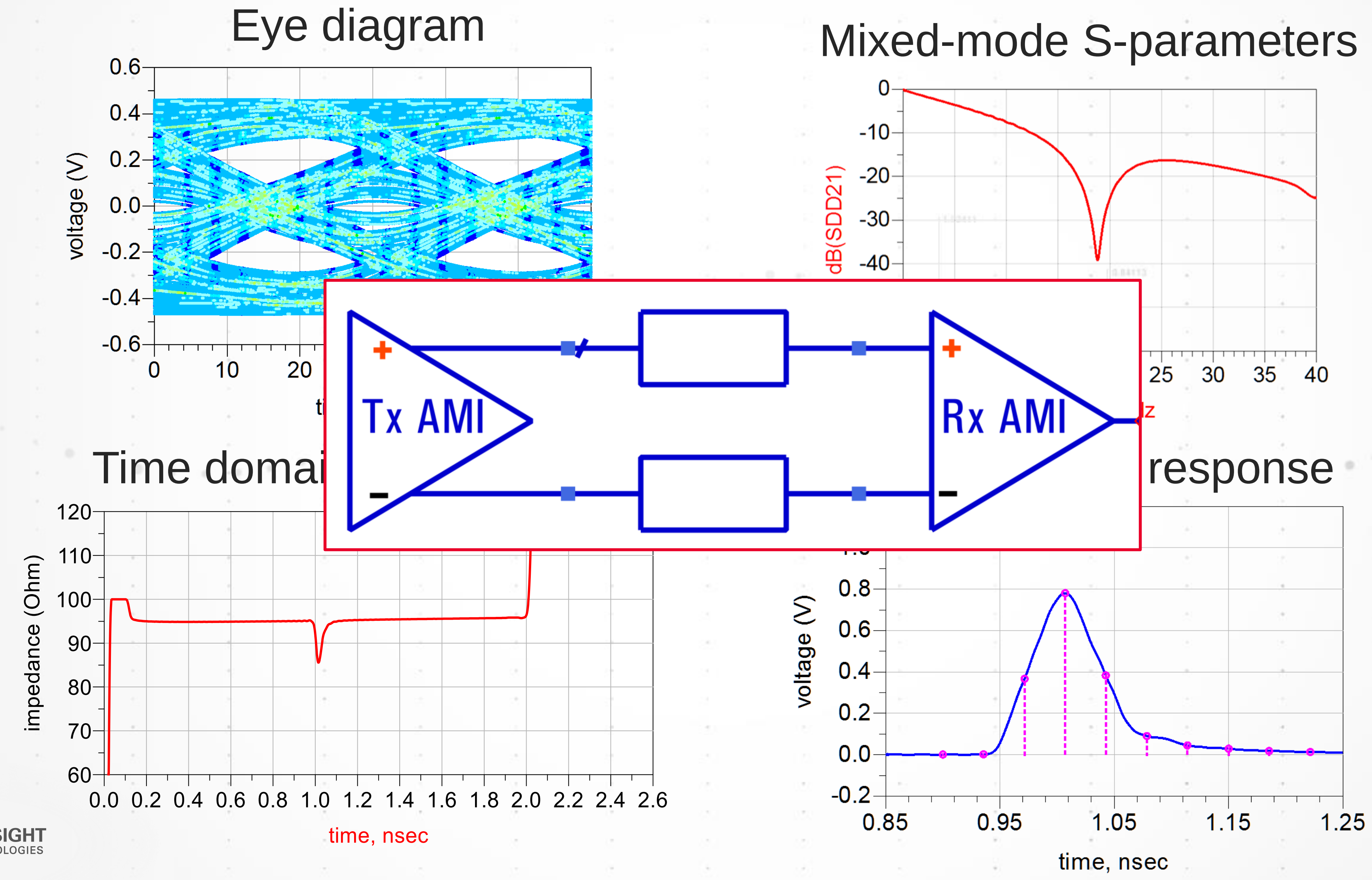
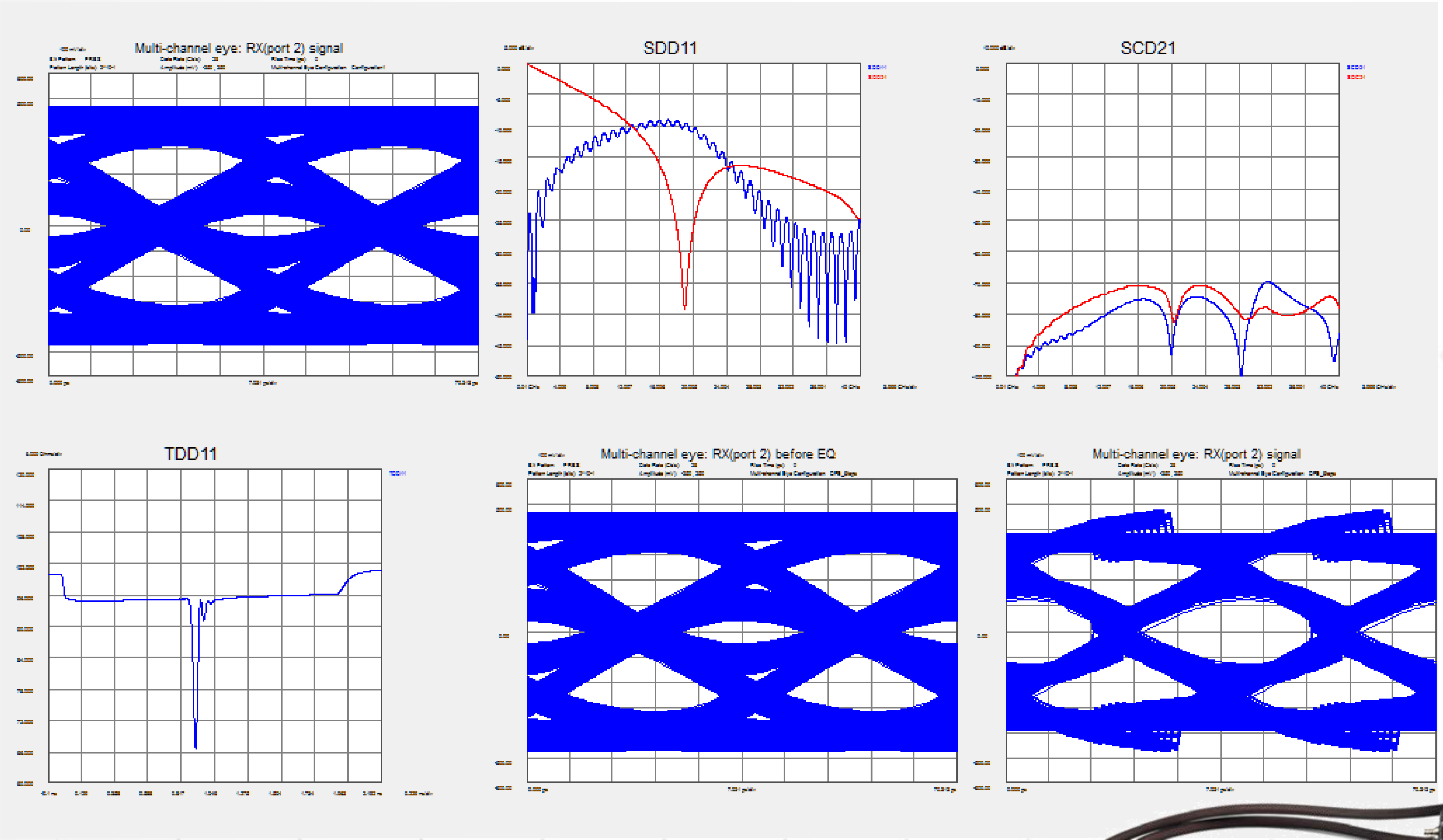
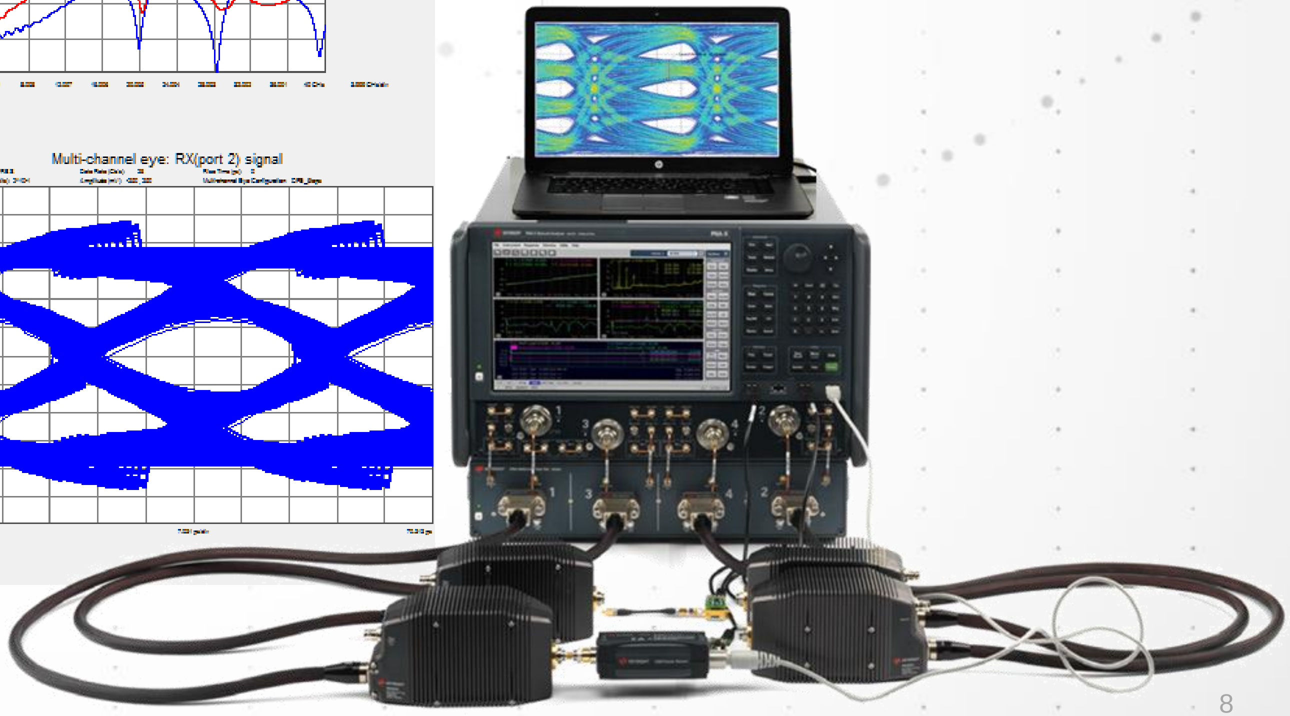
Essential Signal Integrity Analyses in Simulation

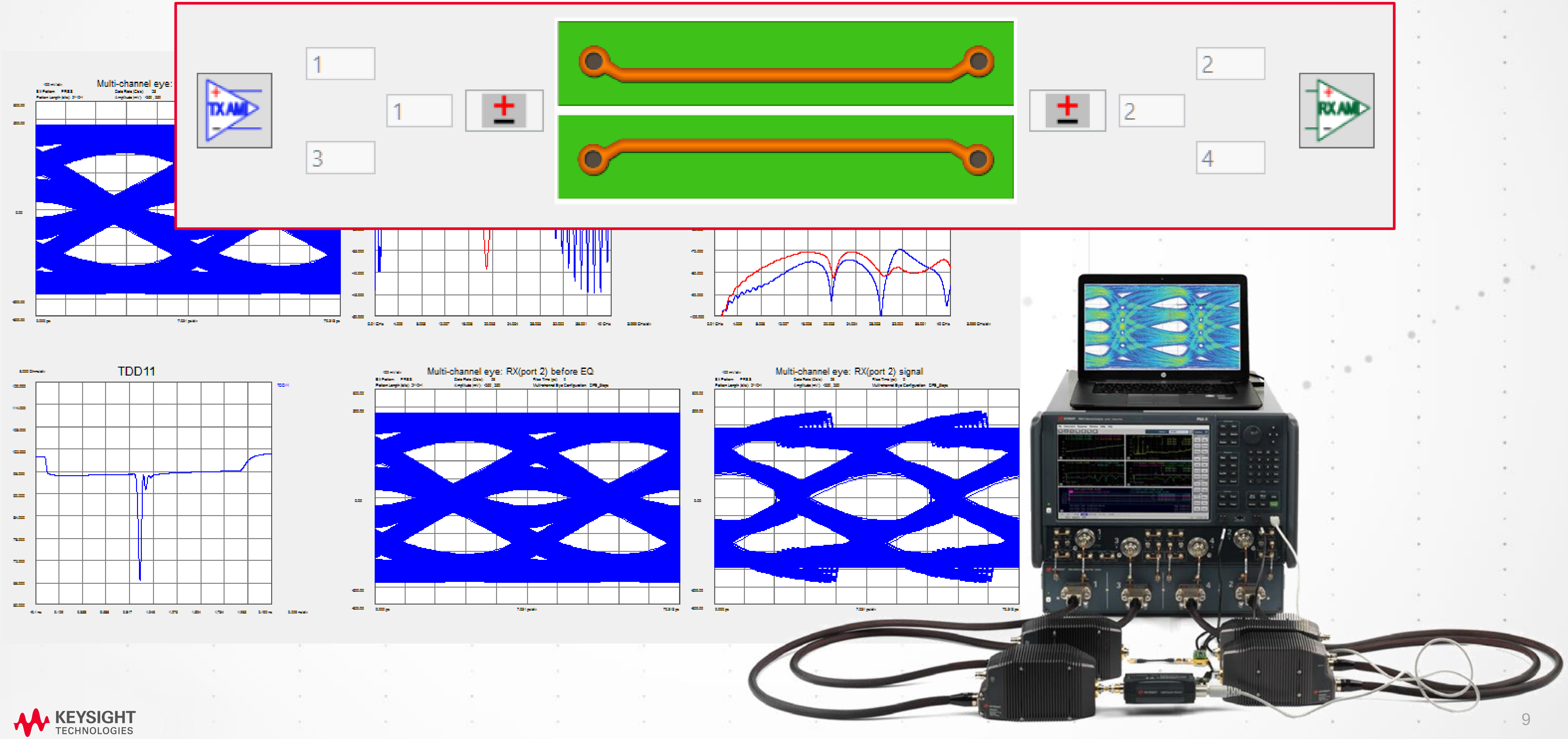


Essential Signal Integrity Analyses in Measurement





Essential Signal Integrity Analyses in Measurement



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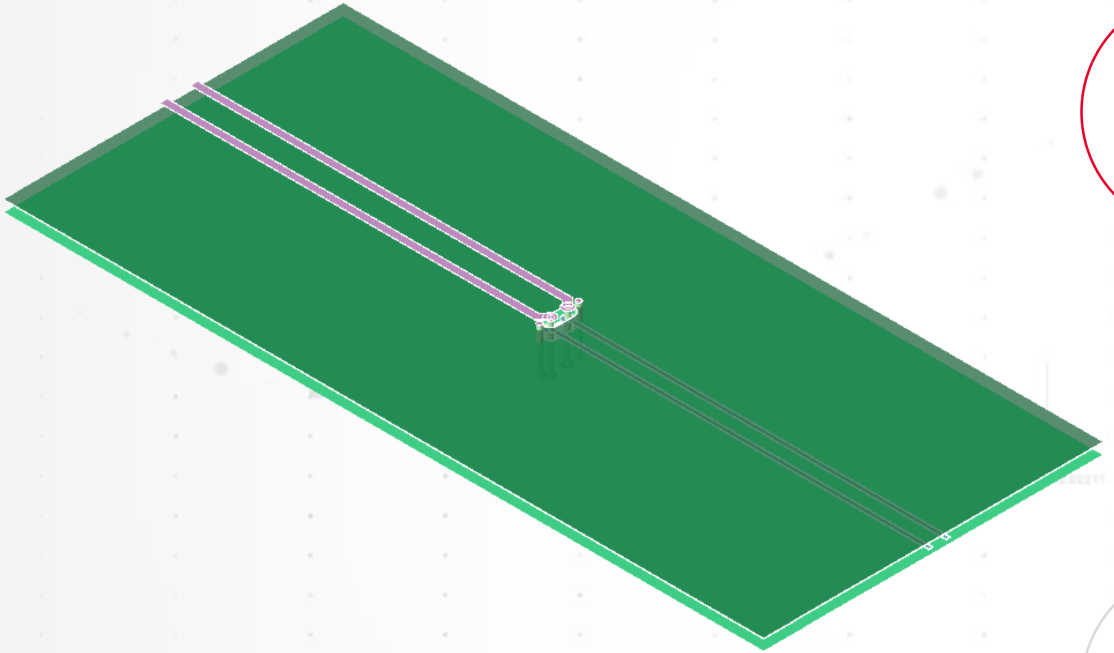

1. Simulate the channel
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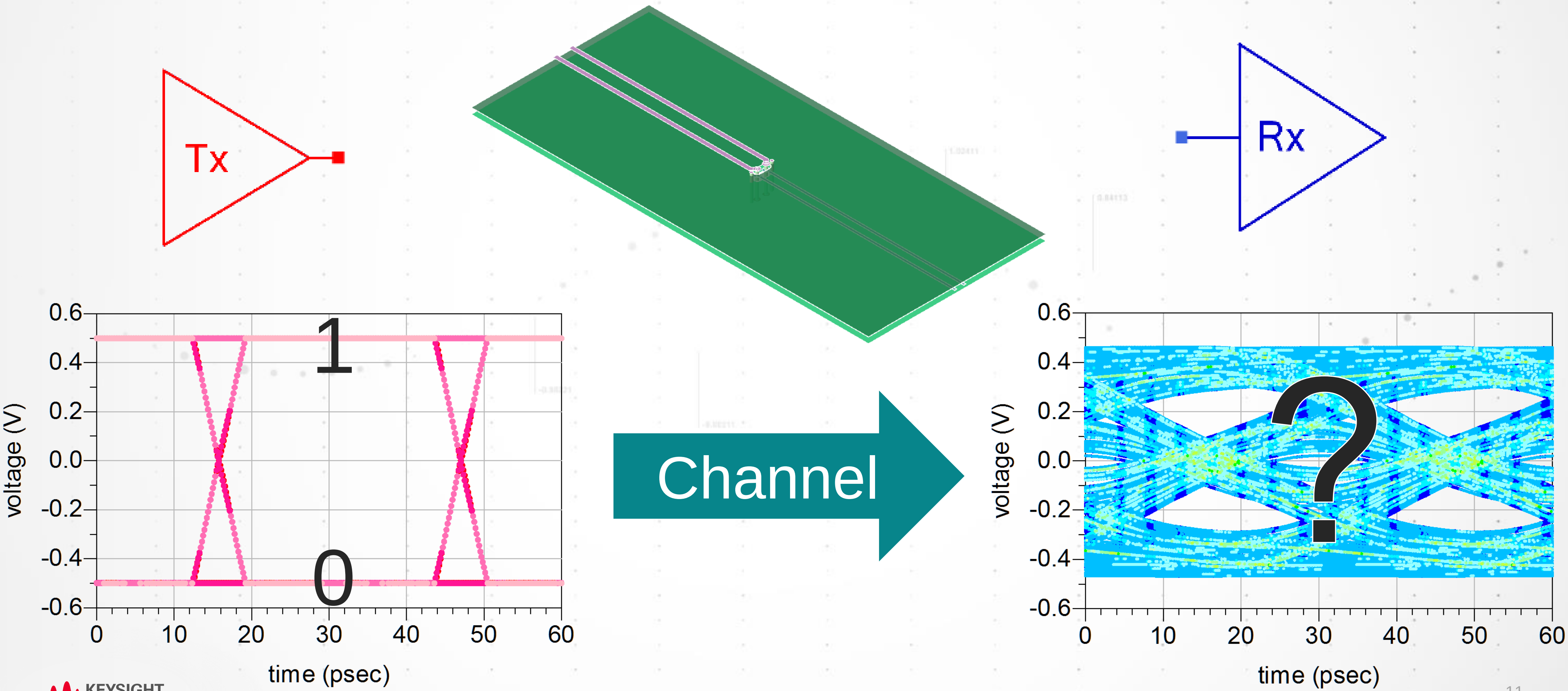
Use Eye Diagram Simulation to Evaluate a Channel

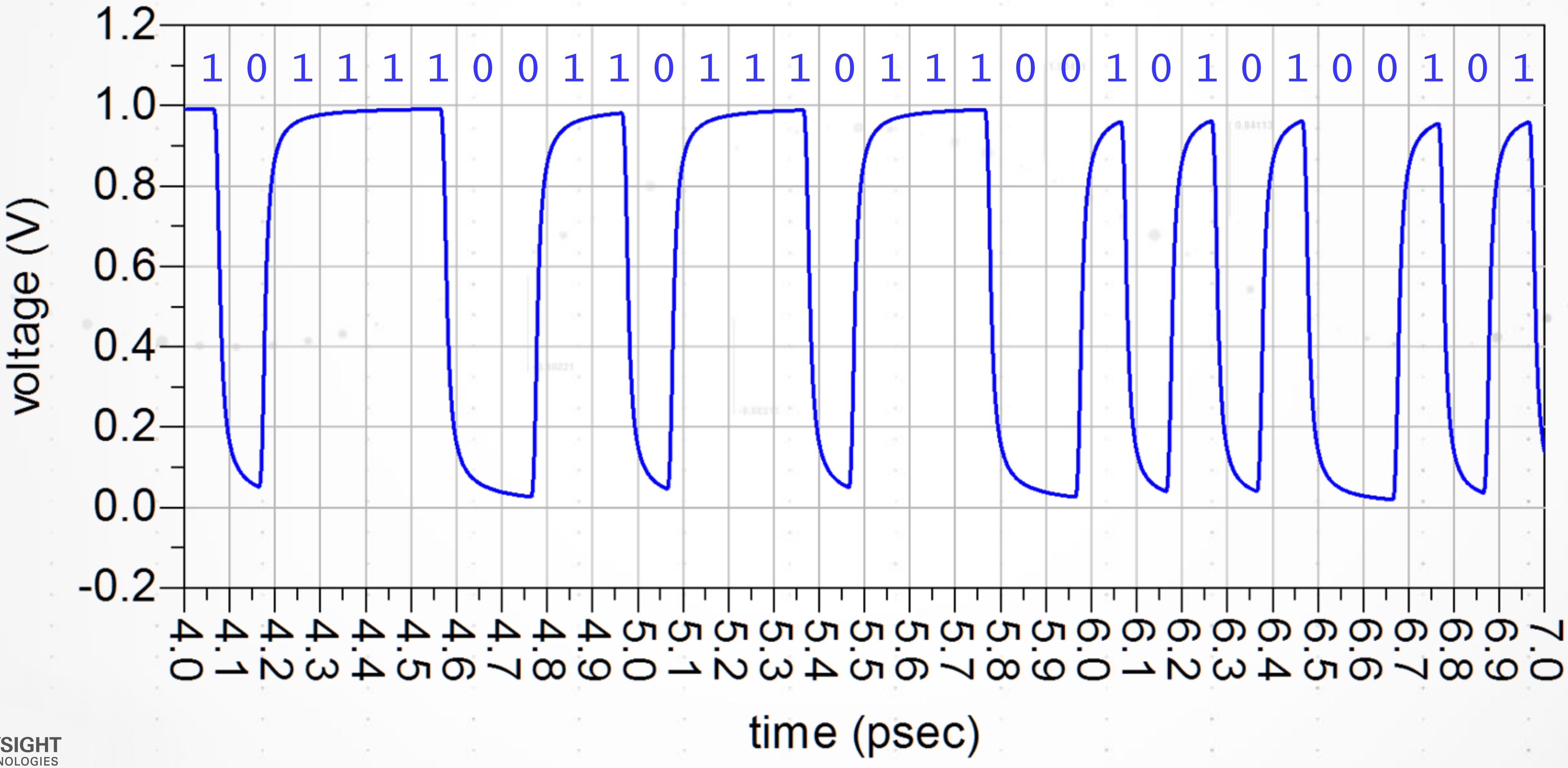


Construct Eye Diagram From PRBS

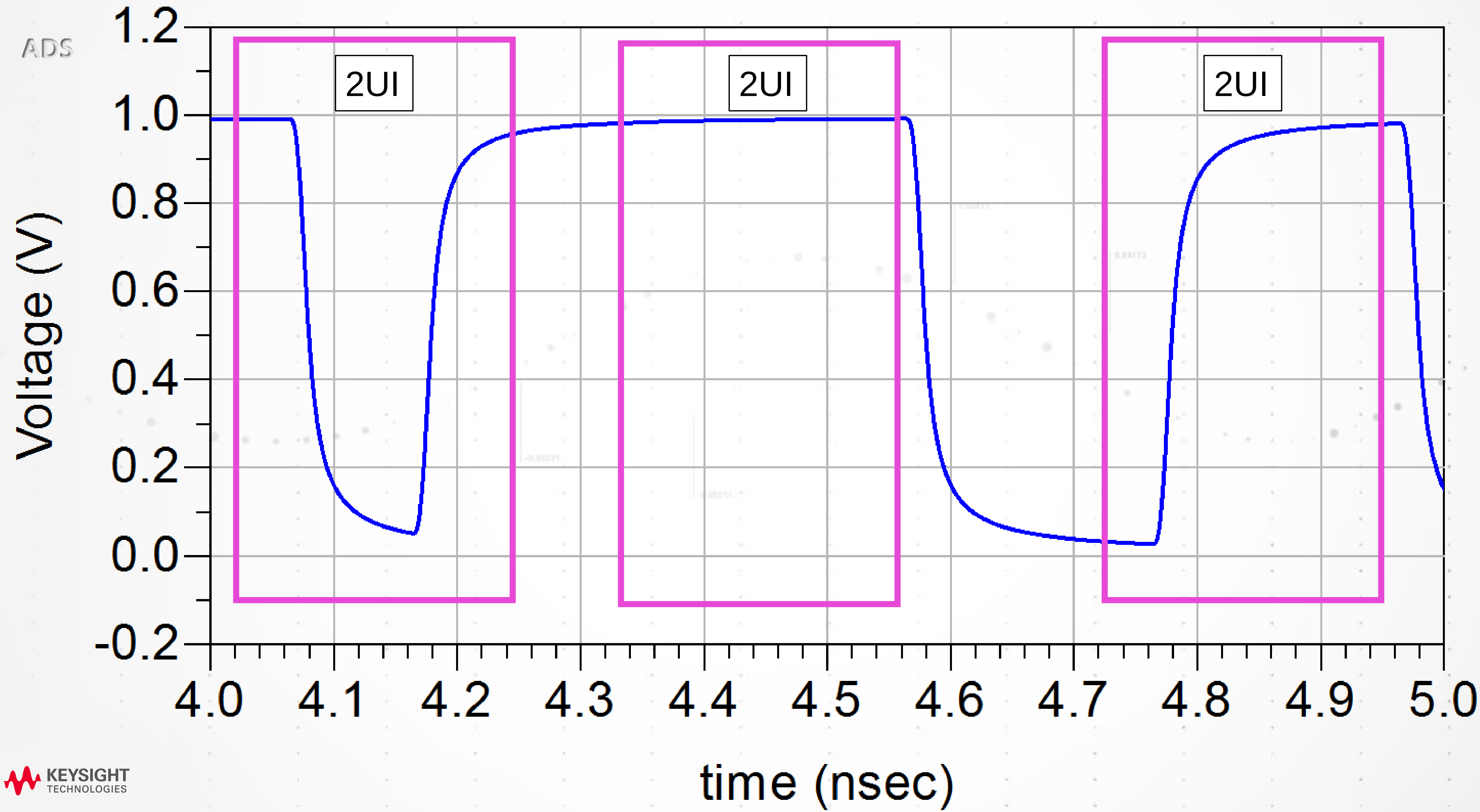
PRBS: Pseudo-Random Binary Sequence

By sending PRBS, we are testing how the channel affects all the possible transmitted data pattern.

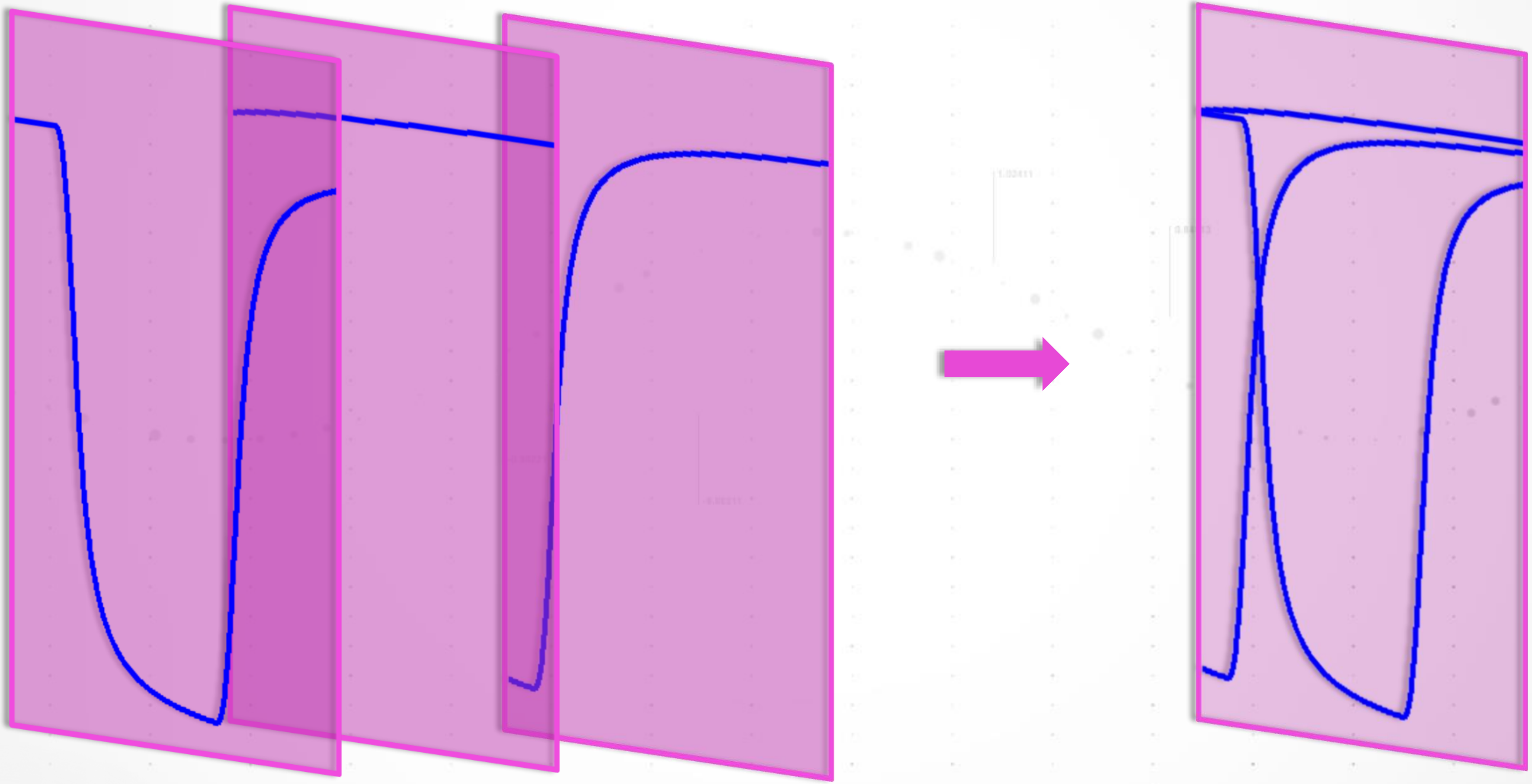
PRBSX: The 2^x-1 pseudo-random binary sequence combines every permutation of x bits.



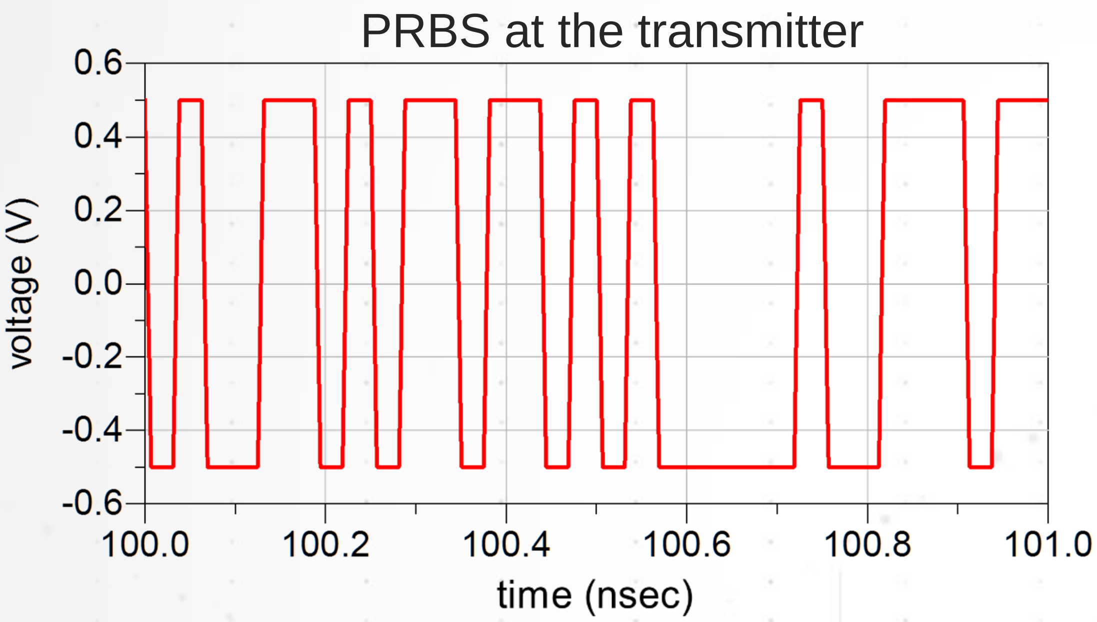
Partition PRBS Pattern by Unit Intervals

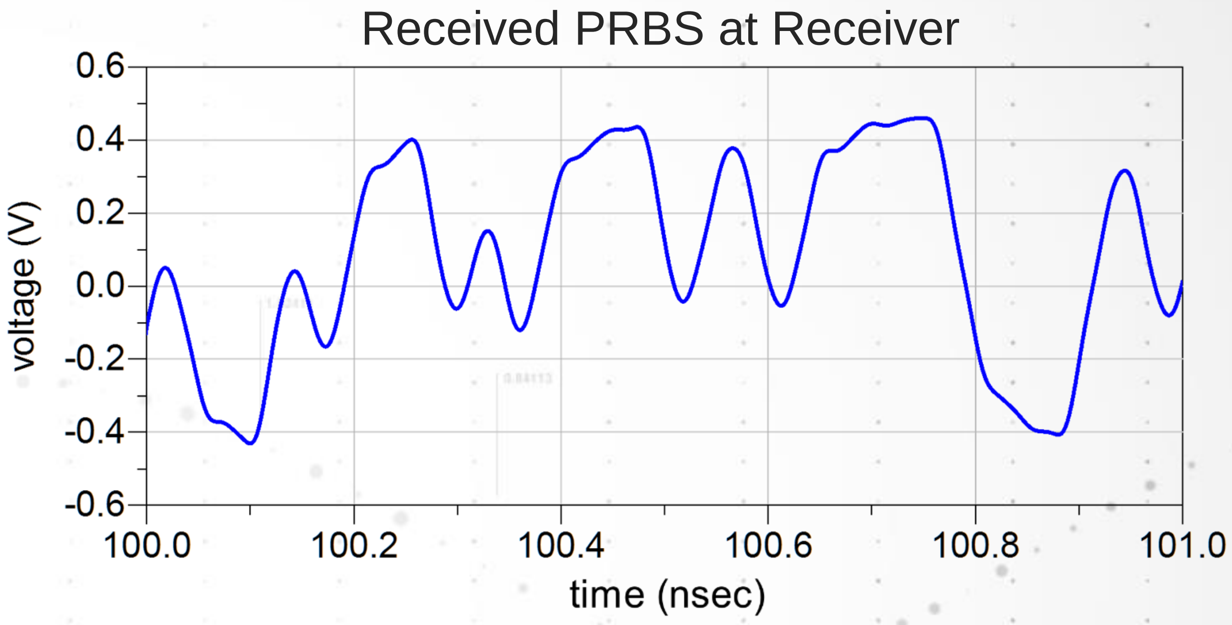


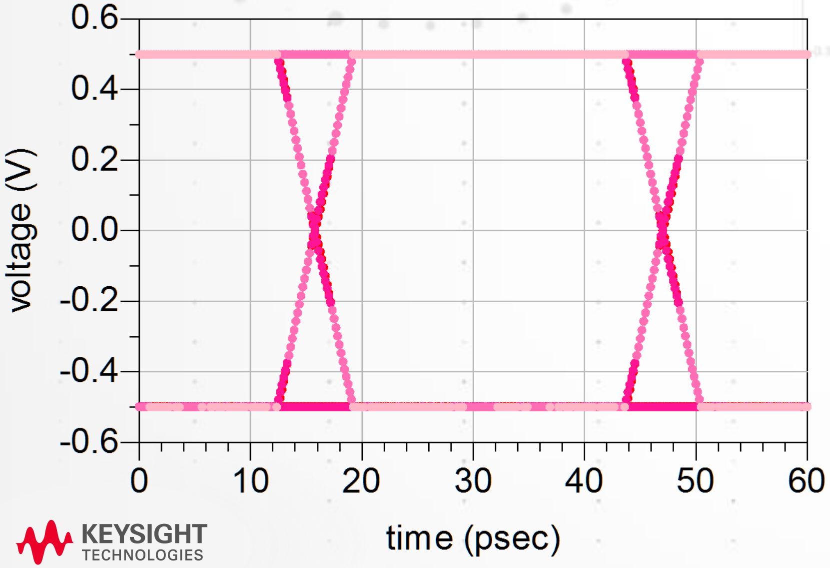
Overlay Partitioned PRBS Slices to Create the Eye

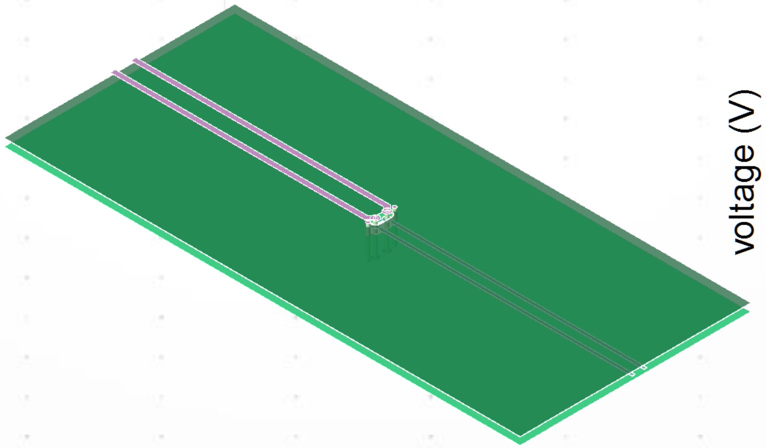


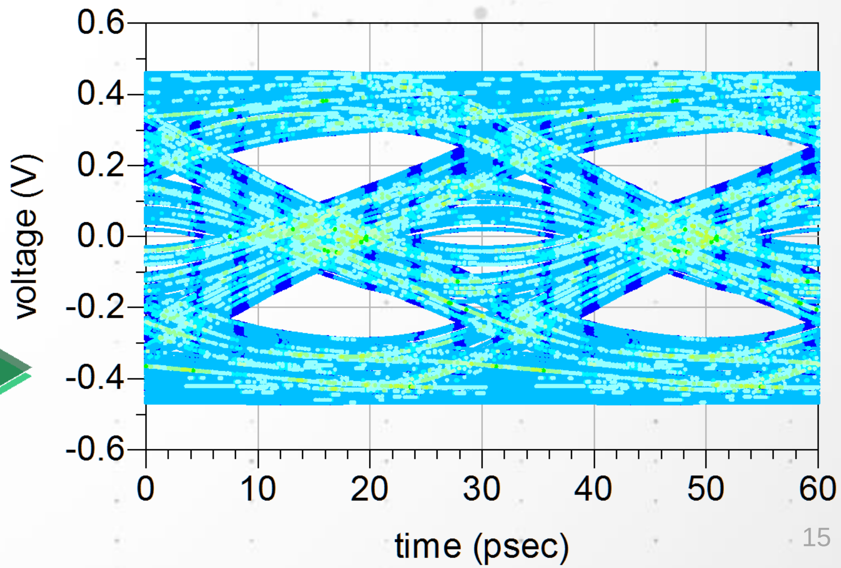
Closed Eye at the Receiver: Signal Integrity Problem











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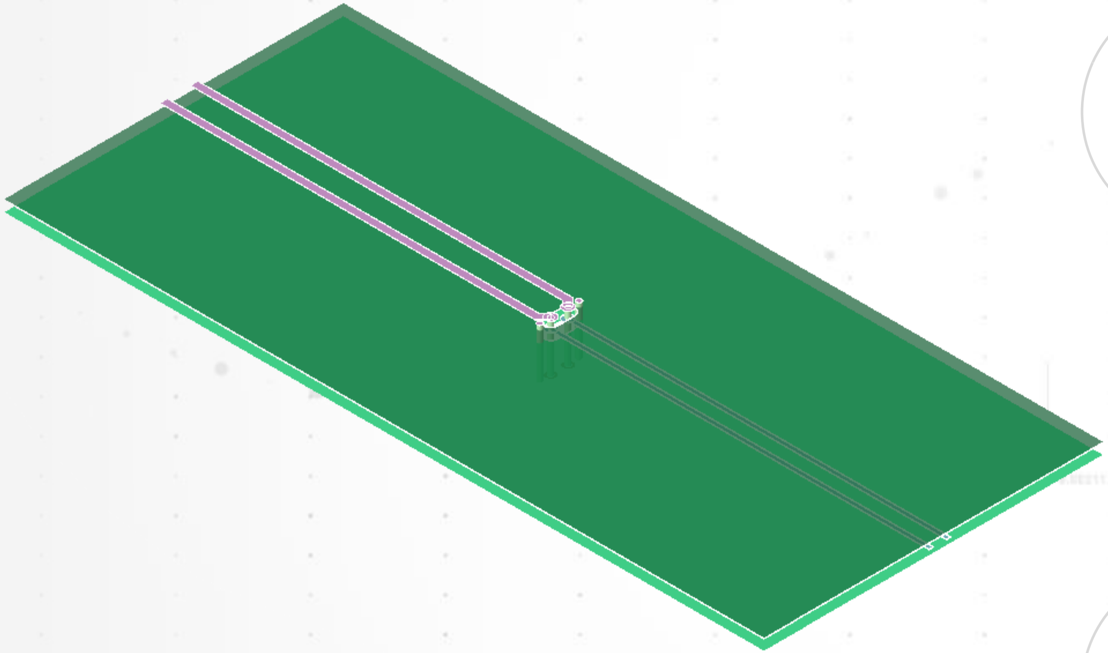

1 Simulate the channel

2 Find the root cause of degradation

3 Explore design solutions

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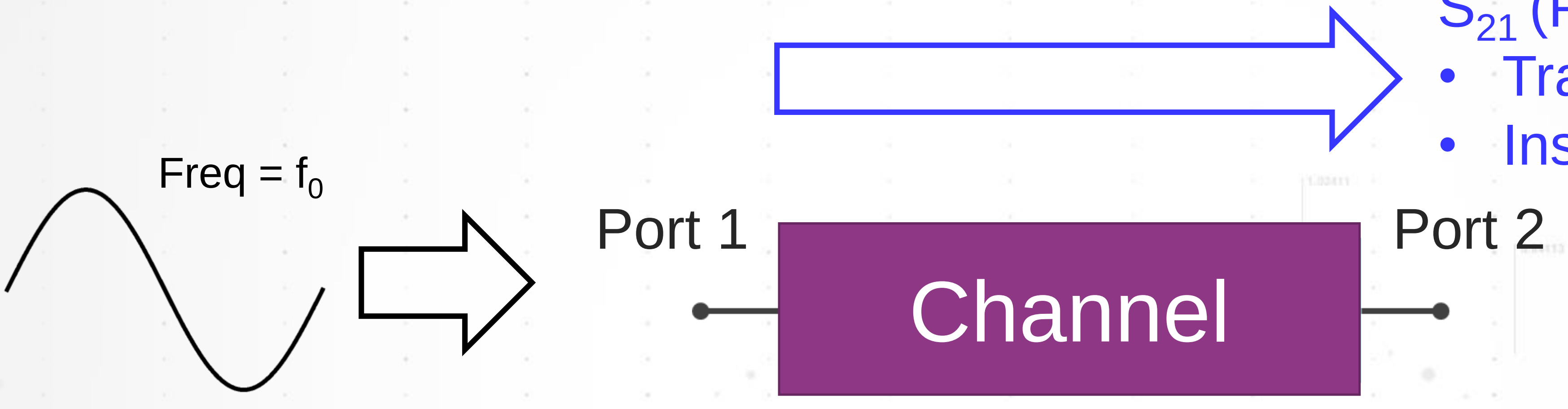
Use S-parameters to Investigate the Channel



S_{21} (Port 2 excited by port 1)
- Transmission coefficient
- Insertion loss

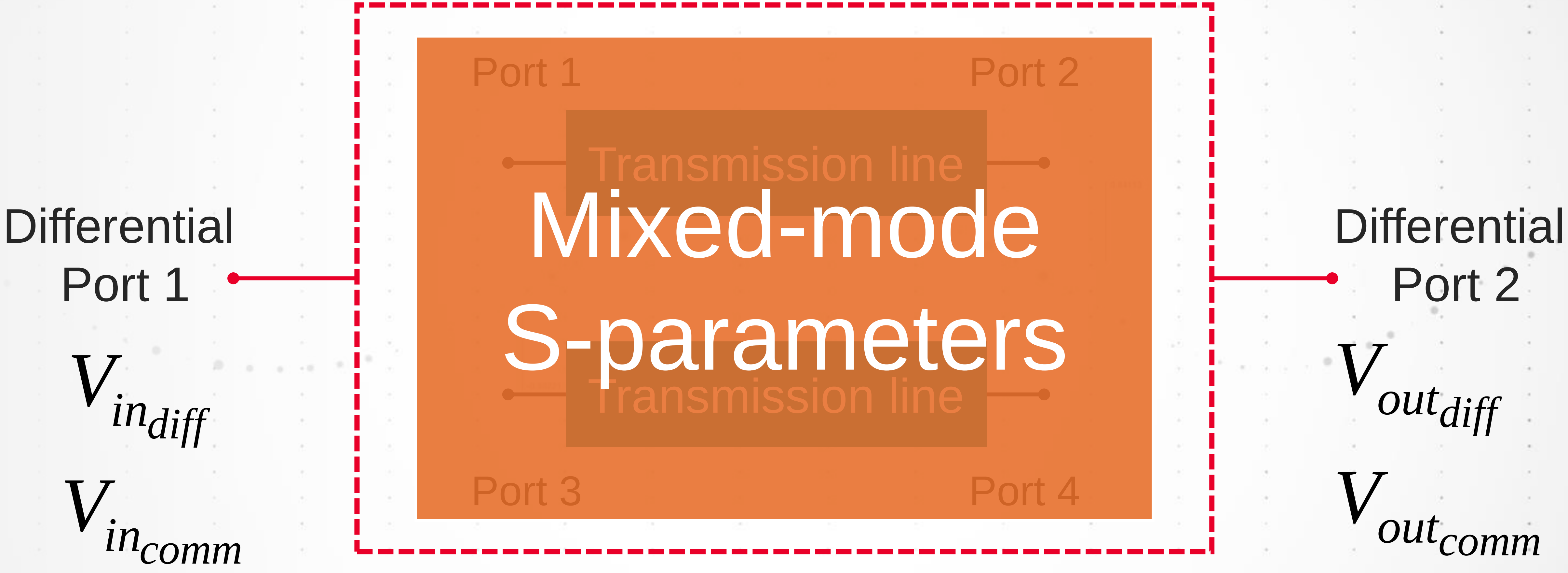
S_{11} (Port 1 excited by port 1)
- Reflection coefficient
- Return loss

Signal Integrity Convention:

$$\mathrm{RL}\ (\mathrm{dB}) = 20\log\left|S_{11}\right|$$

$$\mathrm{IL}\ (\mathrm{dB}) = 20\log\left|S_{21}\right|$$

Use Mixed-mode S-parameters for Differential Channels



Stimulus and Responses in Mixed-mode S-parameters

$[S_{mixed\text{-}mode}]$	Differential Signal Stimulus		Common Signal Stimulus	
Differential Response	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
Common Response	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}

Important Mixed-mode S-parameters

S_{DD11} Differential response at port 1, excited by Differential input at port 1.

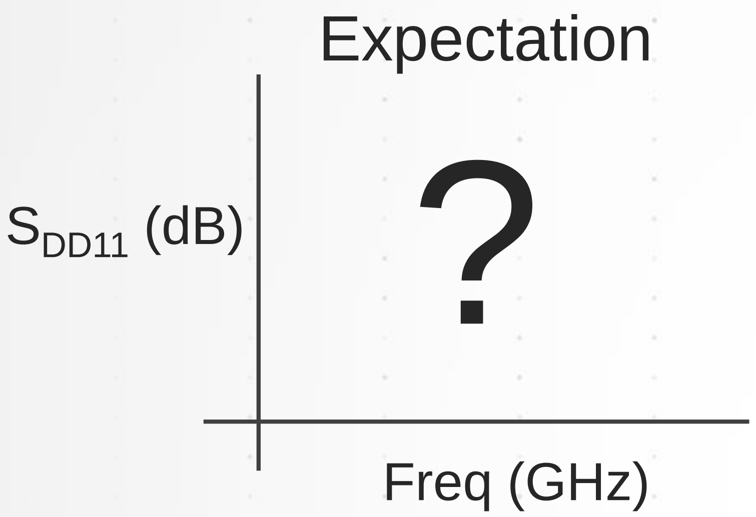
S_{DD11} Related to differential return loss.

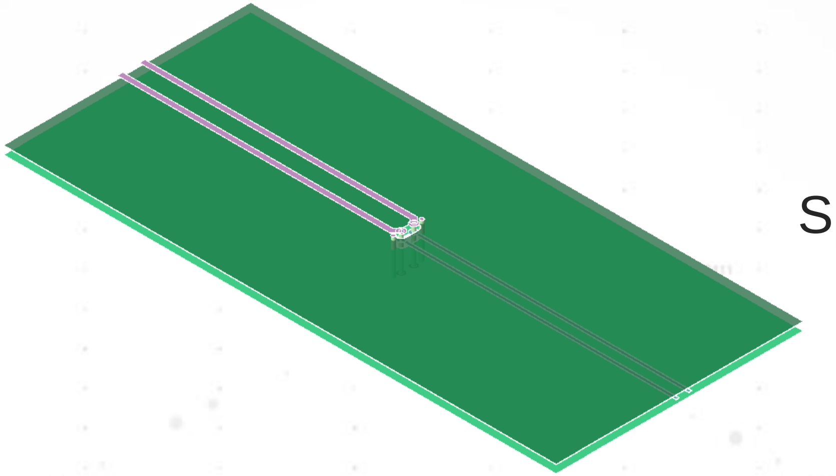
S_{DD21} Related to differential insertion loss.

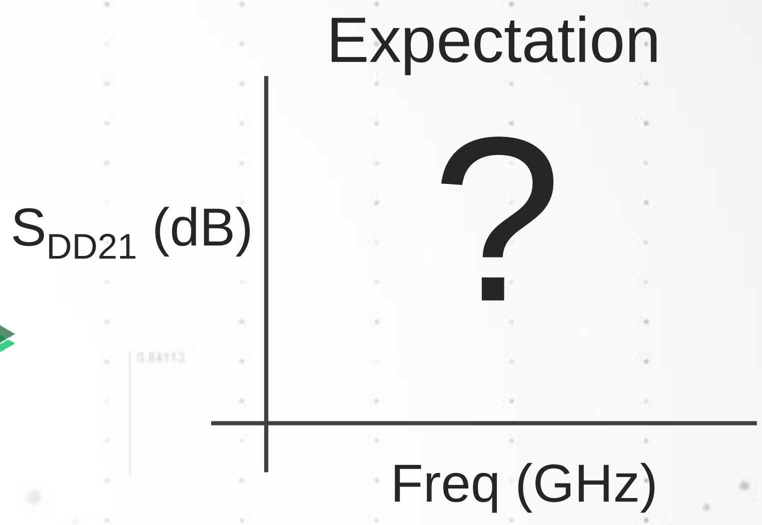
S_{CD21} Mode-conversion: EM generation.

S_{DC21} Mode-conversion: EM susceptibility.

Rule #9: What Do We Expect with Given Channel?







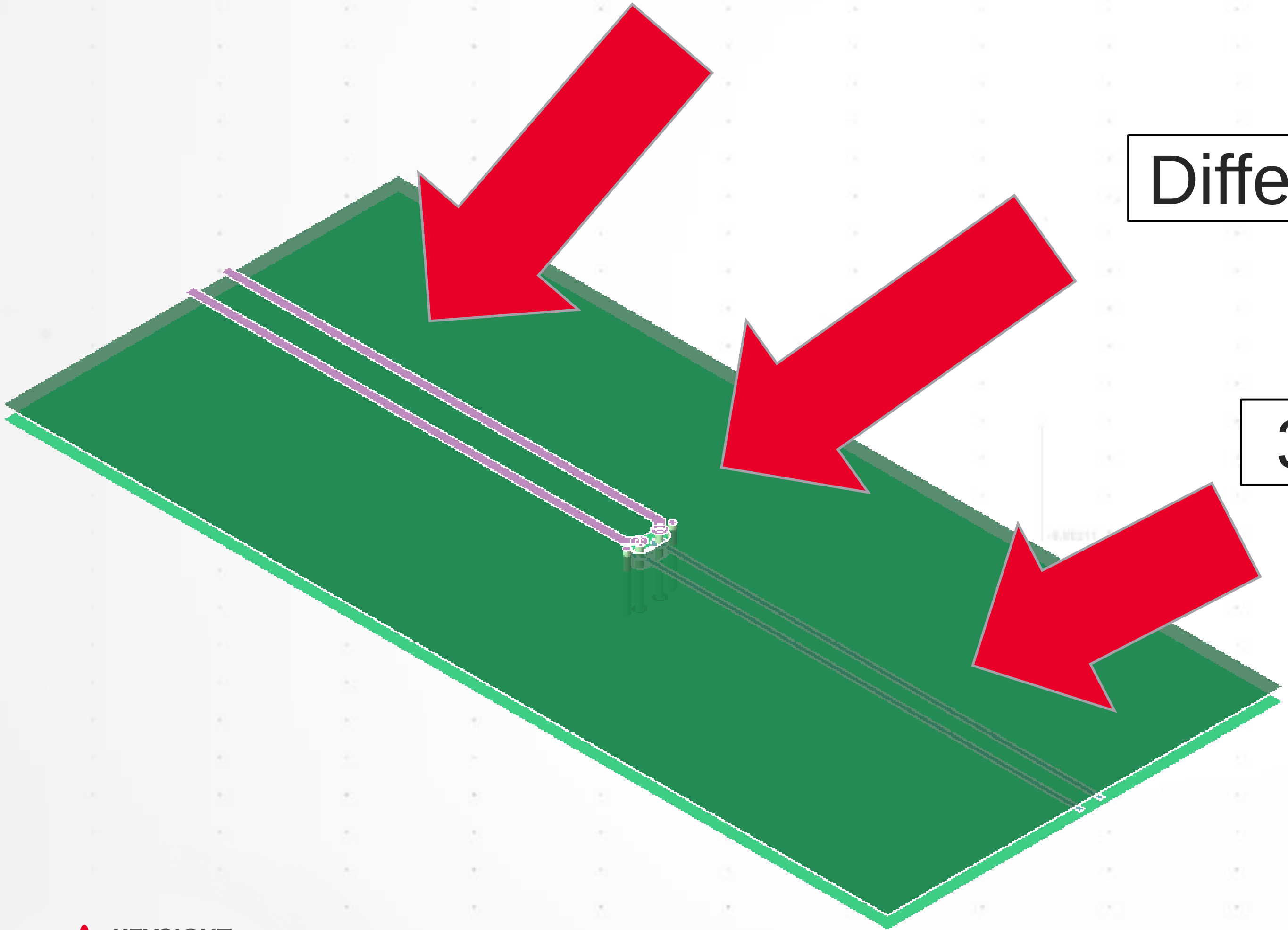
Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)			
Impedance (Ohm)			

First Glimpse of the Virtual Channel

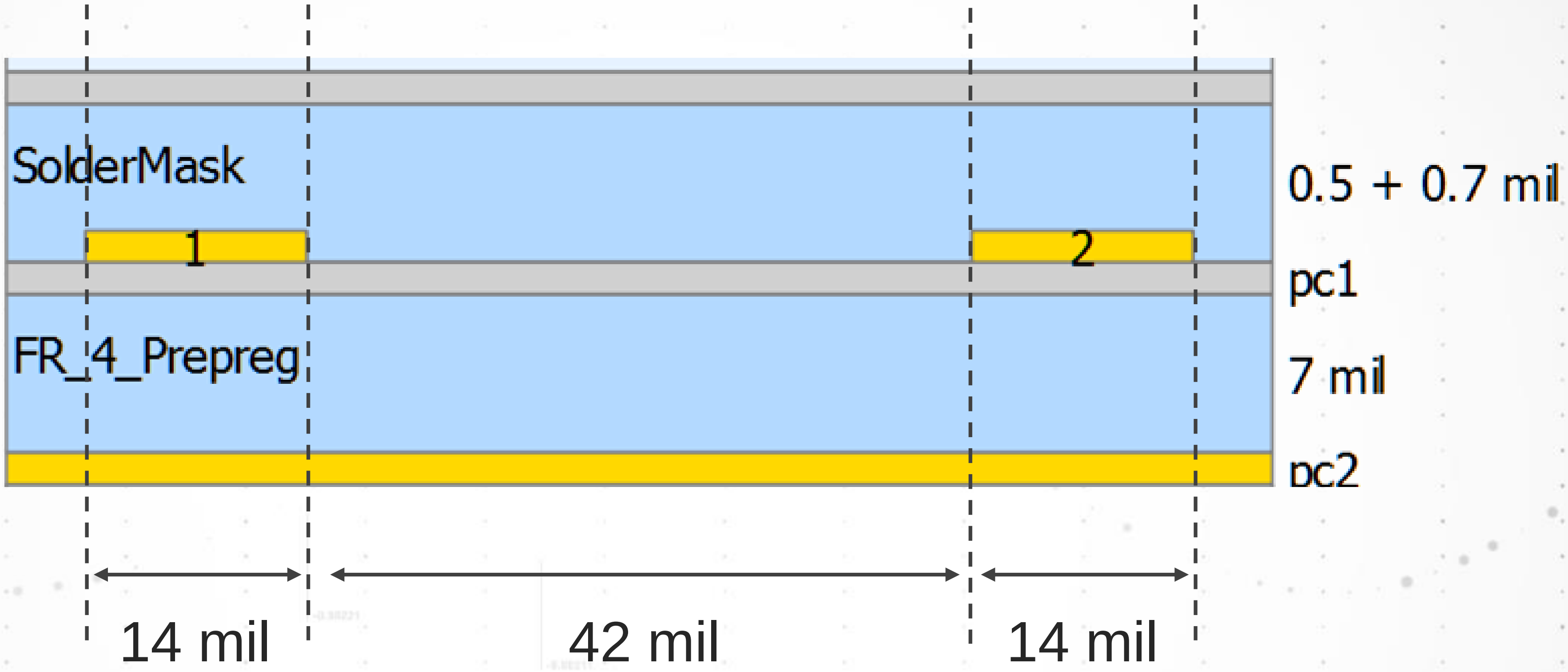
3-inch microstrip differential pair

Differential Via structure

3-inch stripline differential pair



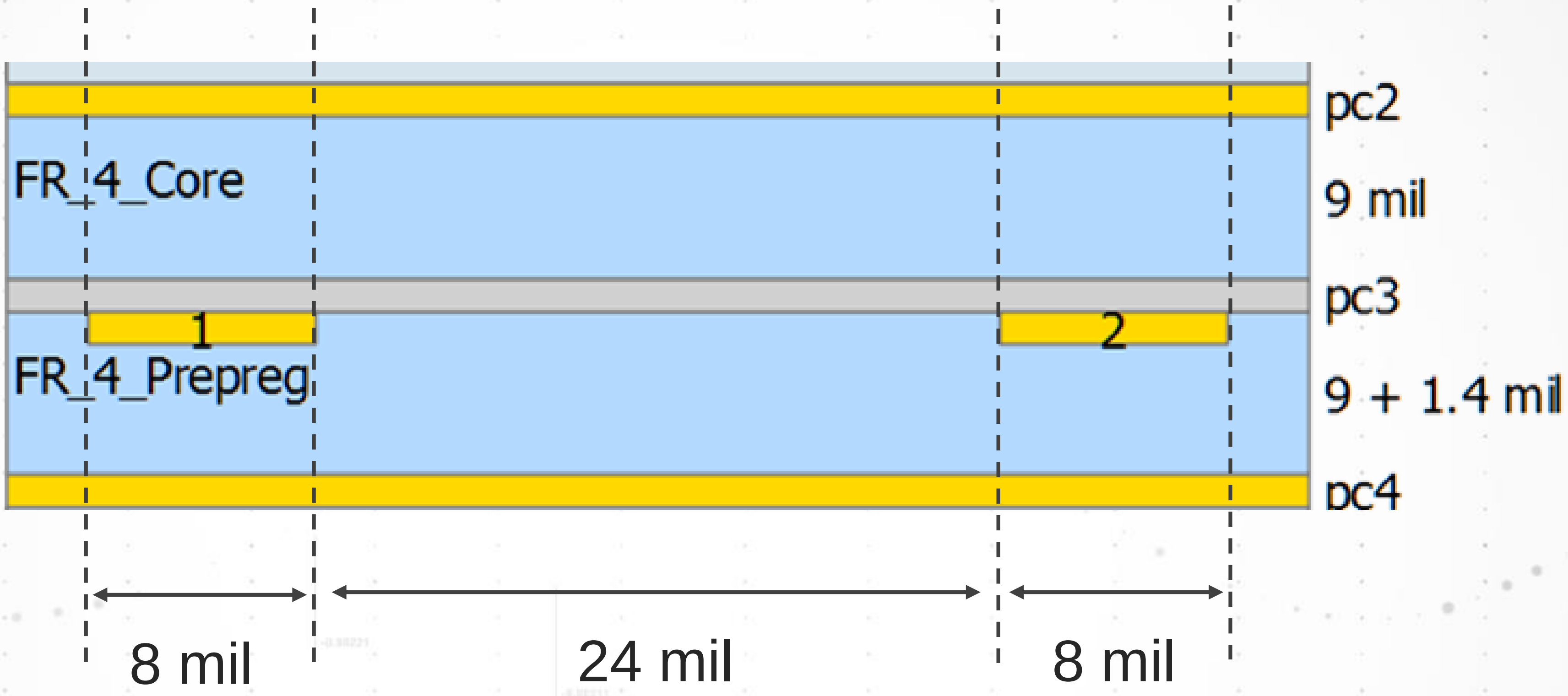
Cross-section of the Microstrip Differential Pair



Single-ended Microstrip Impedance
Rule of Thumb: W/H = 2 → Z = 50 Ohm

Because of solder mask, we expect:
differential impedance <100 Ohm

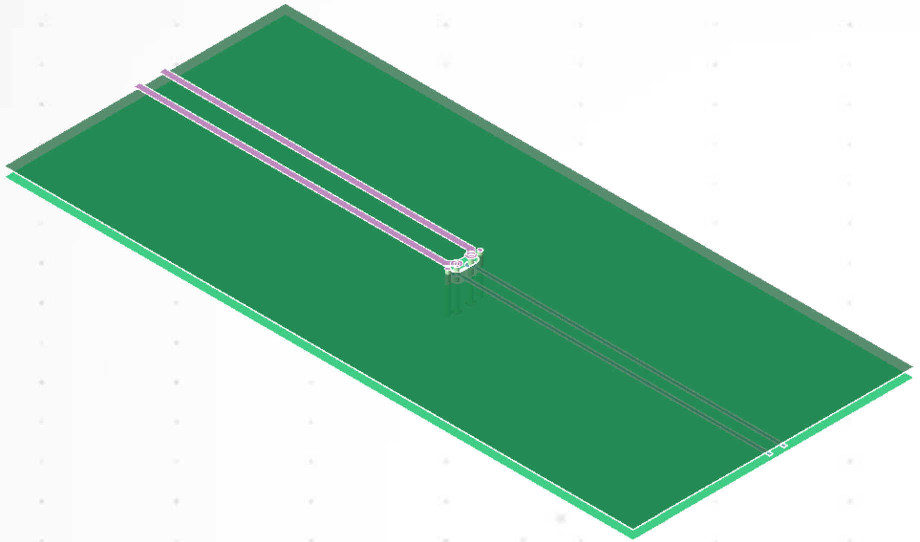
Cross-section of the Stripline Differential Pair



Single-ended Microstrip Impedance Rule of Thumb:
0.8 < W/H < 1 → Z ~ 50 Ohm

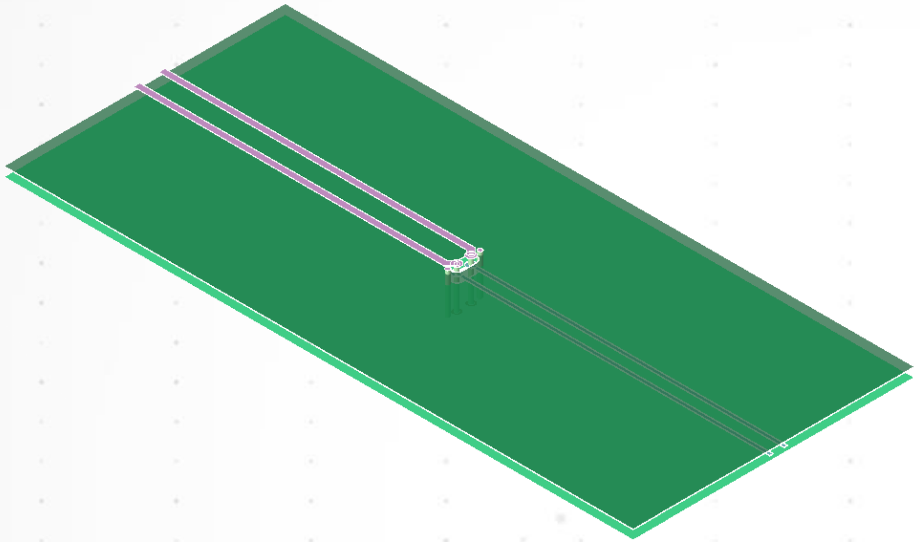
We expect:
differential impedance ~100 Ohm

Rule #9: What Loss Do We Expect with Given Channel?



Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)			
Impedance (Ohm)	<100		~100

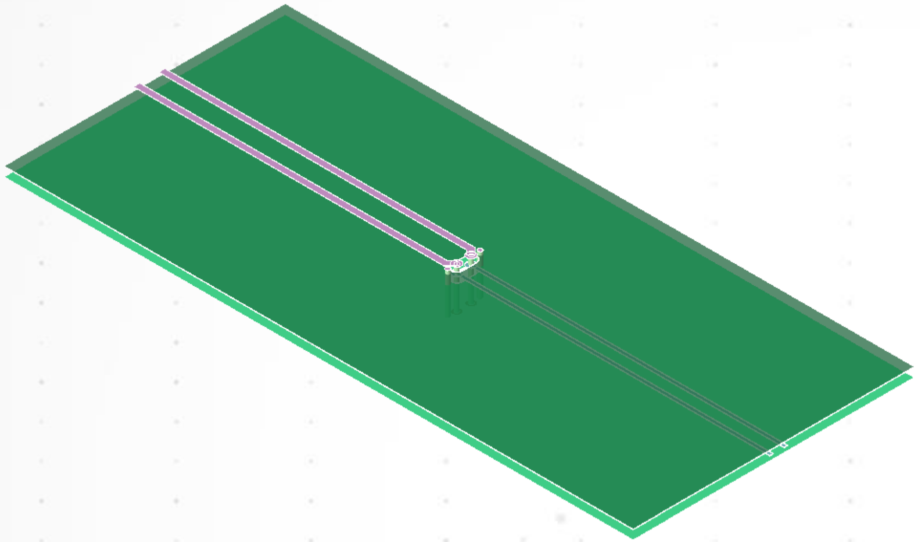
Rule #9: What Loss Do We Expect with Given Channel?



Date Rate: 32 Gbps
Nyquist Frequency: 16 GHz
Estimated Loss: ~ 0.1 dB/in/GHz

Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)			
Impedance (Ohm)	<100		~100

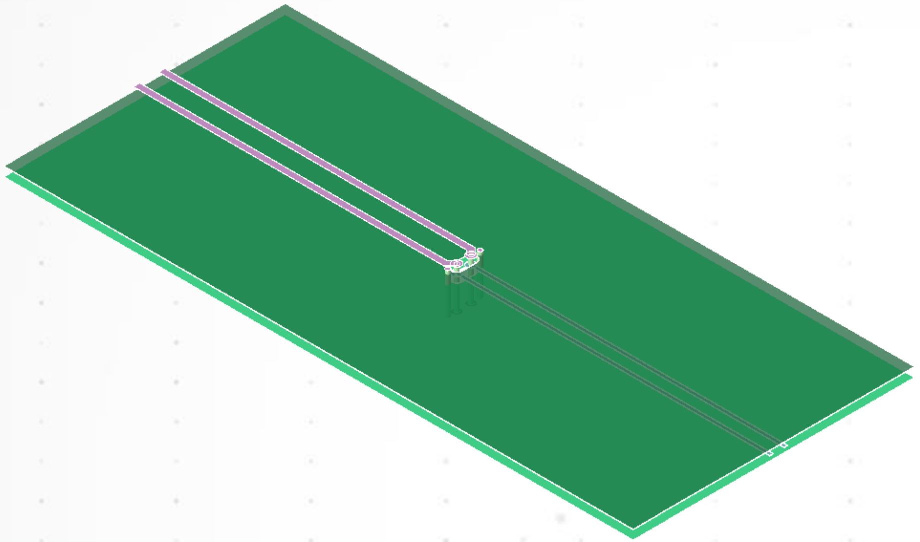
Rule #9: What Loss Do We Expect with Given Channel?



Date Rate: 32 Gbps
Nyquist Frequency: 16 GHz
Estimated Loss: ~ 0.1 dB/in/GHz

Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)	5 dB		5 dB
Impedance (Ohm)	<100		~100

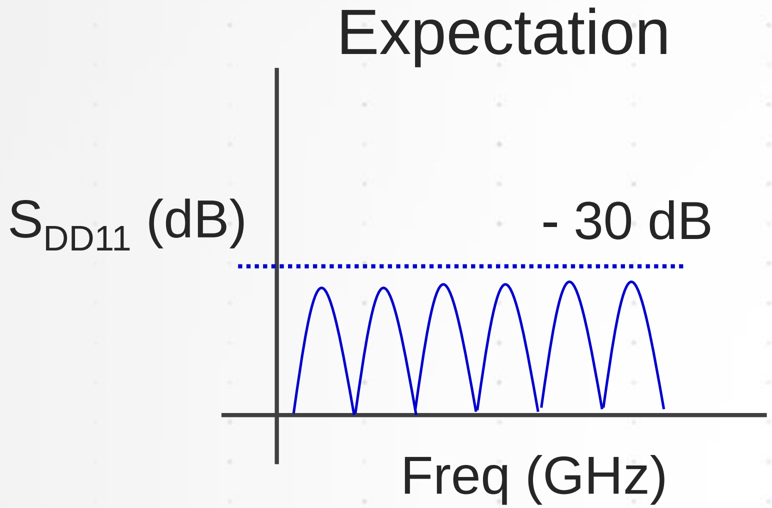
Rule #9: What Loss Do We Expect with Given Channel?

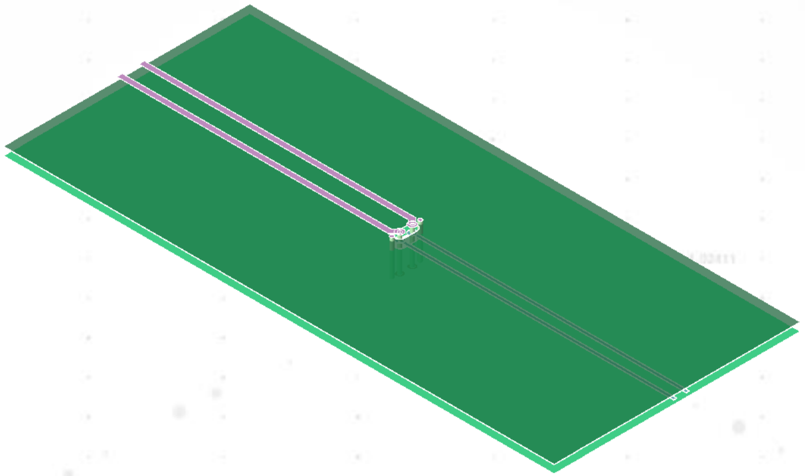


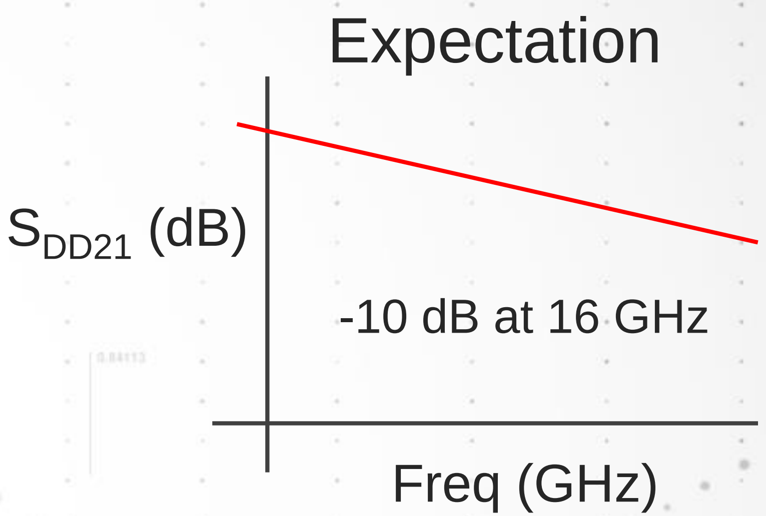
Date Rate: 32 Gbps
Nyquist Frequency: 16 GHz
Estimated Loss: ~ 0.1 dB/in/GHz

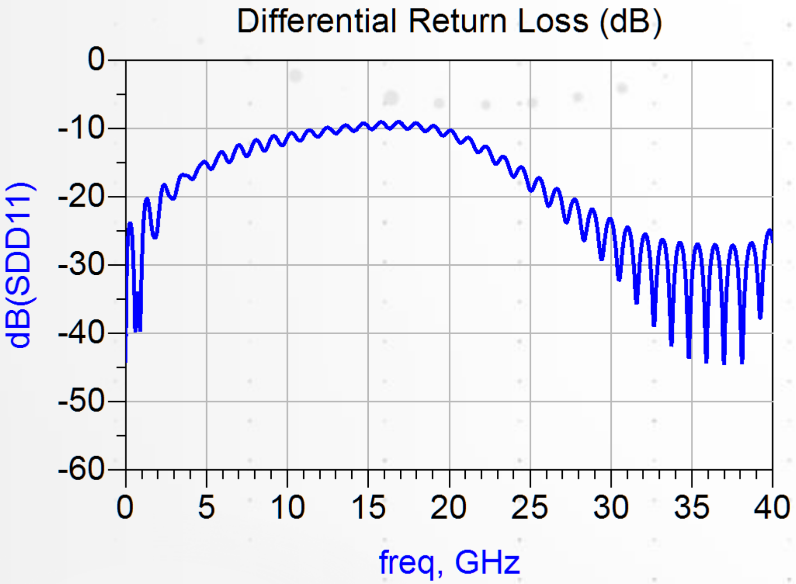
Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)	5 dB	small	5 dB
Impedance (Ohm)	<100	?	~100

Compare Expectation to S-Parameters Result



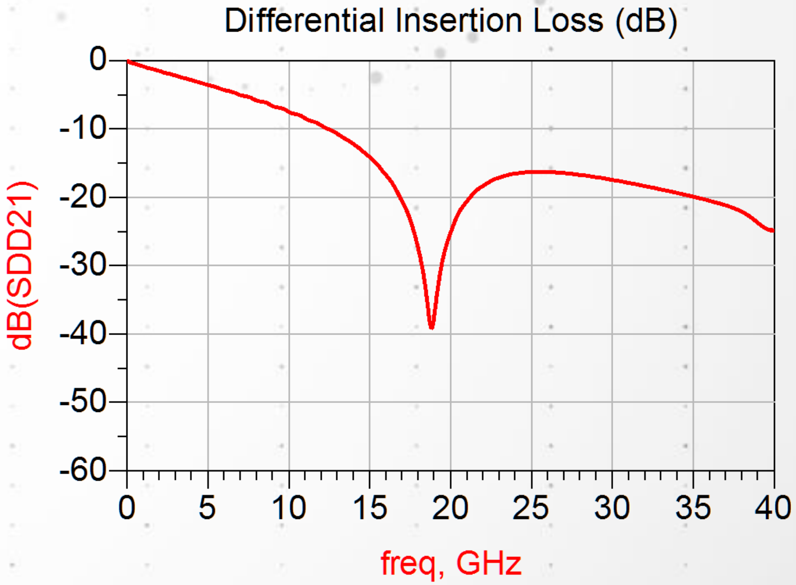




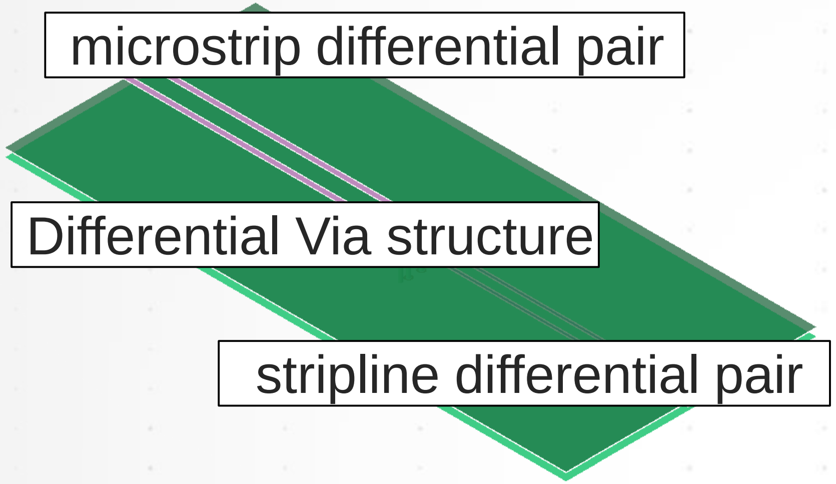


Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)	5	Small	5
Impedance (Ohm)	<100	?	~100

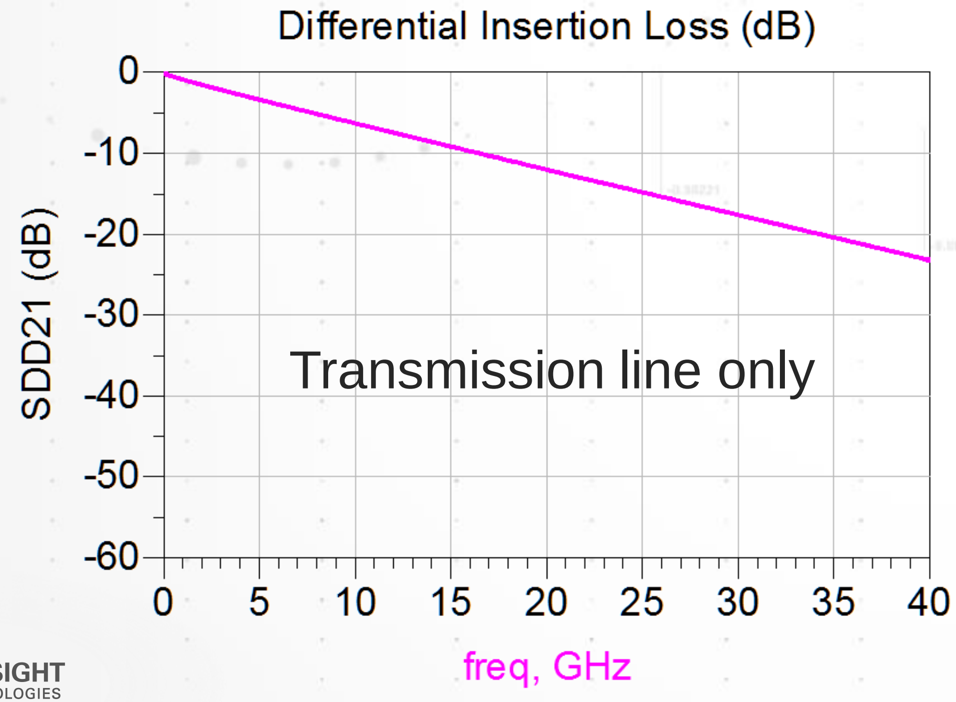
Not what we expect!

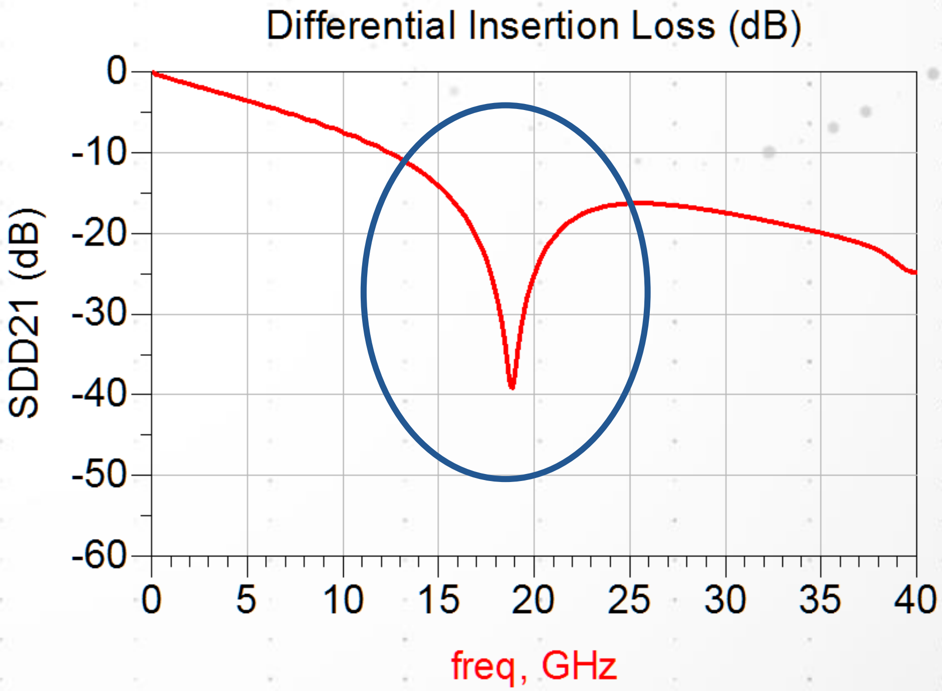


Simulate Only the Transmission Lines

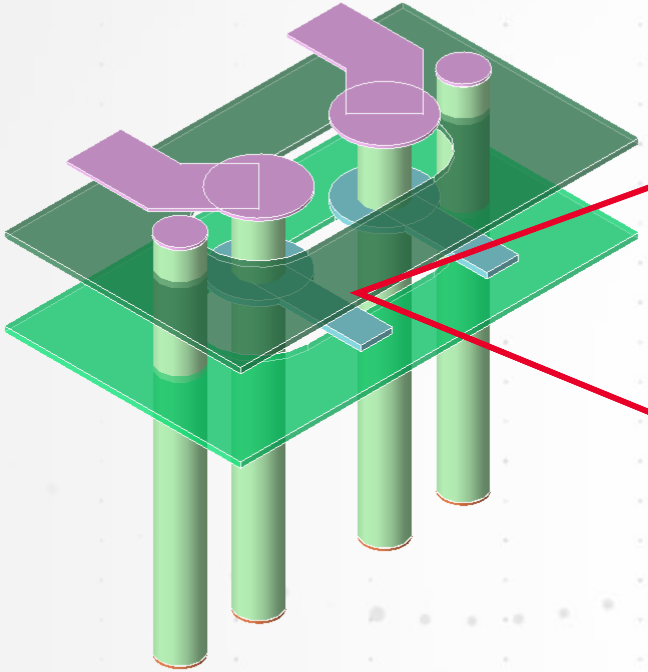


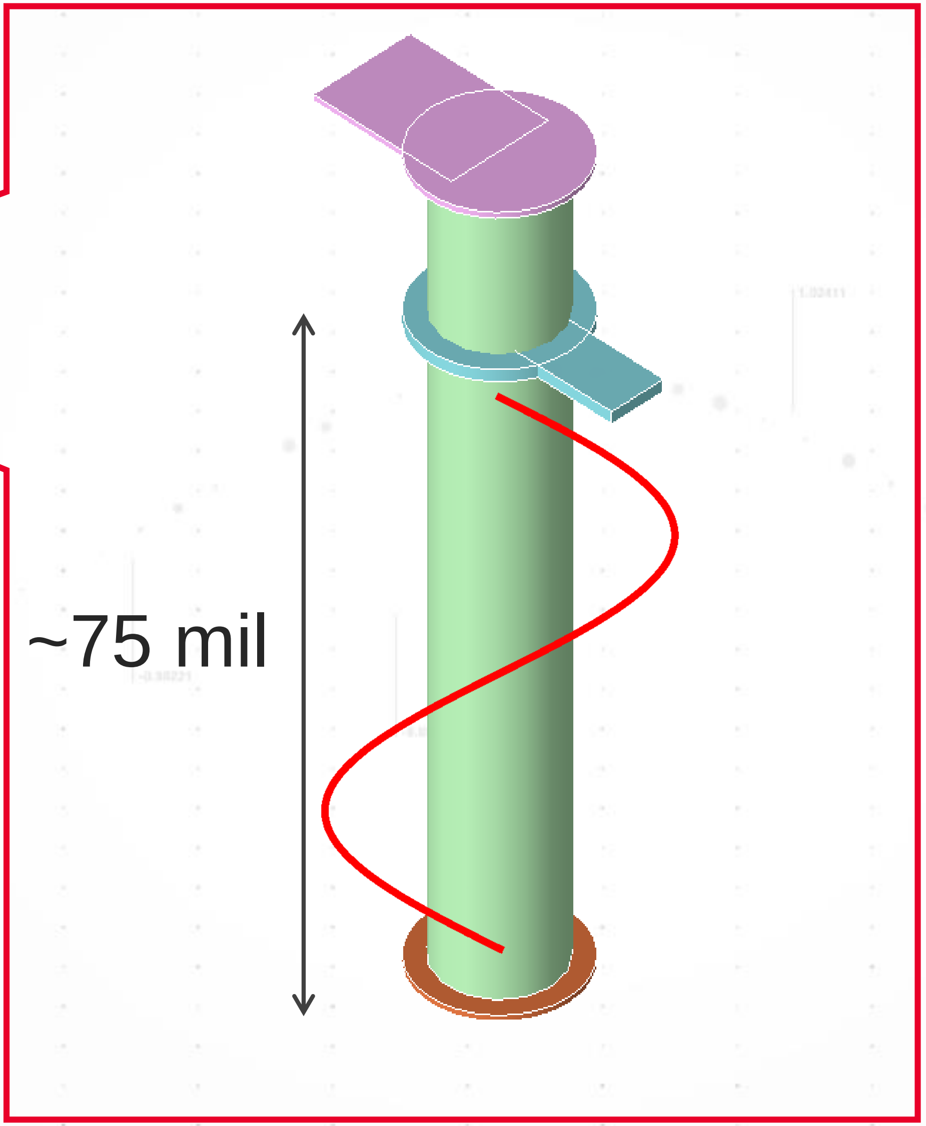
Structure	3-inch microstrip	Via	3-inch stripline
Estimated Loss (dB at Nyquist)	5	Small	5





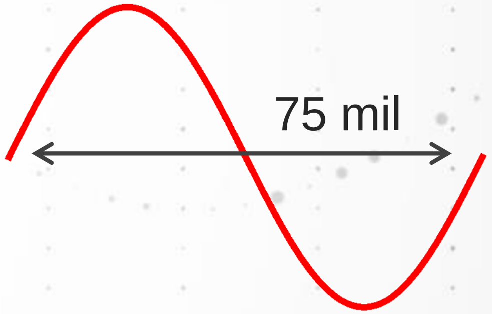
Via Structure Consists of Transmission Line





Data rate: 32 Gbps
Nyquist: 16 GHz

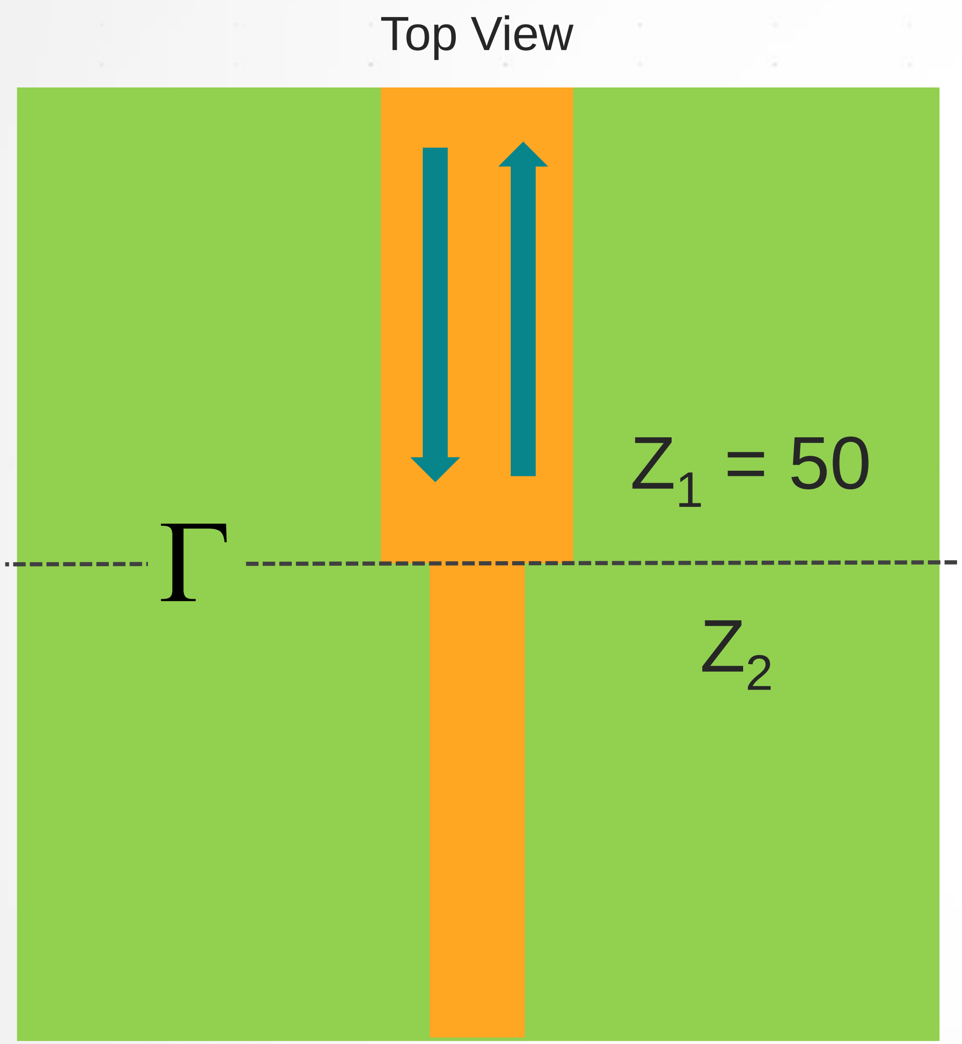
Bandwidth: 5*16 = 80 GHz
Wavelength: 6 in/nsec/80 ~ 75 mil



Transmission line:

Voltages and currents vary in magnitude and phase over physical length.

Impedance Discontinuity Creates Reflection in TLine



Γ : Reflection Coefficient

$$\Gamma = \frac{Z_2 - Z_1}{Z_1 + Z_2}$$

Z_2 (Ohm)	Z_2 short	$Z_2 < 50$	$Z_2 = 50$	$Z_2 > 50$	Z_2 open
Γ	**-1**	$-1<\Gamma<0$	**0**	$0>\Gamma>1$	**1**

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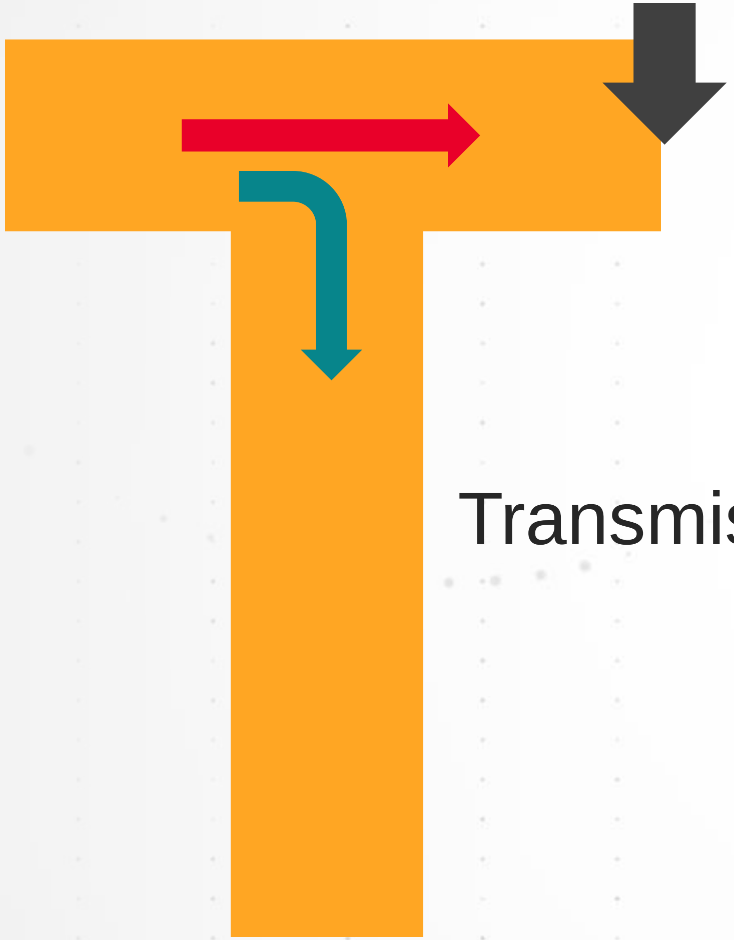
What Can Reflected Waves Do?

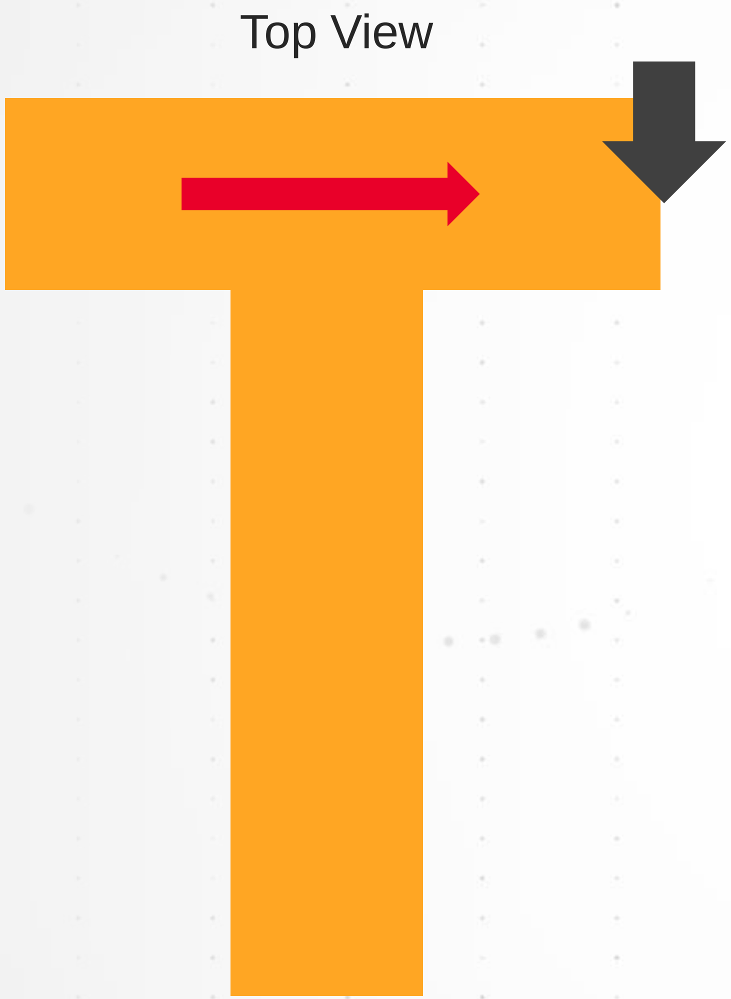
Top View

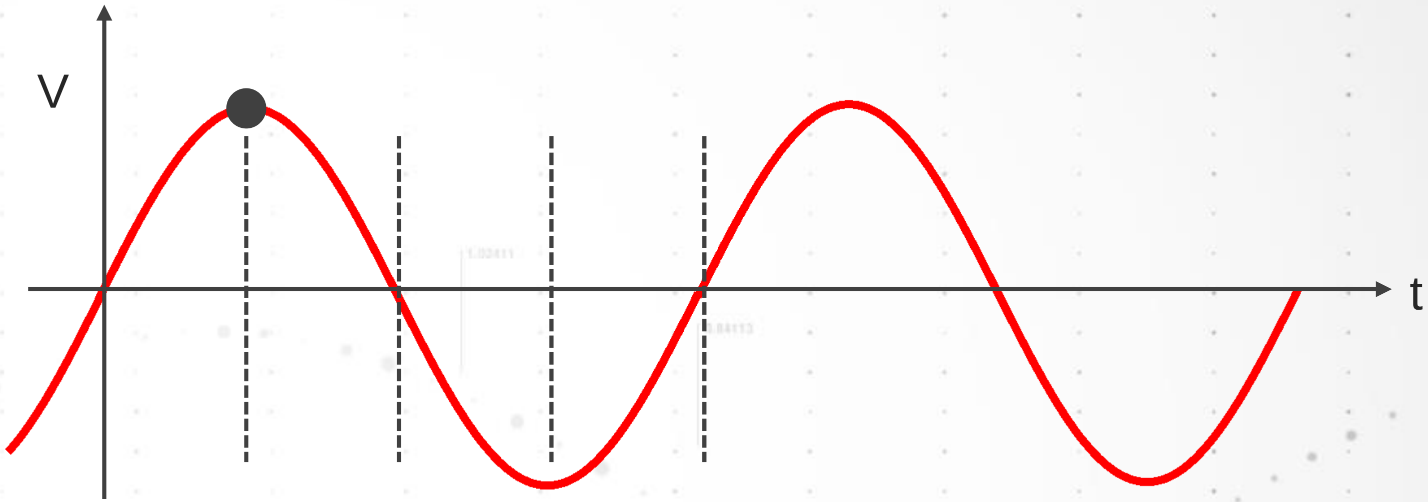


Transmission line stub

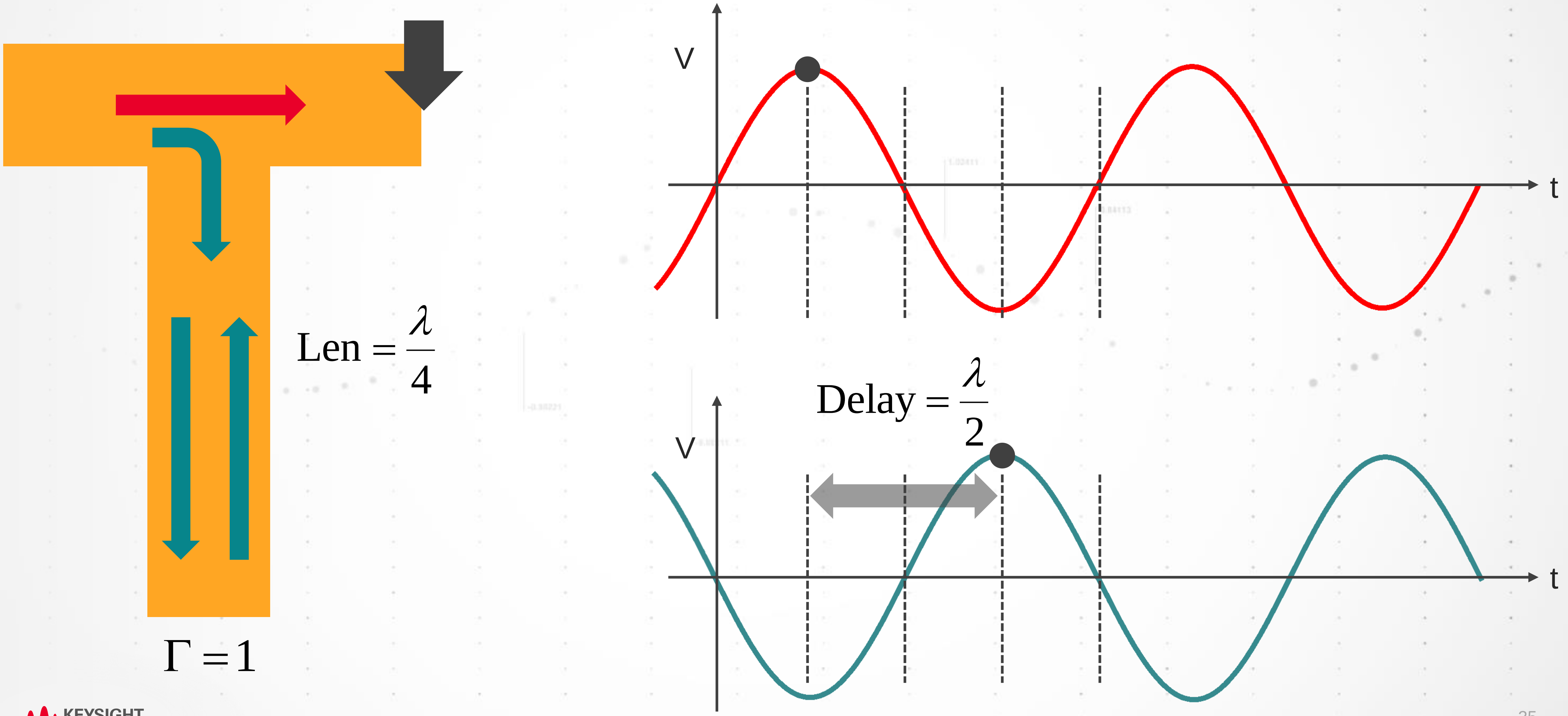
Open

Wave Propagation Path Not Through Stub

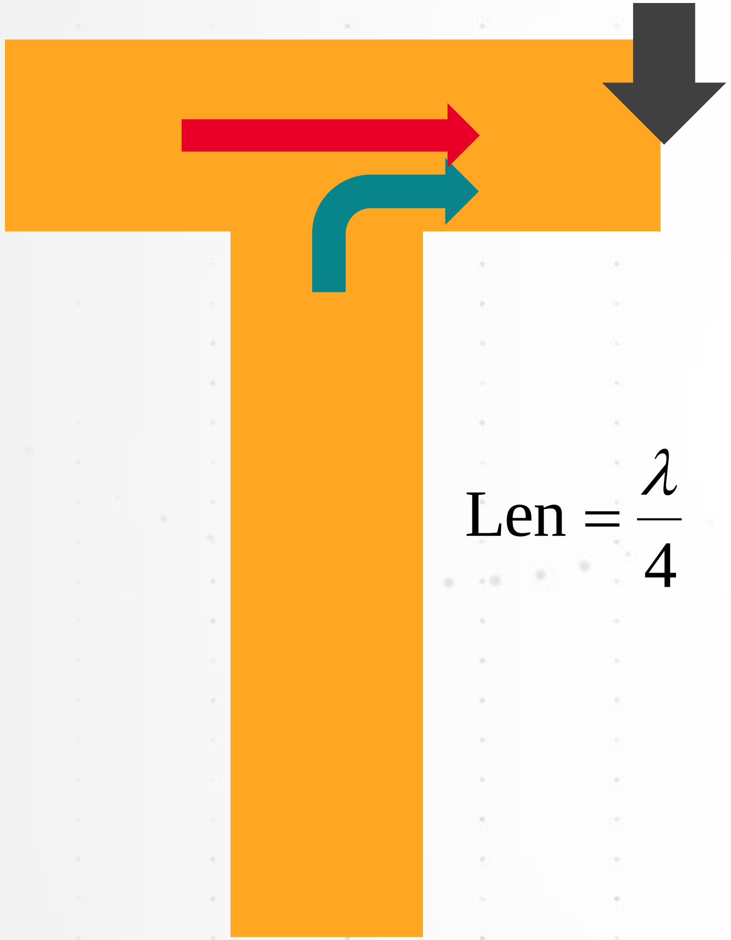




Wave Propagation in the Stub Direction

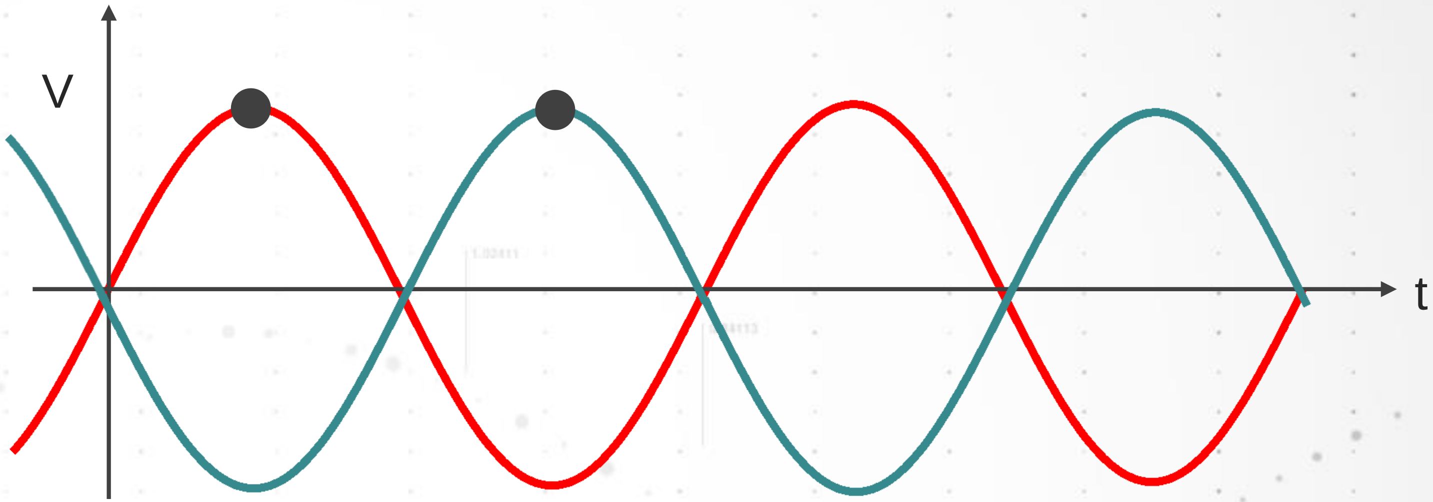


Quarter-wave Stub Resonance Minimizes Transmission



$$Len = \frac{\lambda}{4}$$

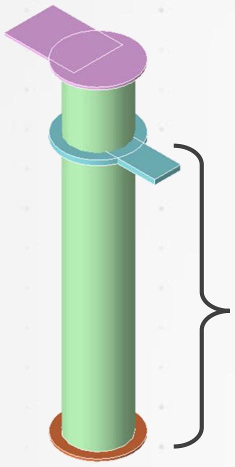
$$\Gamma = 1$$



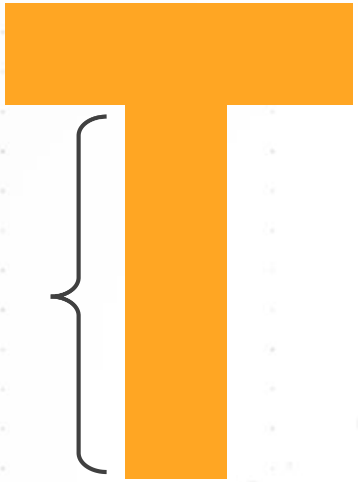
Quarter-wave stub resonance

At frequency where the physical length if the stub is a quarter of a wave length, it seems like nothing is being transmitted (virtual short).

Transmission Line Resonance Example



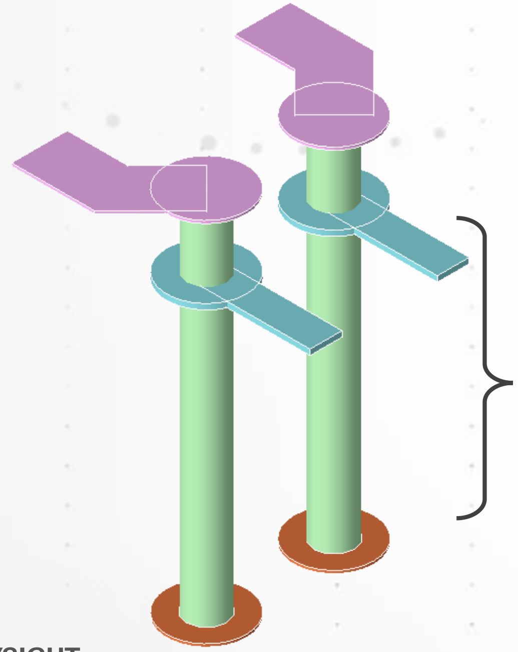
Len ~ 75 mil



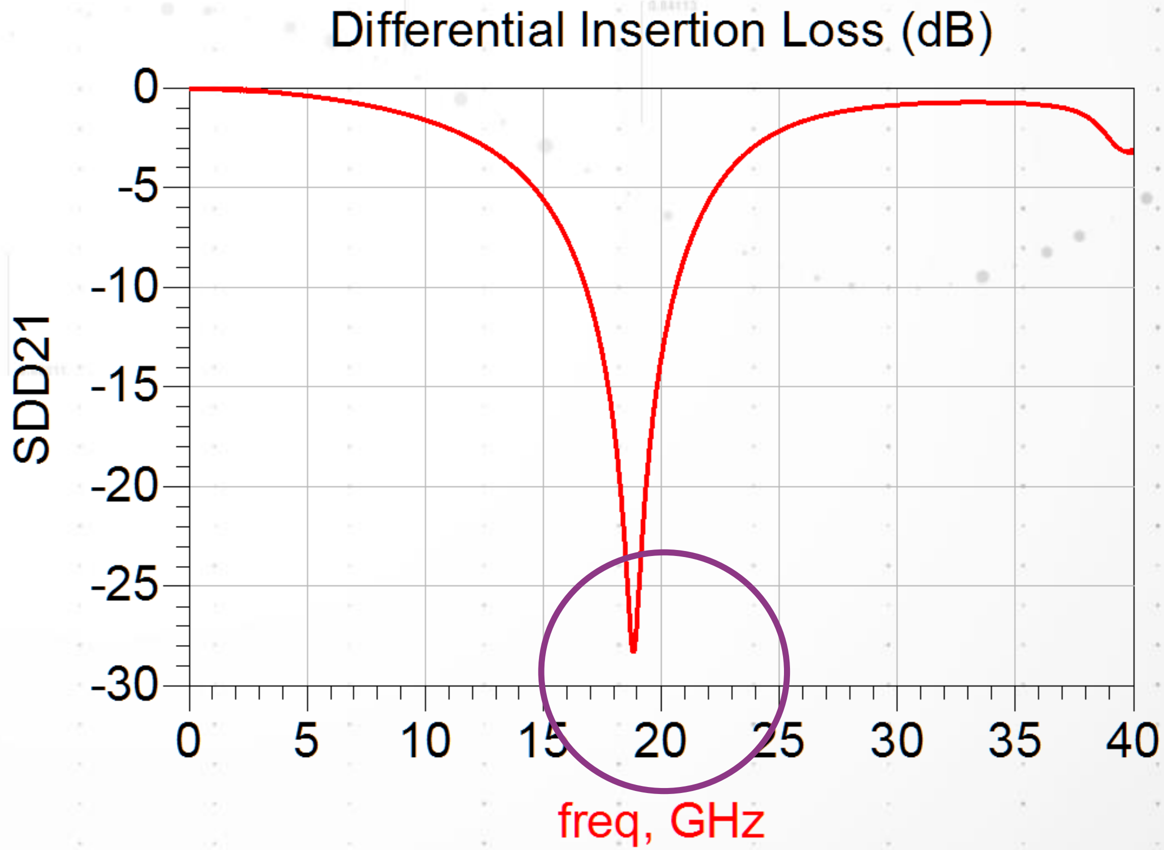
$$len = \frac{\lambda}{4} \rightarrow \lambda = 4 \cdot len \qquad f_{res} = \frac{v}{\lambda} = \frac{v}{4 \cdot len} \qquad v \simeq 6\,\frac{\text{in}}{\text{nsec}}$$

$$f_{res}(\text{GHz}) = \frac{1.5}{len\,(\text{in})}$$

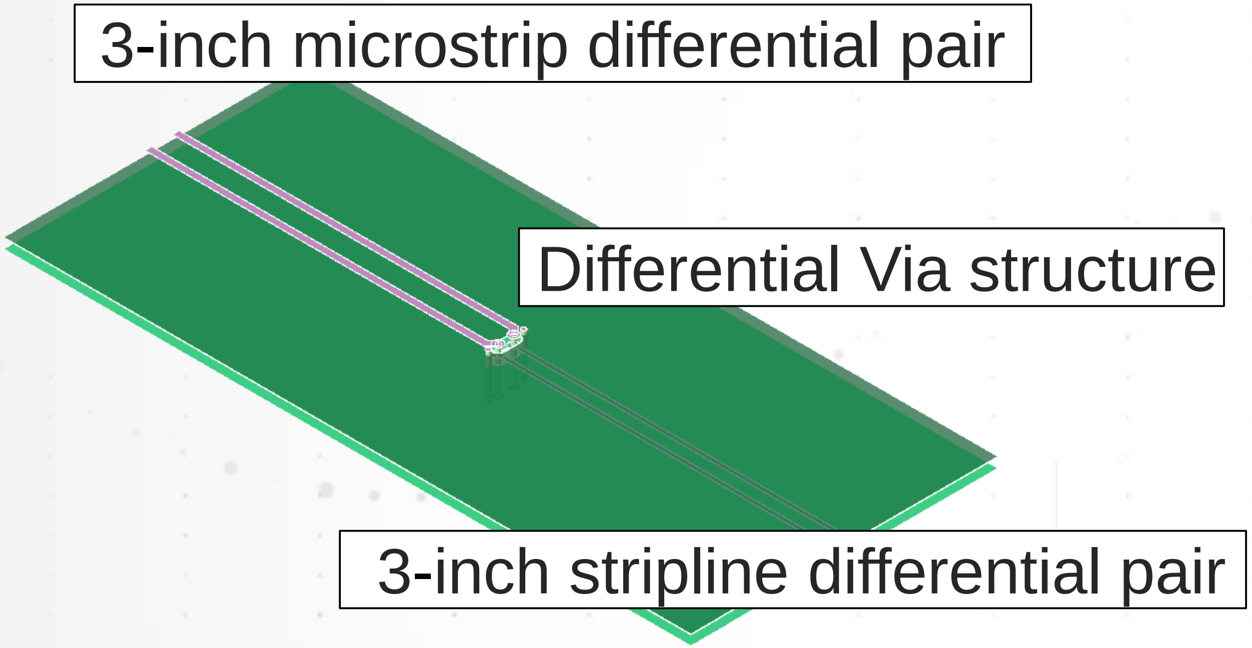
For FR4, expect f_{res} = 20 GHz

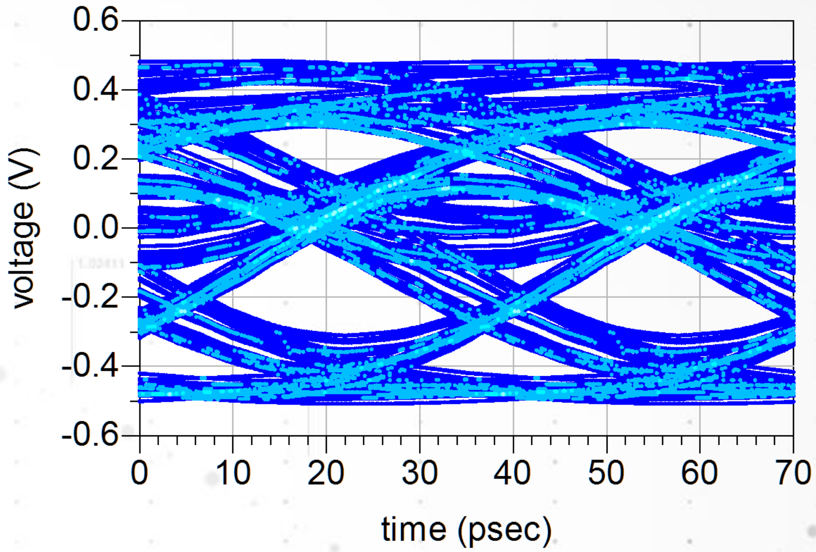


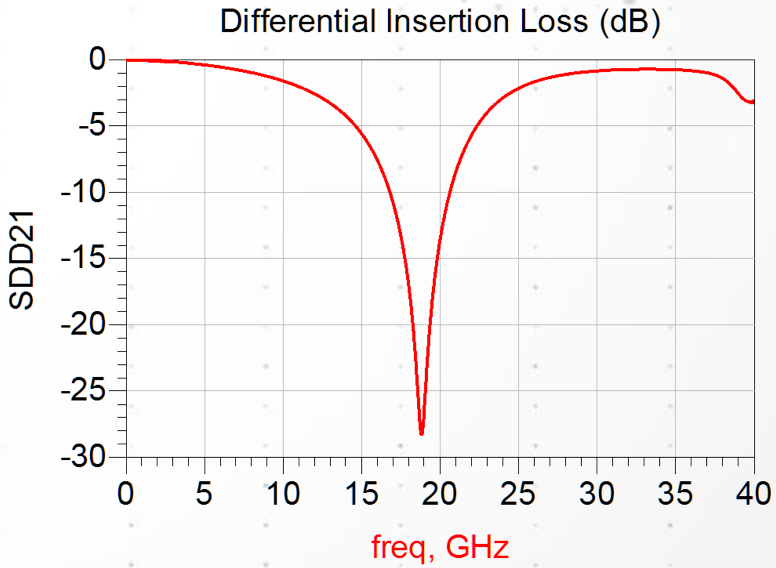
Len ~ 75 mil



The Stub Is a Possible Root Cause of Degradation



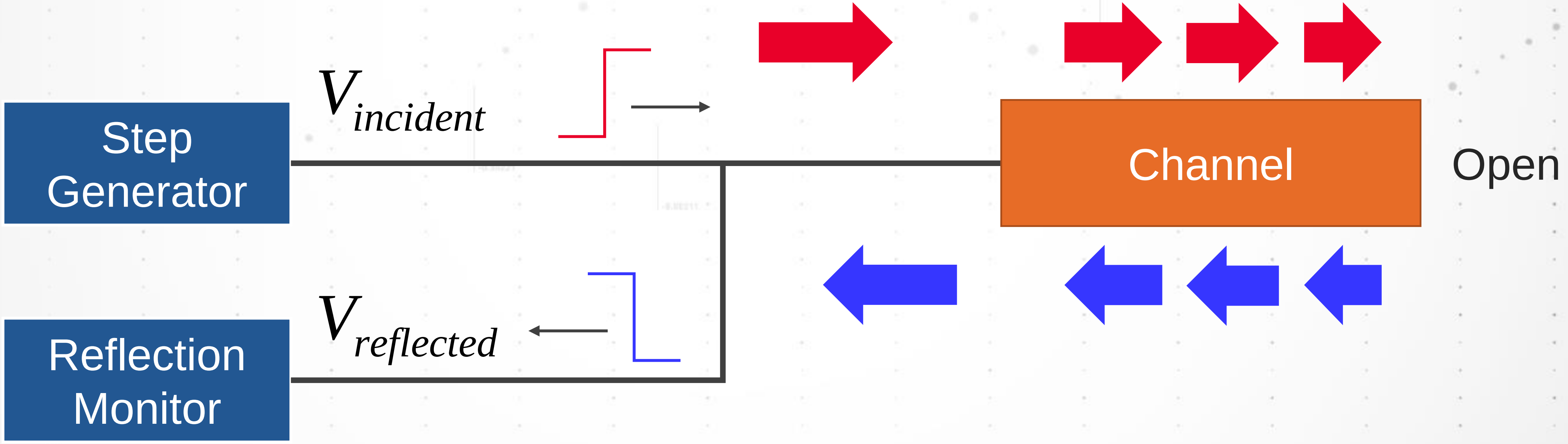




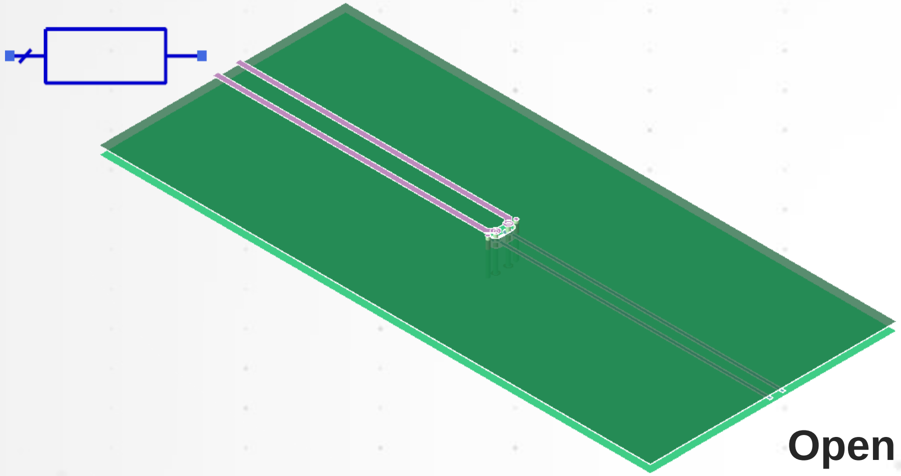
KEYSIGHT TECHNOLOGIES

Perform Consistency Test with TDR Impedance Plot

$$Z_{DUT}(t) = Z_0 \frac{1+\Gamma(t)}{1-\Gamma(t)} \qquad \Gamma(t) = \frac{V_{reflected}(t)}{V_{incident}(t)}$$



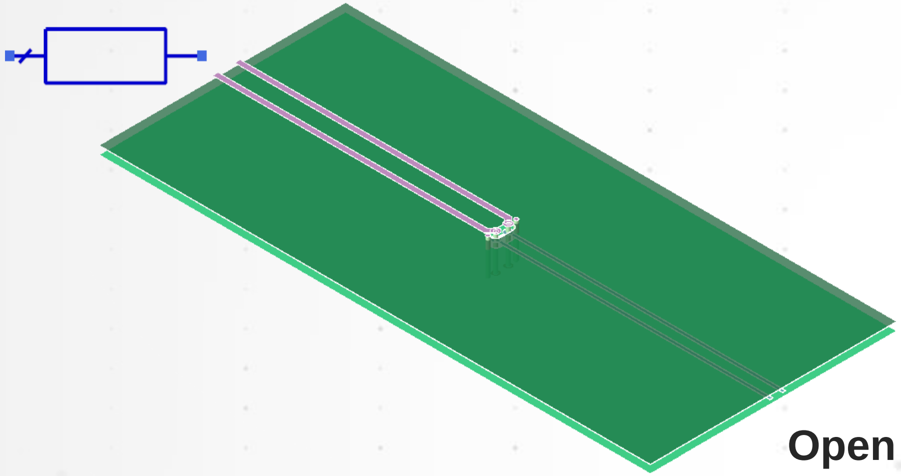
Expectation of Impedance Profile Before Simulation

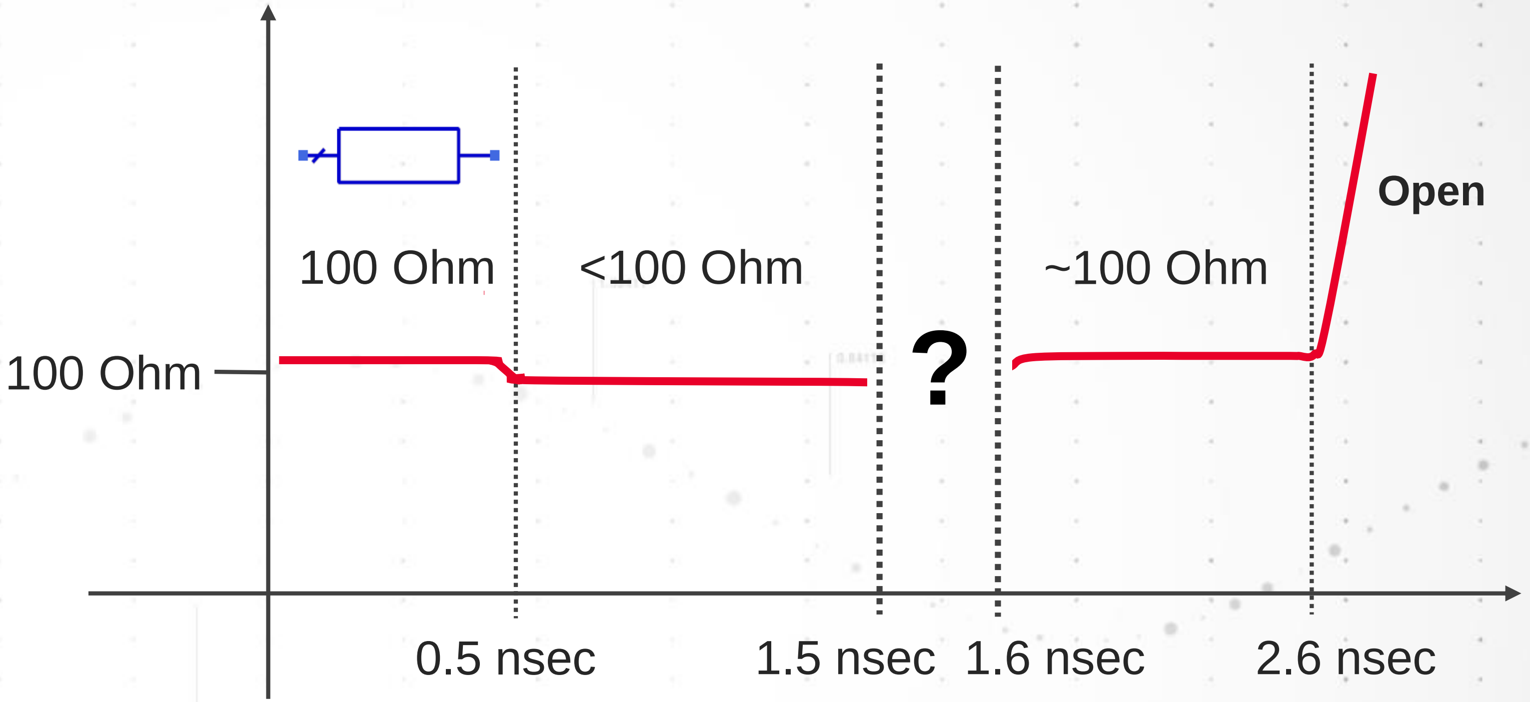


Estimated Delay (FR4): 6 in/nsec

Structure	3-inch microstrip	Via	3-inch stripline
Round Trip Delay (nsec)		Small	
Impedance (Ohm)	<100	?	~100

Expectation of Impedance Profile Before Simulation

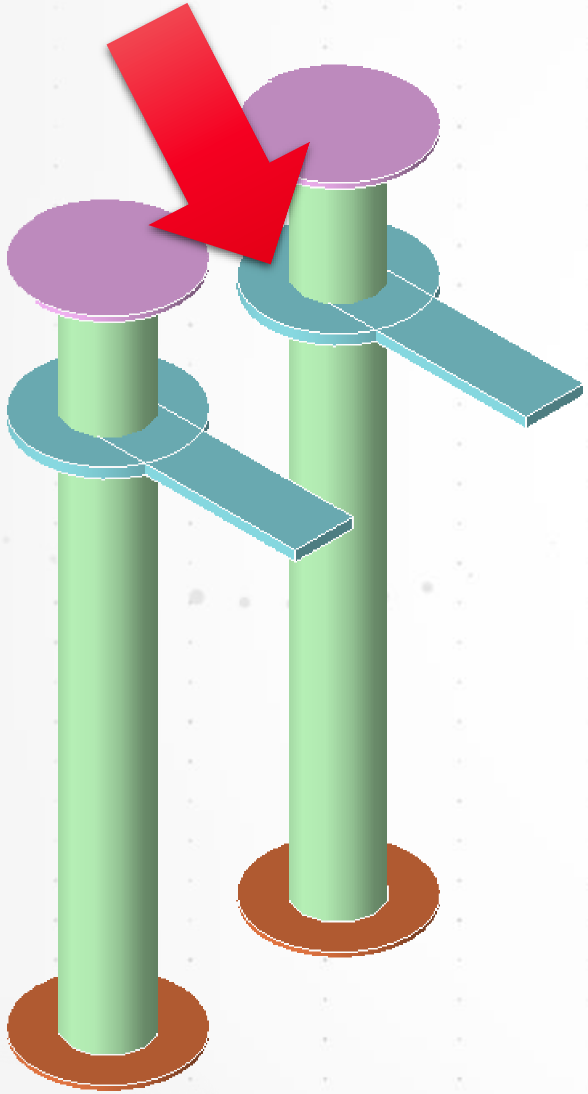


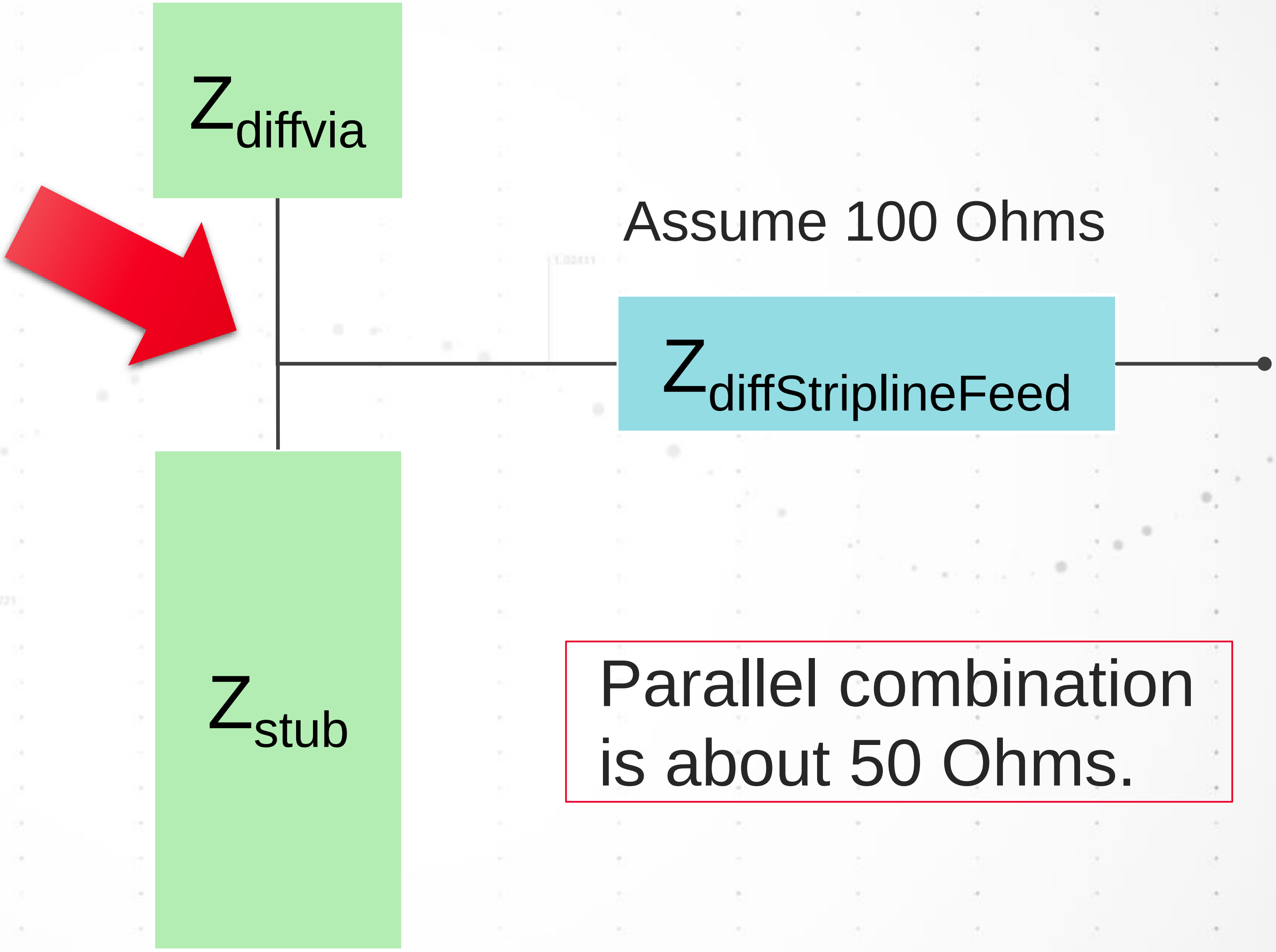


Estimated Delay (FR4): 6 in/nsec

Structure	3-inch microstrip	Via	3-inch stripline
Round Trip Delay (nsec)	1	Small	1
Impedance (Ohm)	<100	?	~100

Examine Via Structure to Estimate Impedance



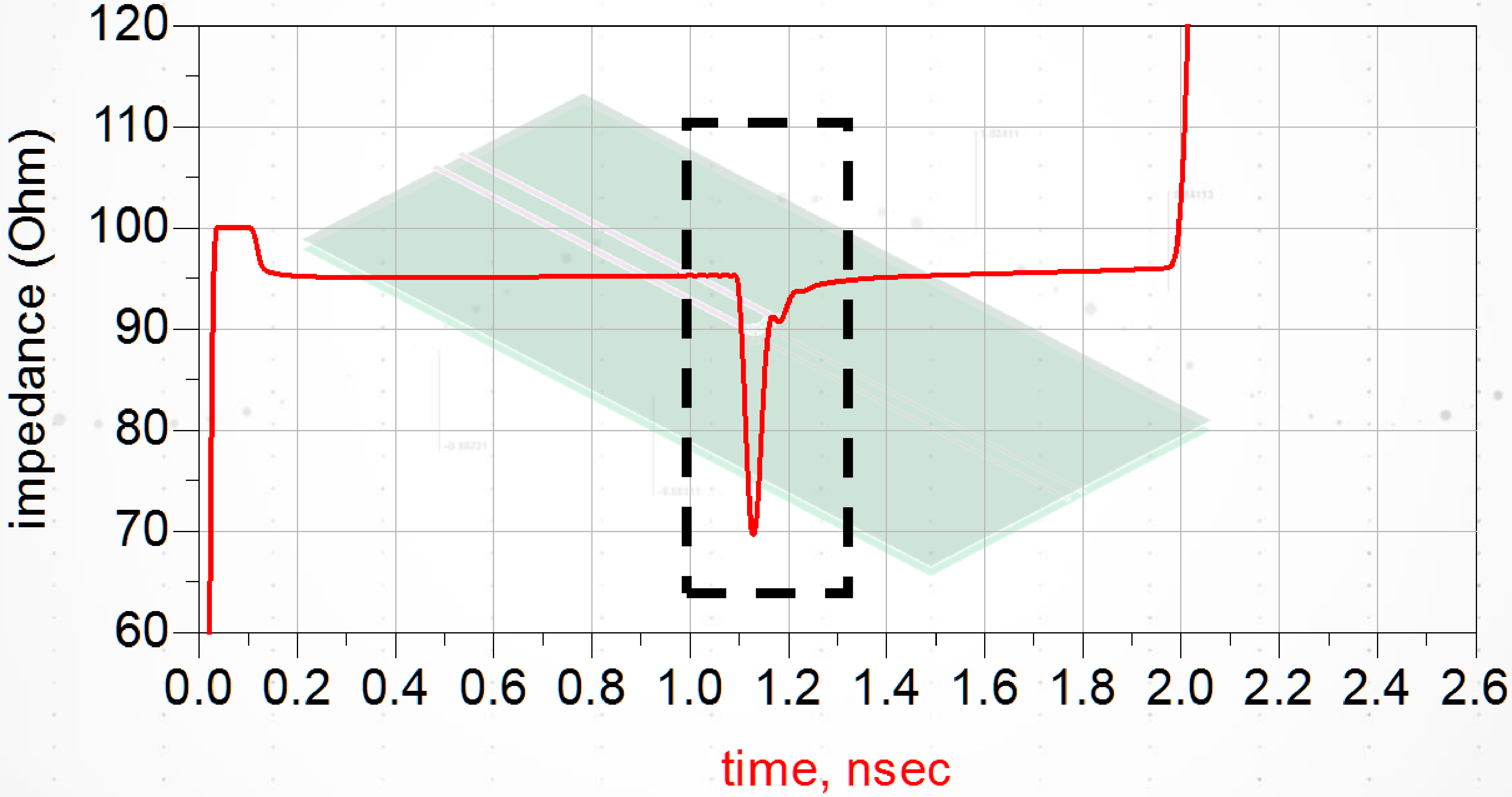


Assume 100 Ohms

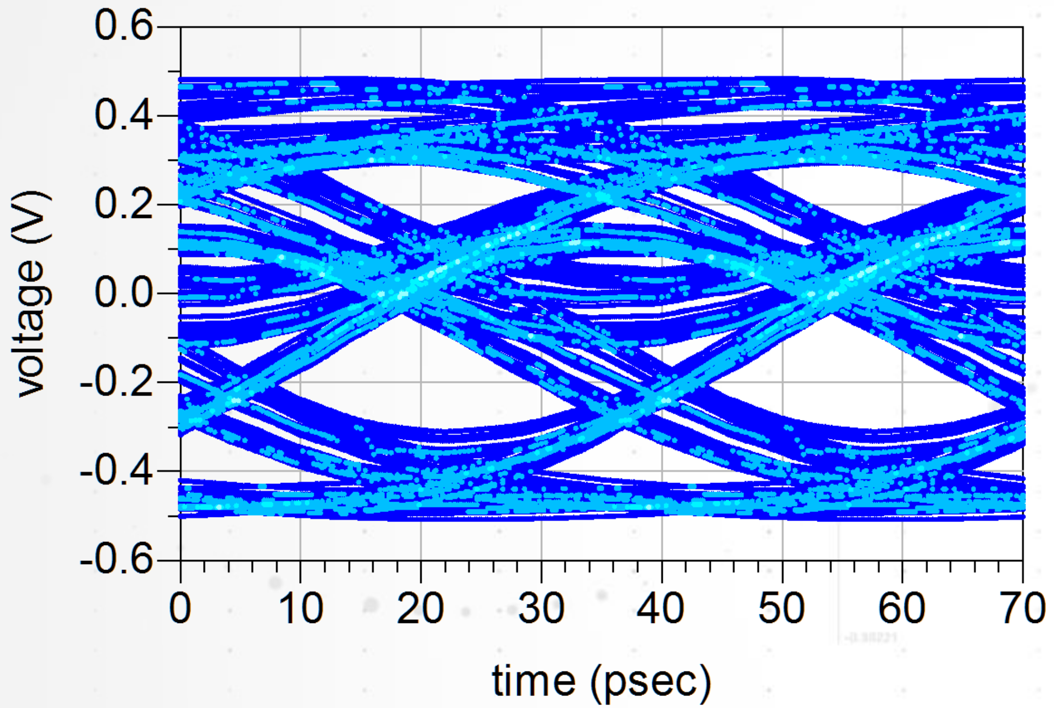
Assume 100 Ohms

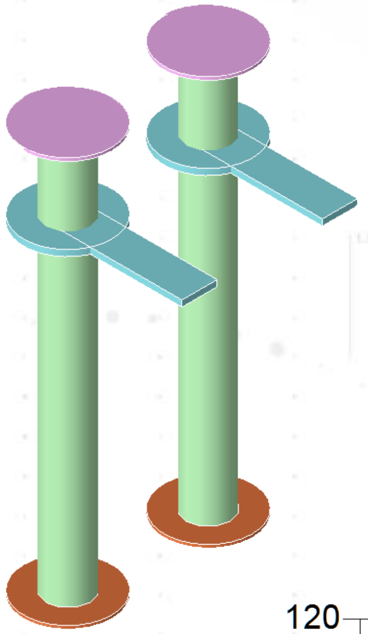
Parallel combination is about 50 Ohms.

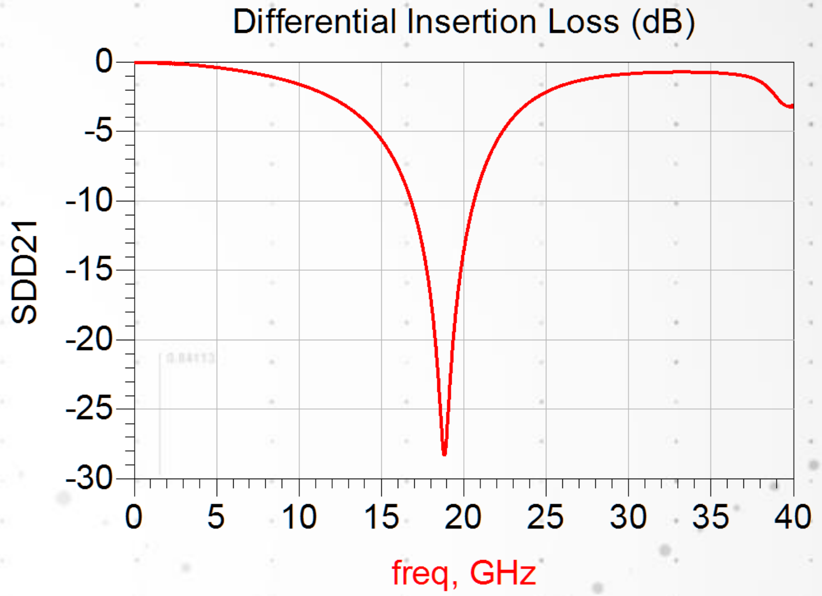
Low Impedance Shown in TDR is Consistent



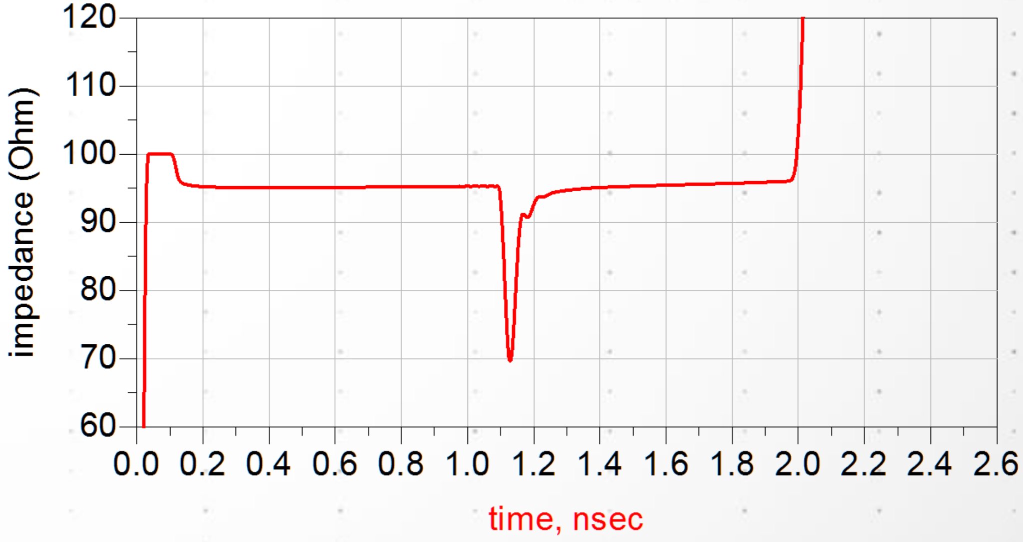
Via Stub is The Root Cause of Eye Closure





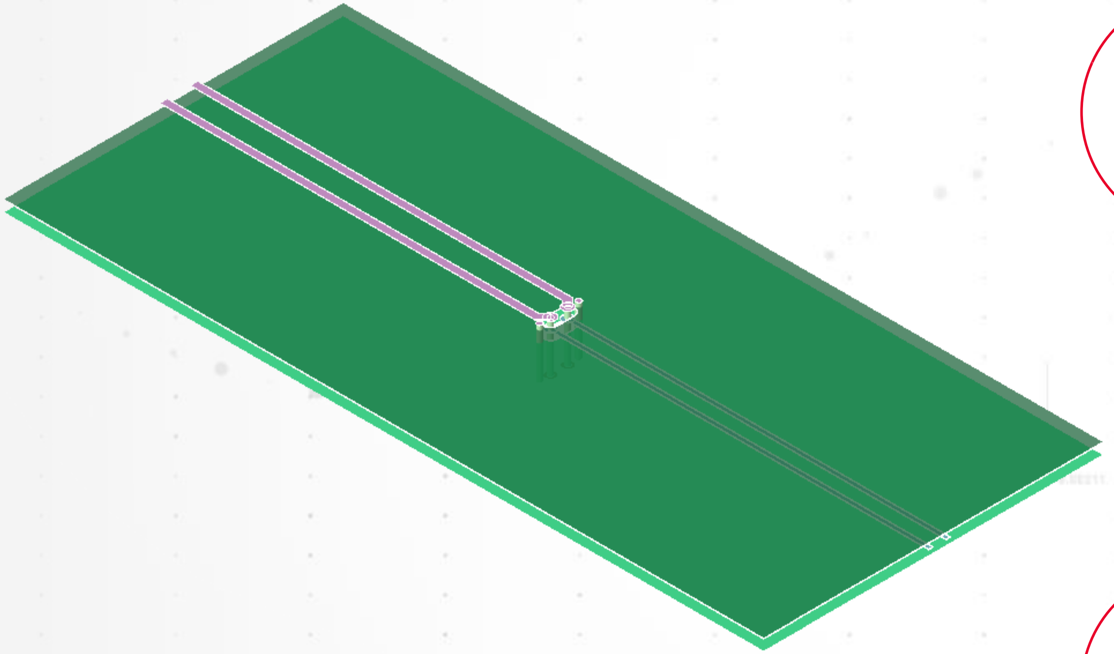


<u>The Root Cause:</u>
The via stub is resonating at frequency close to Nyquist and degrading the frequency spectrum of the input signal.



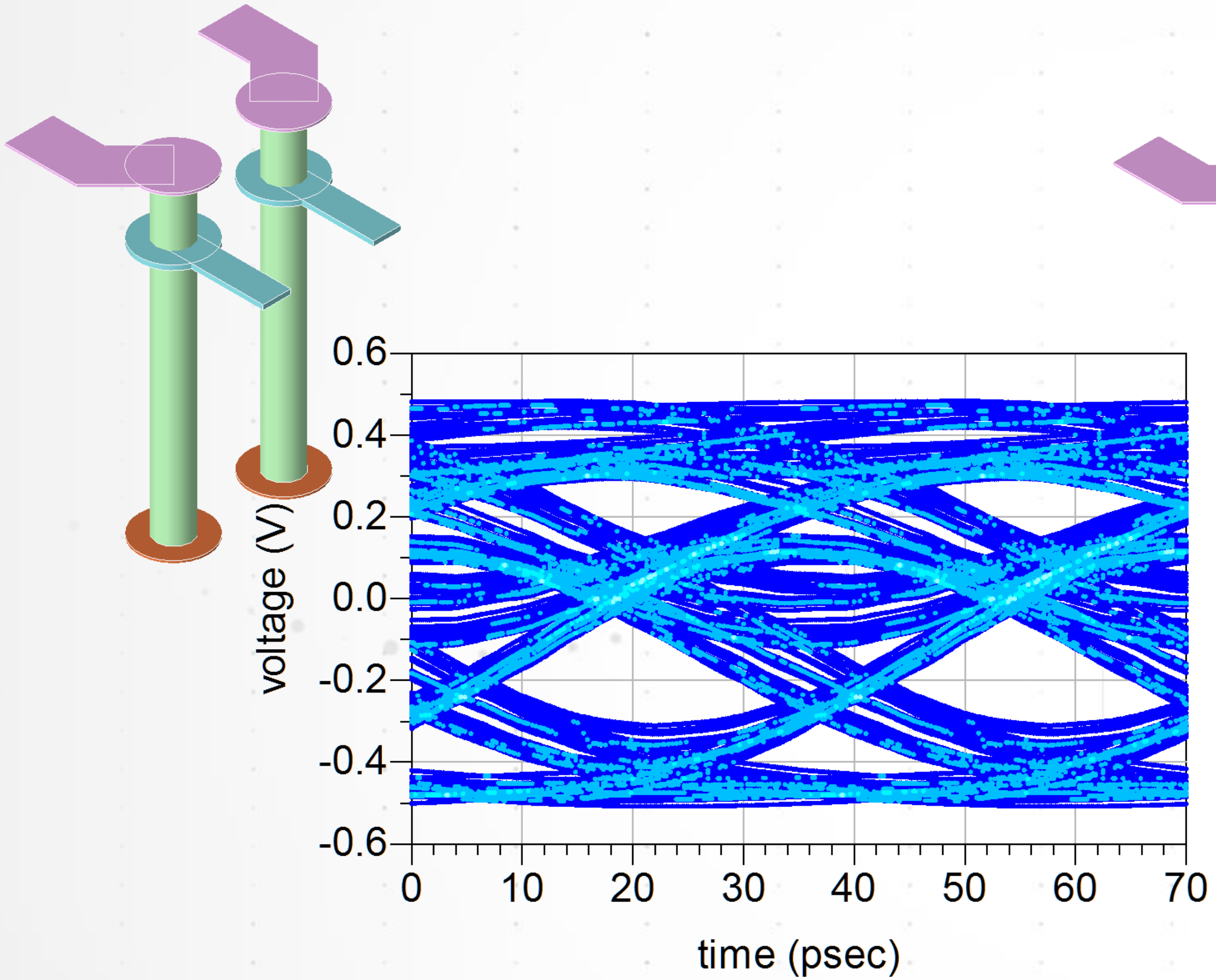
Understand Signal Integrity Analyses with a Case Study

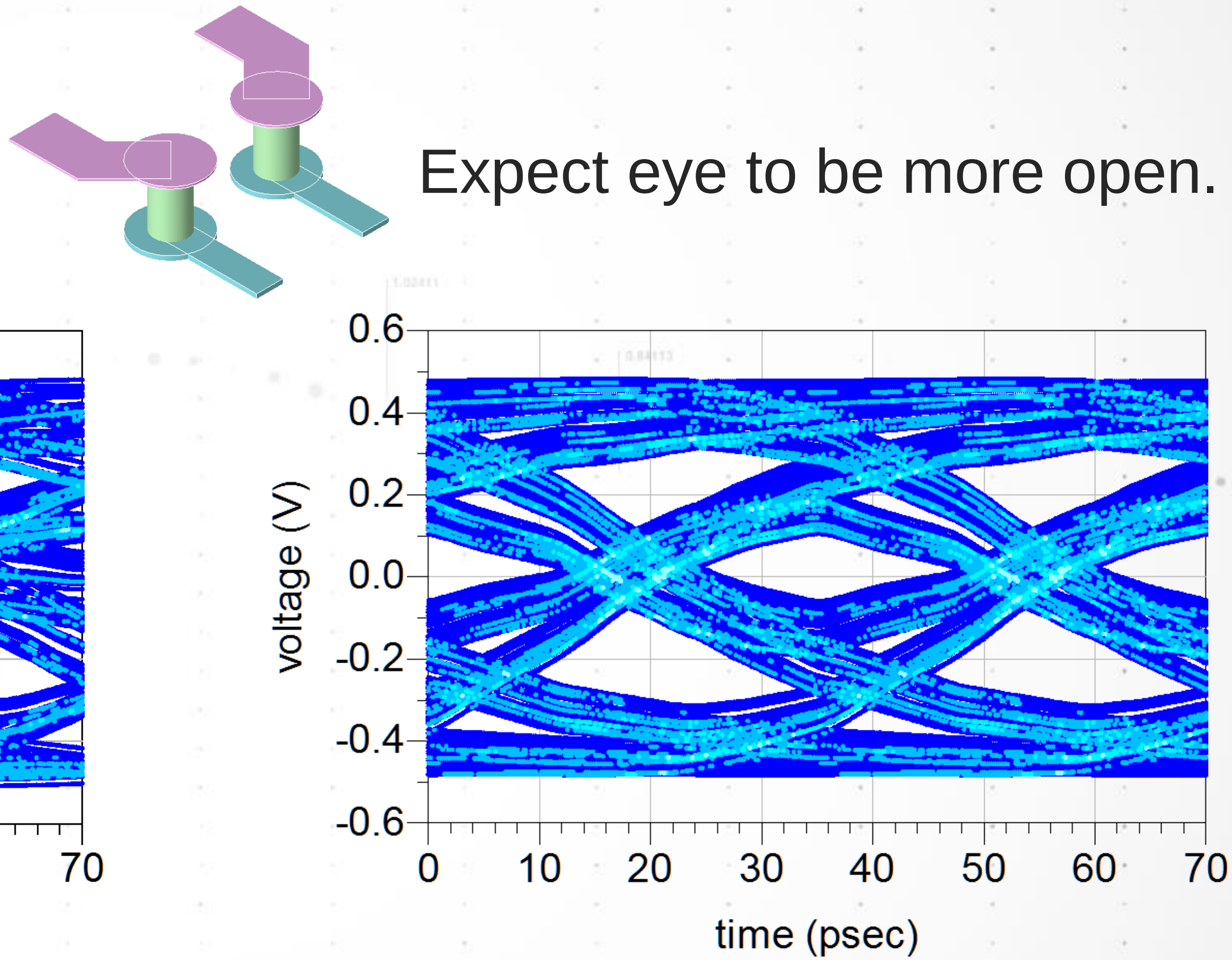
The case of the failing virtual channel



1. Simulate the channel
2. Find the root cause of degradation
3. Explore design solutions

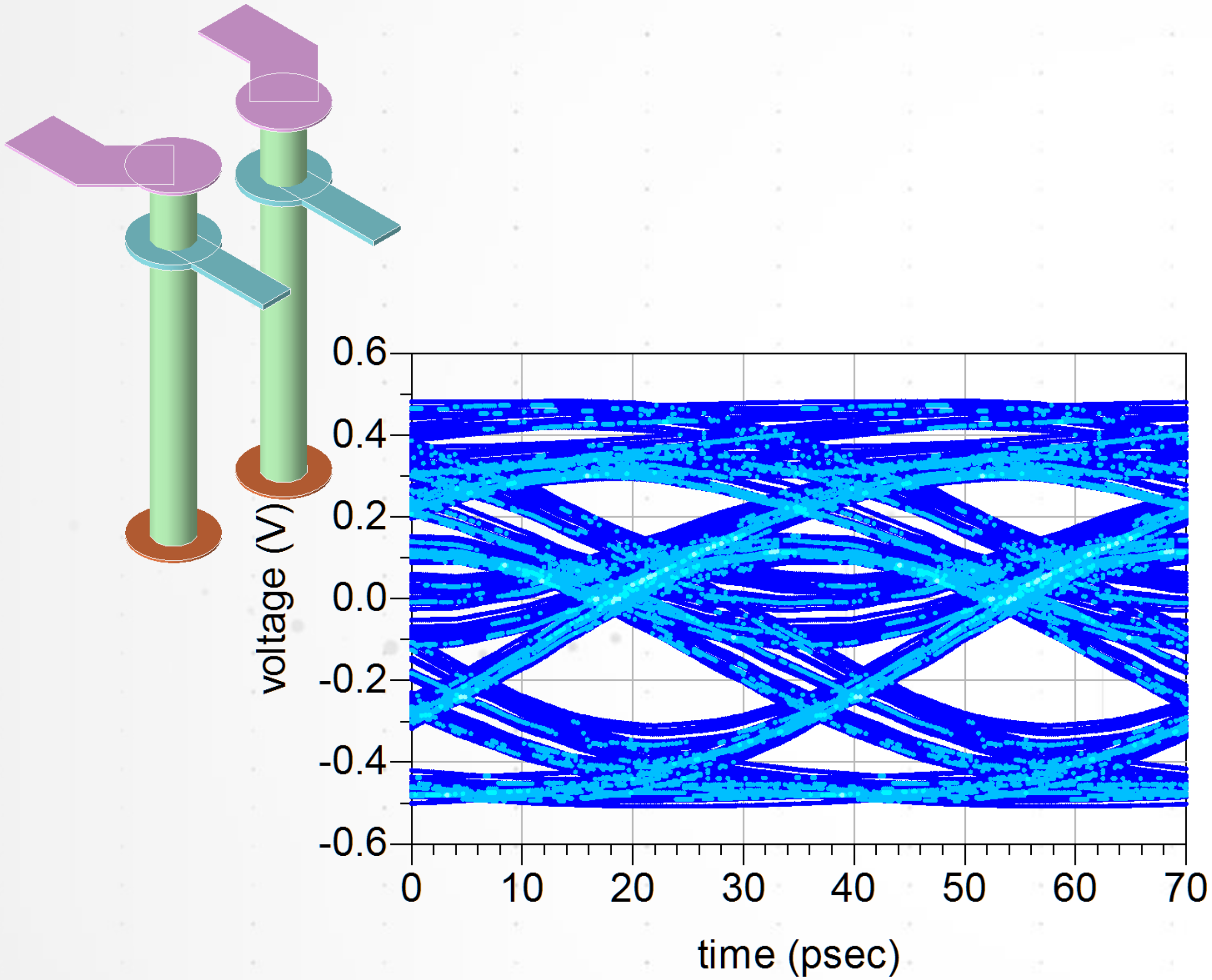
Solution 1: Remove Stub with Back-drilling





Expect eye to be more open.

Solution 2: Add Equalization at the Receiver



Decision Feedback

+ Equalization

But… How many taps?

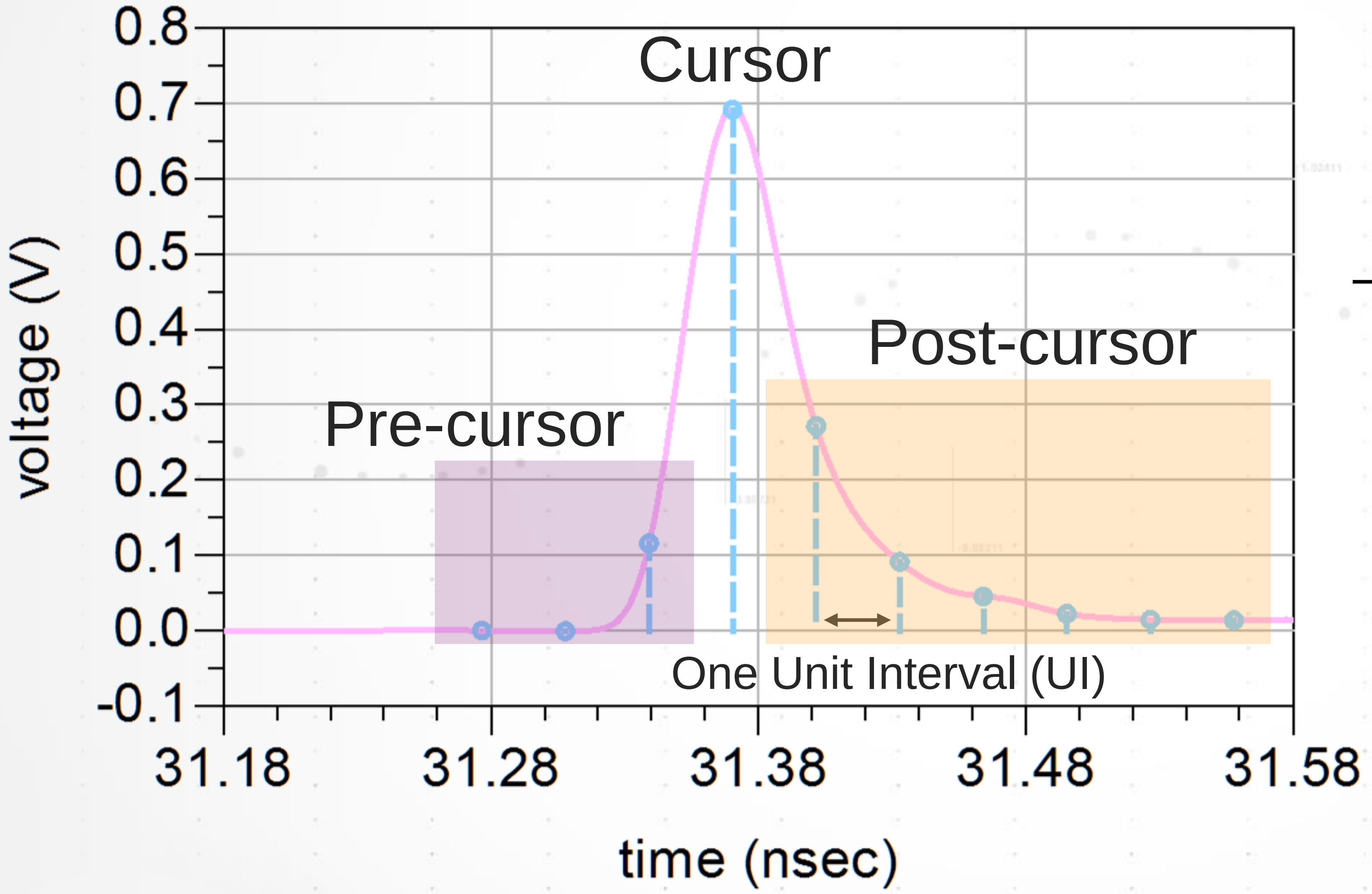
Use Single Pulse to Identify Number of Taps Needed

Single pulse

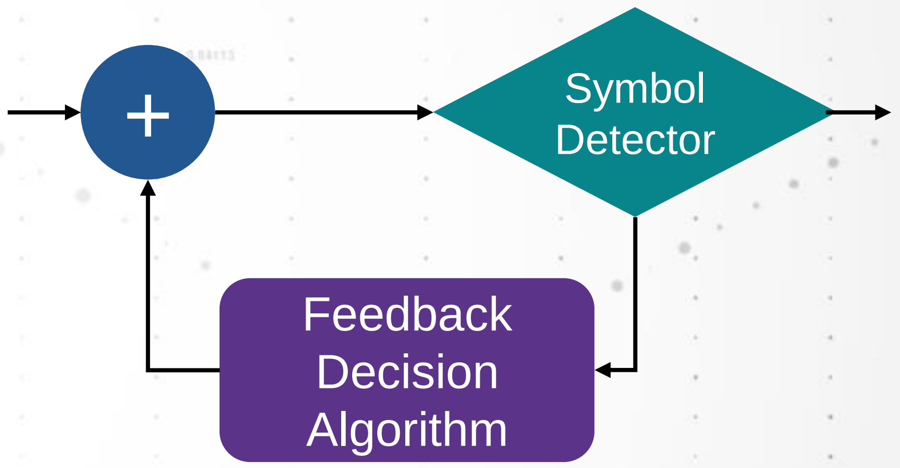
Single pulse response

- Rise Time
- Data rate (Unit Interval)

Select Number of Taps for Decision Feedback Equalization

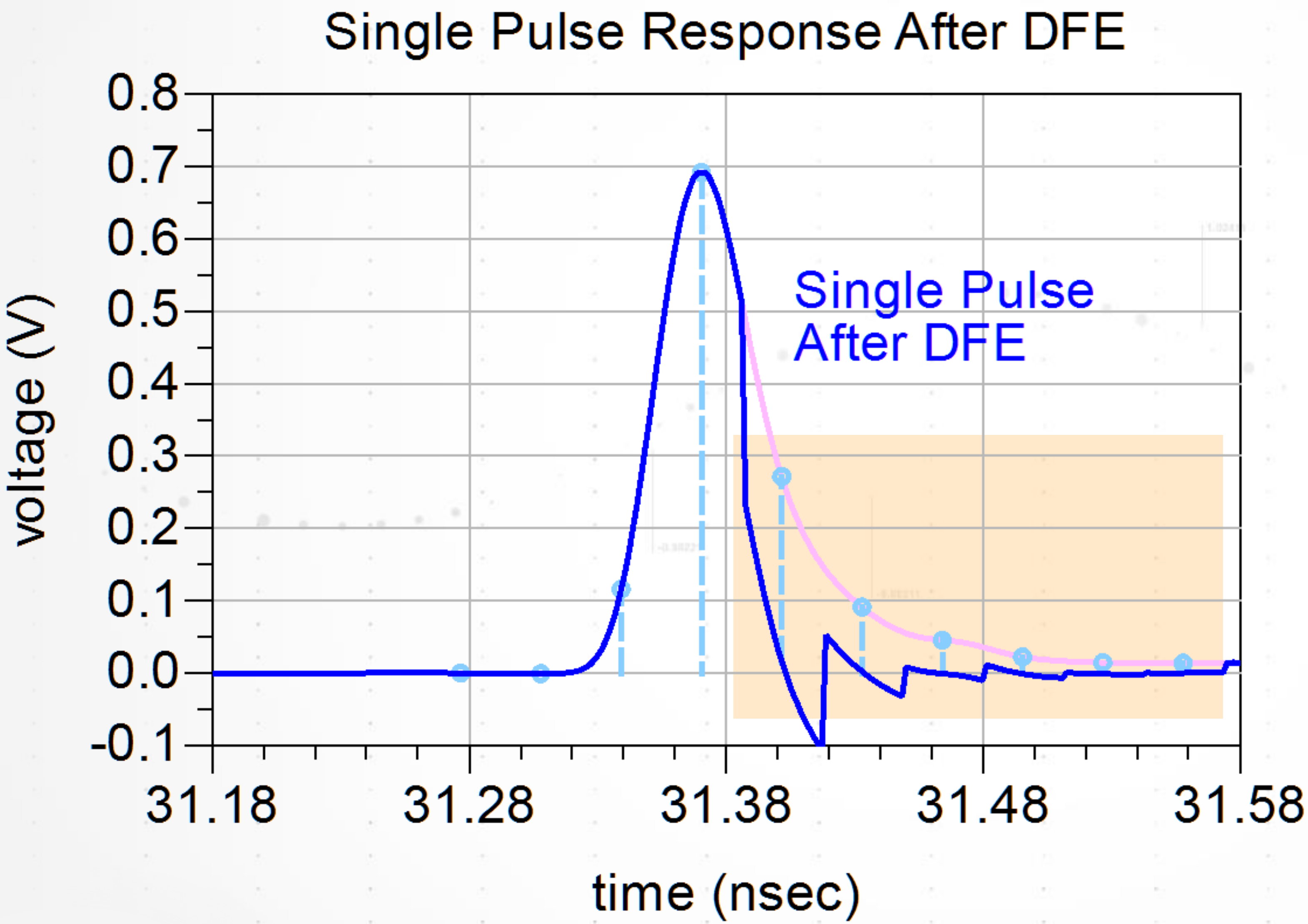


Decision Feedback Equalization



If I detect a “1”, emphasize the next “0”.

Decision Feedback Equalization in Time Domain

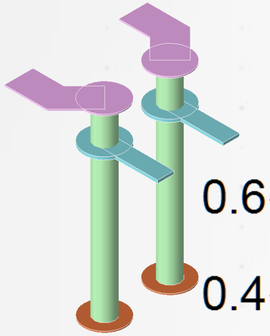


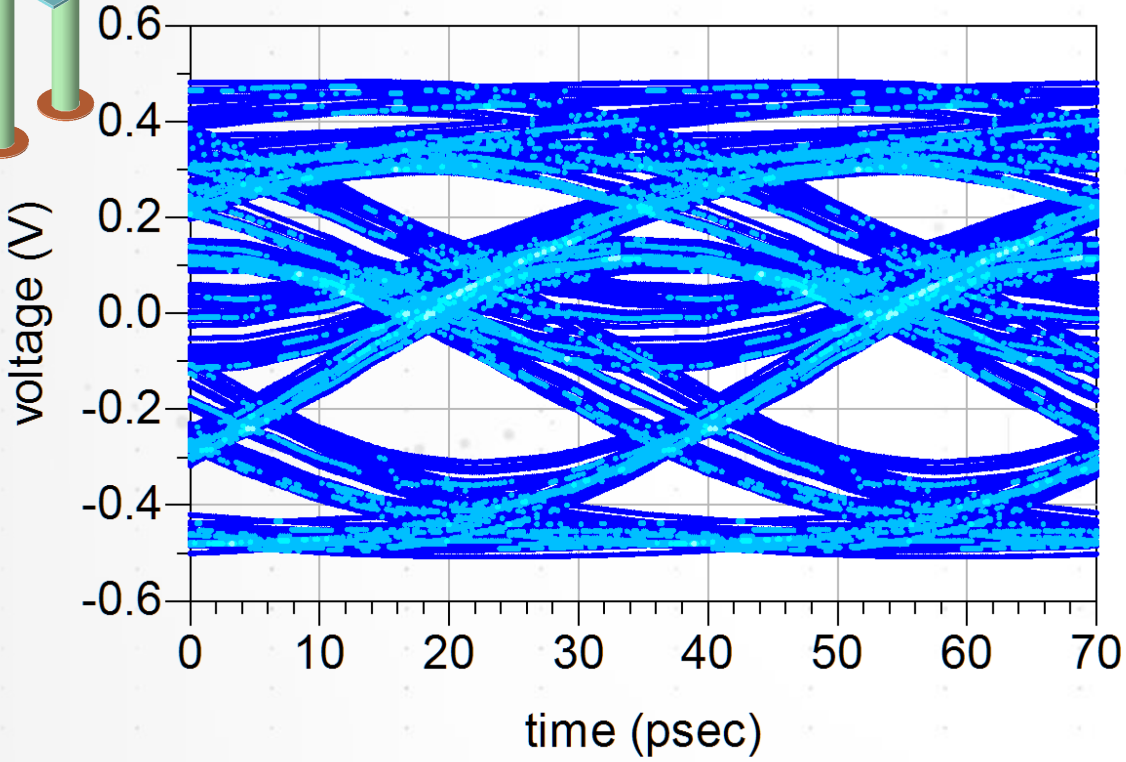
If I detect a “1”, emphasize the next “0”.

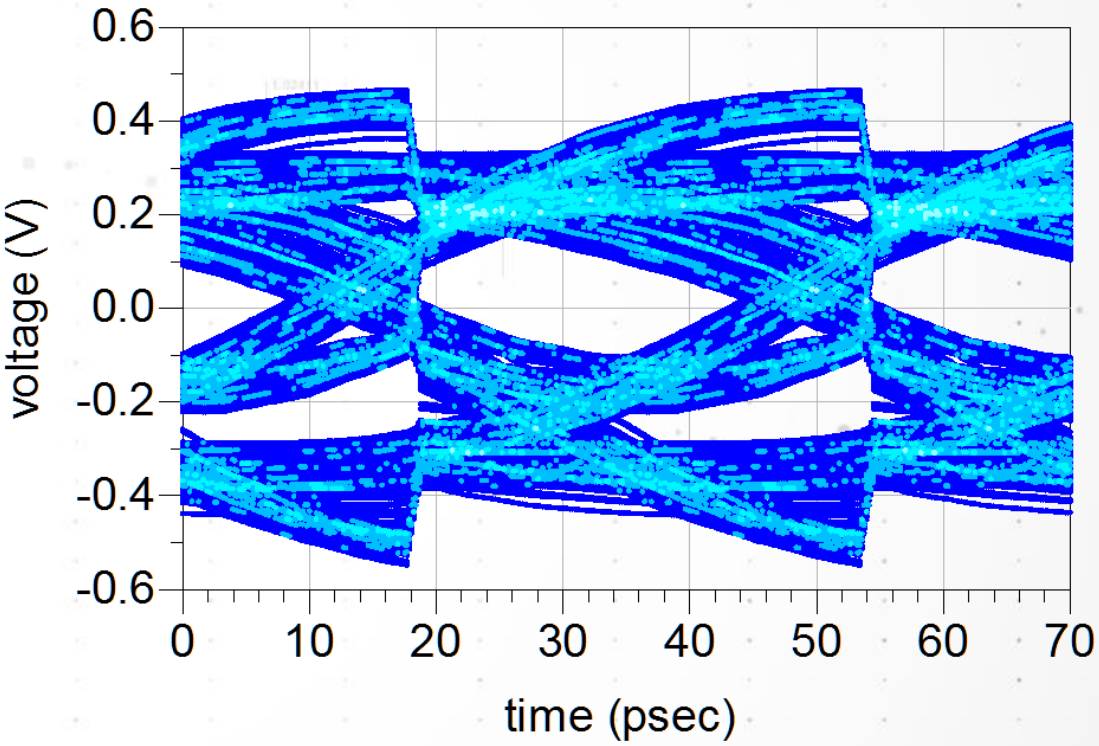
Solution 2: Add Equalization at the Receiver

Decision Feedback

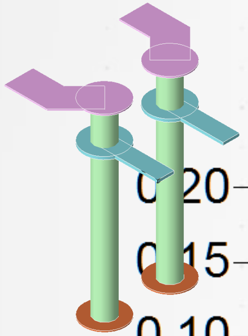
+ Equalization

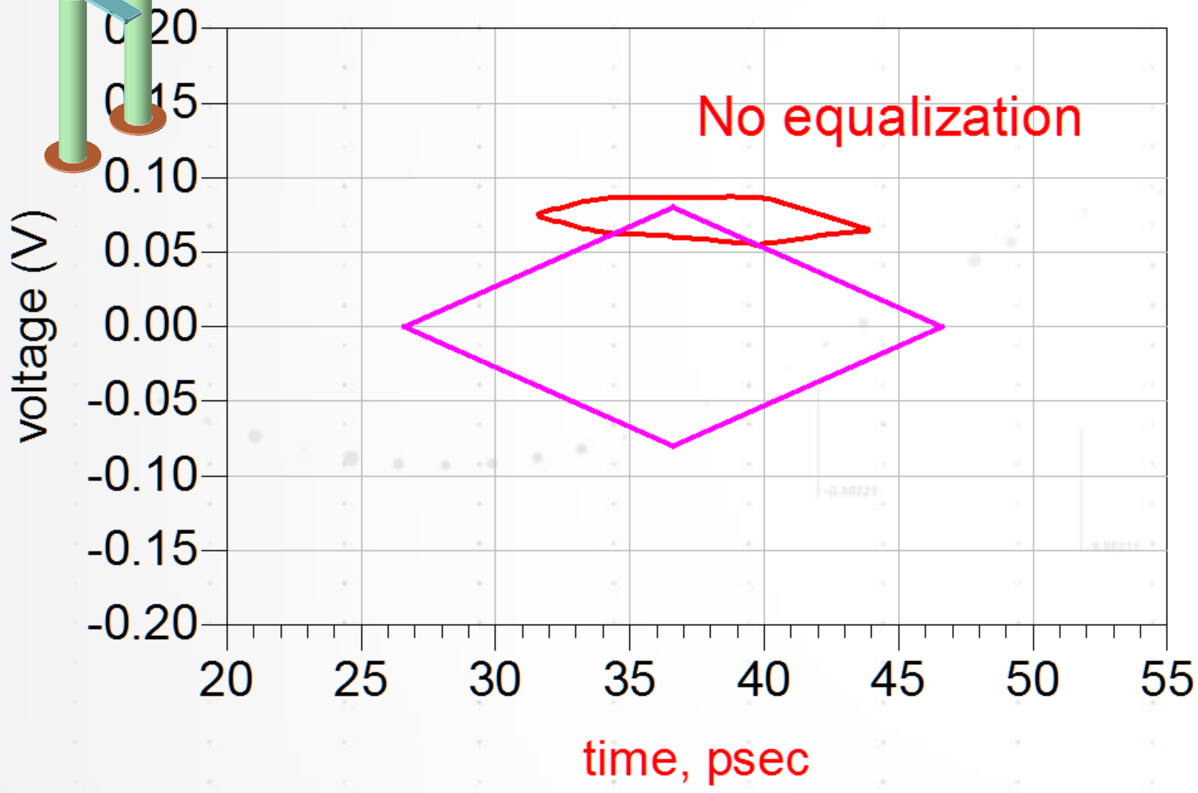


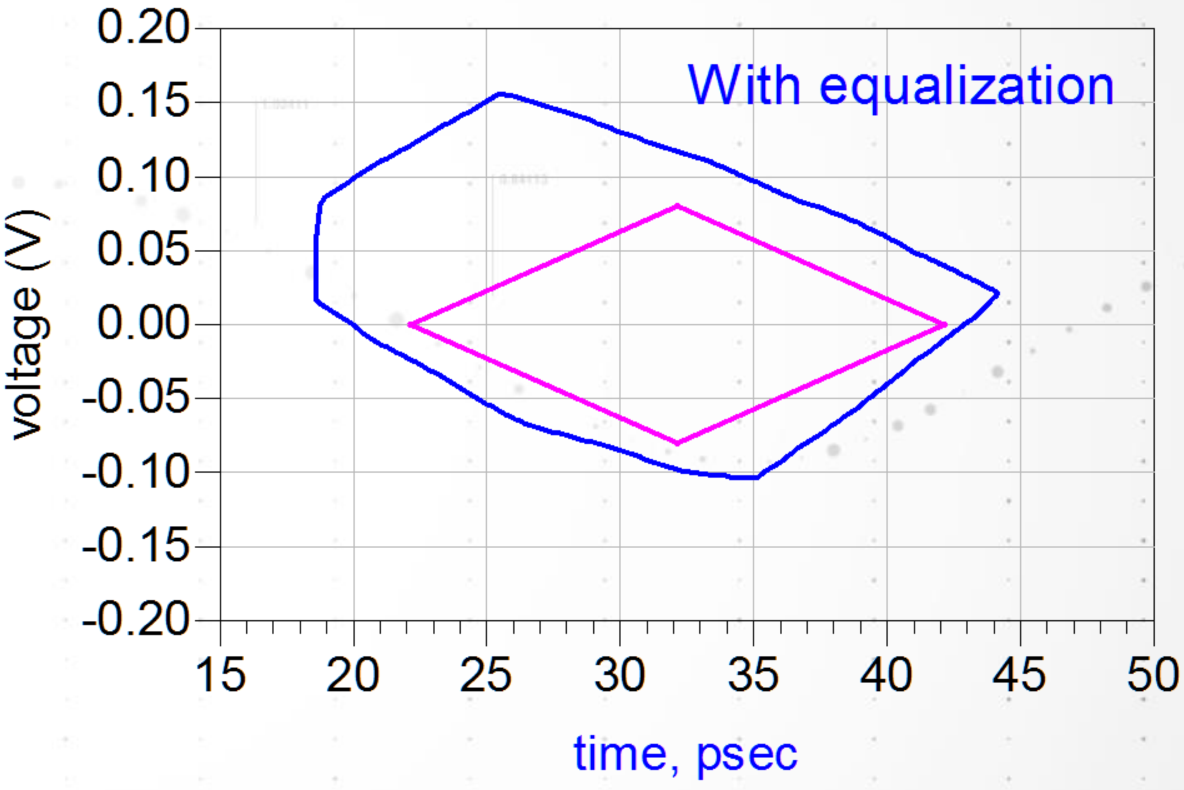




Eye Mask Comparison Before and After DFE

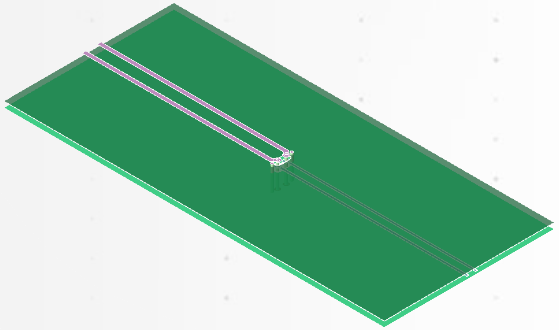


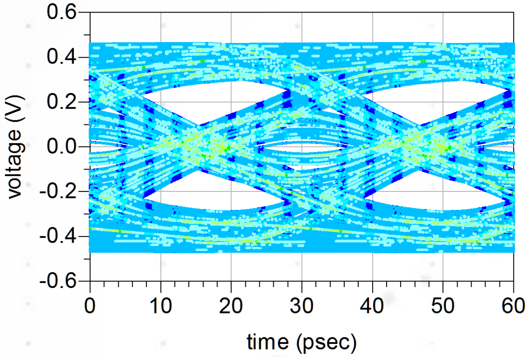


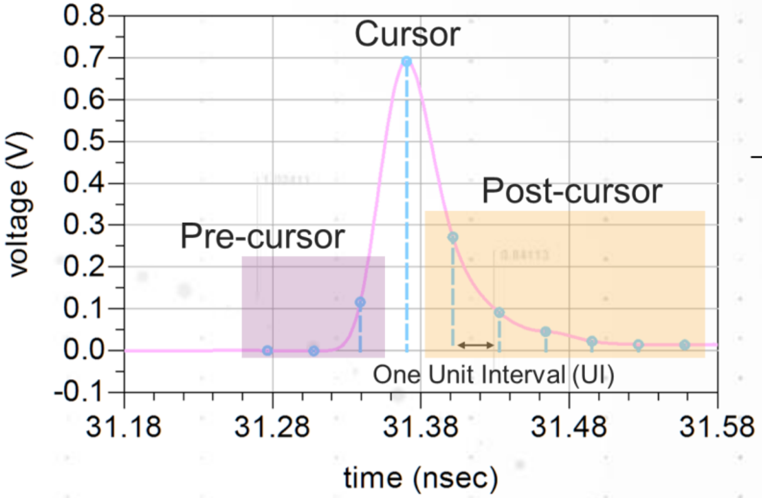


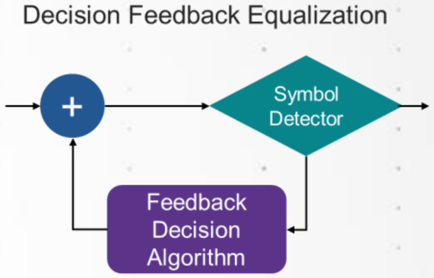
Understand Signal Integrity in the Ideal World

The case of the failing virtual channel

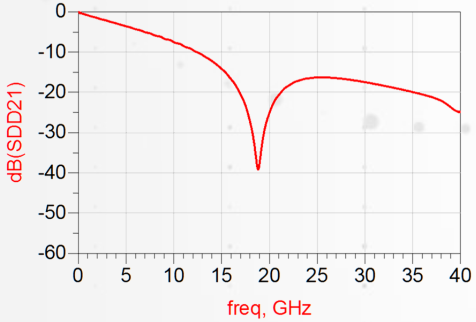


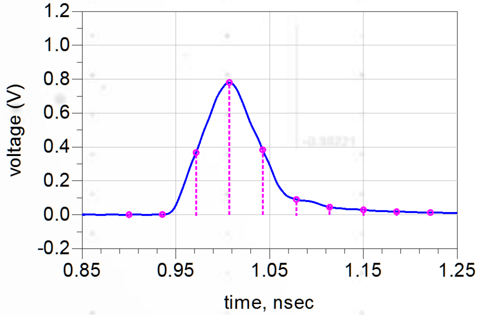


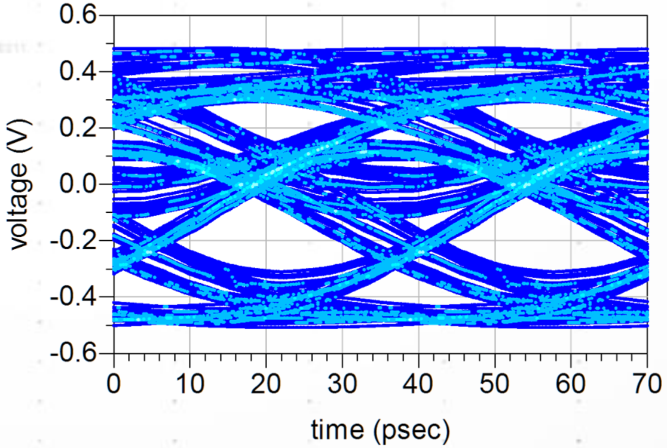


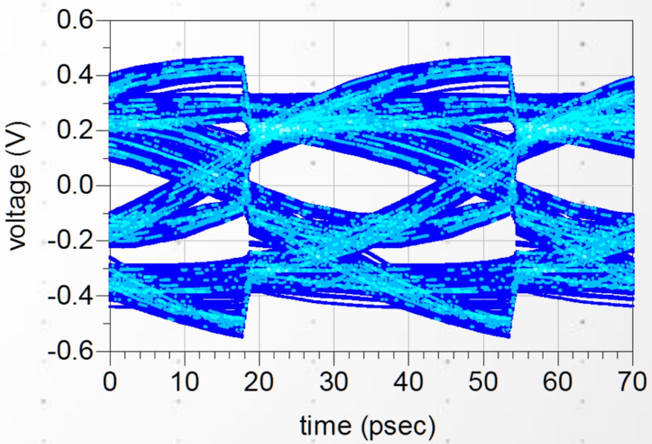


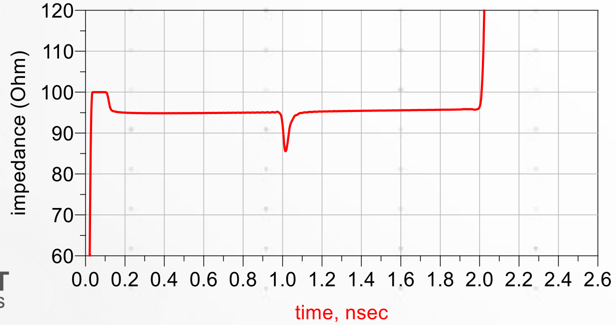
If I detect a "1", emphasize the next "0".









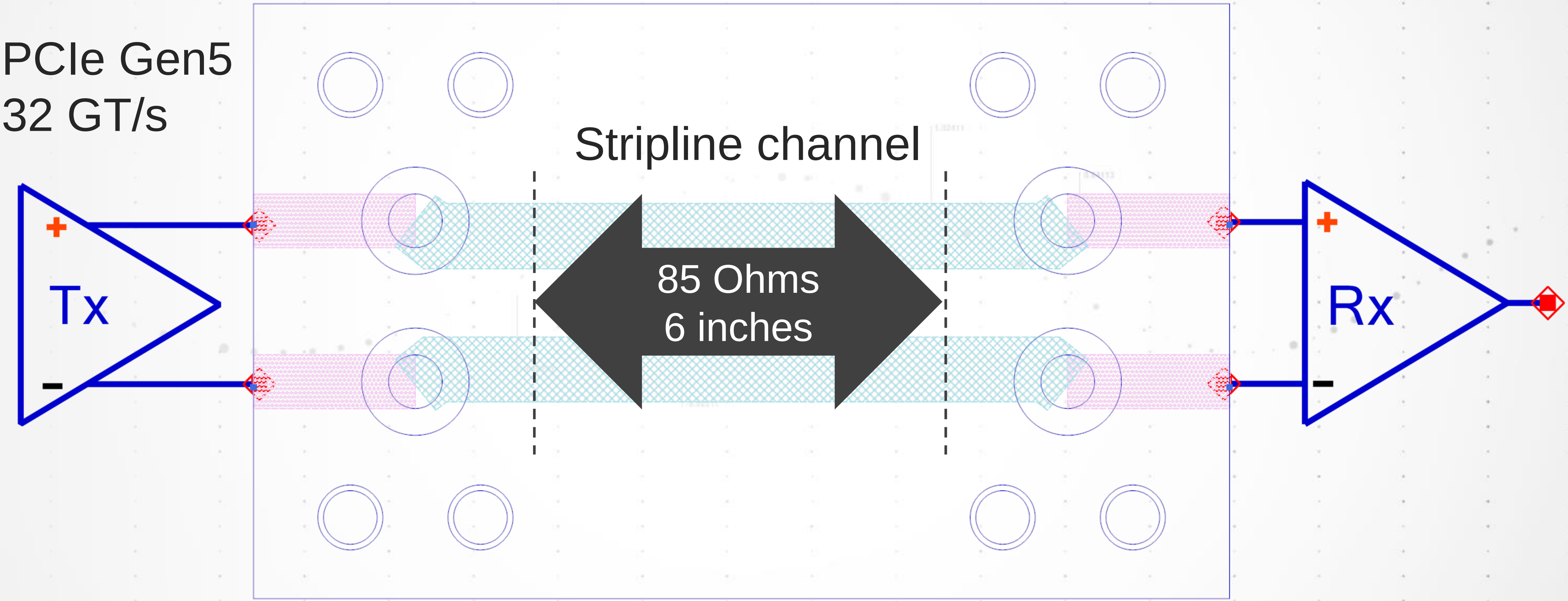


KEYSIGHT TECHNOLOGIES

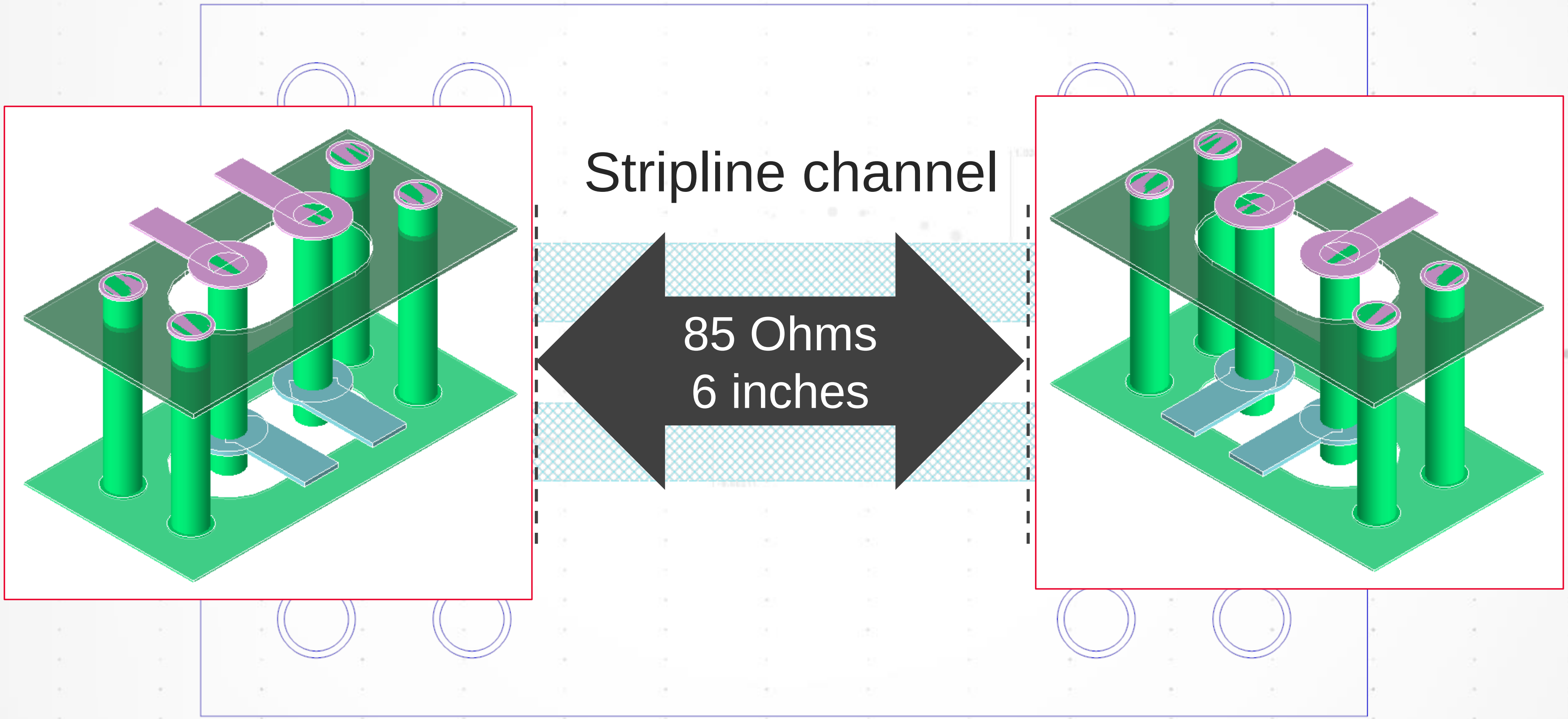
ADS Essential Signal Integrity Analysis Demo

PCIe Example: Simulate a Differential Channel

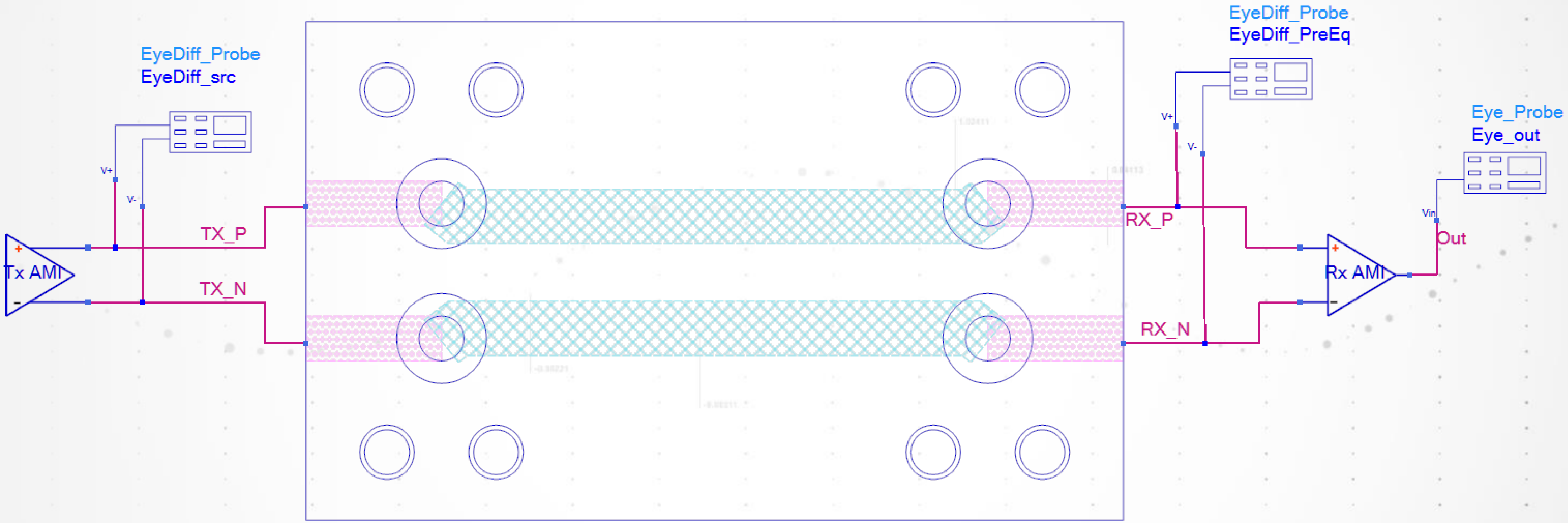
PCIe Gen5
32 GT/s



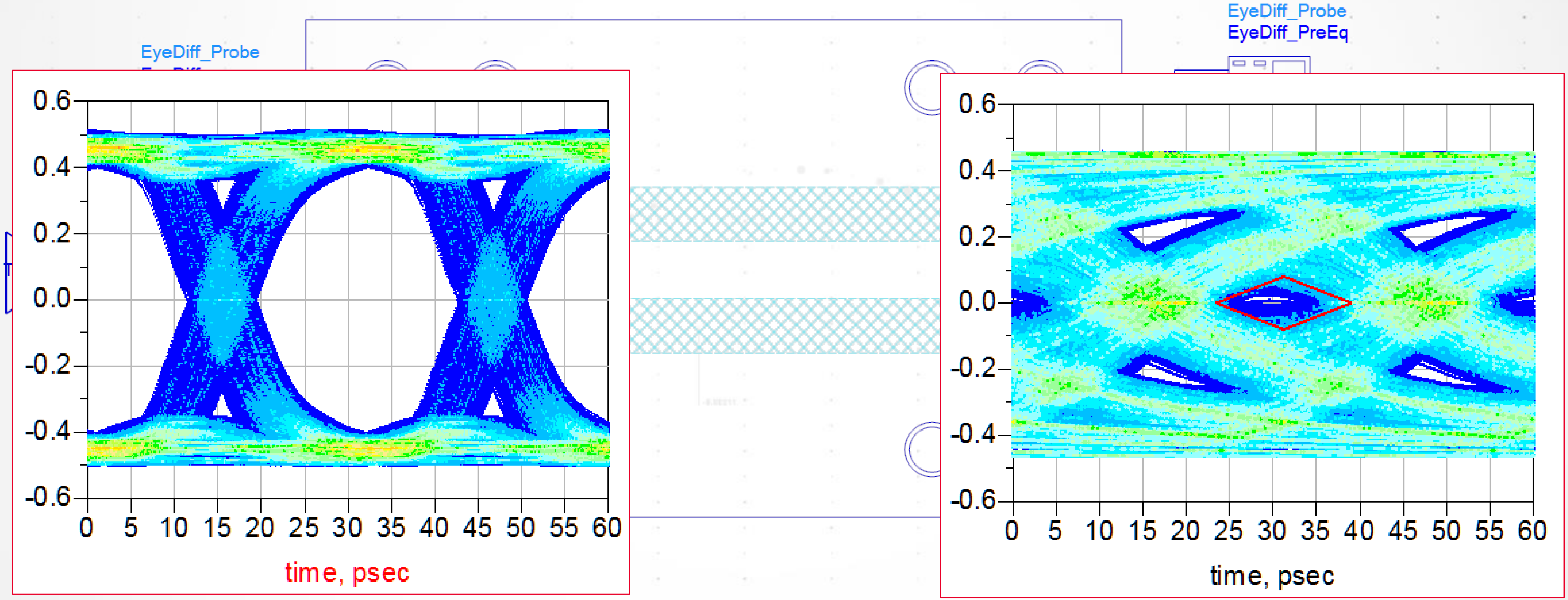
PCIe Example: Simulate a Differential Channel



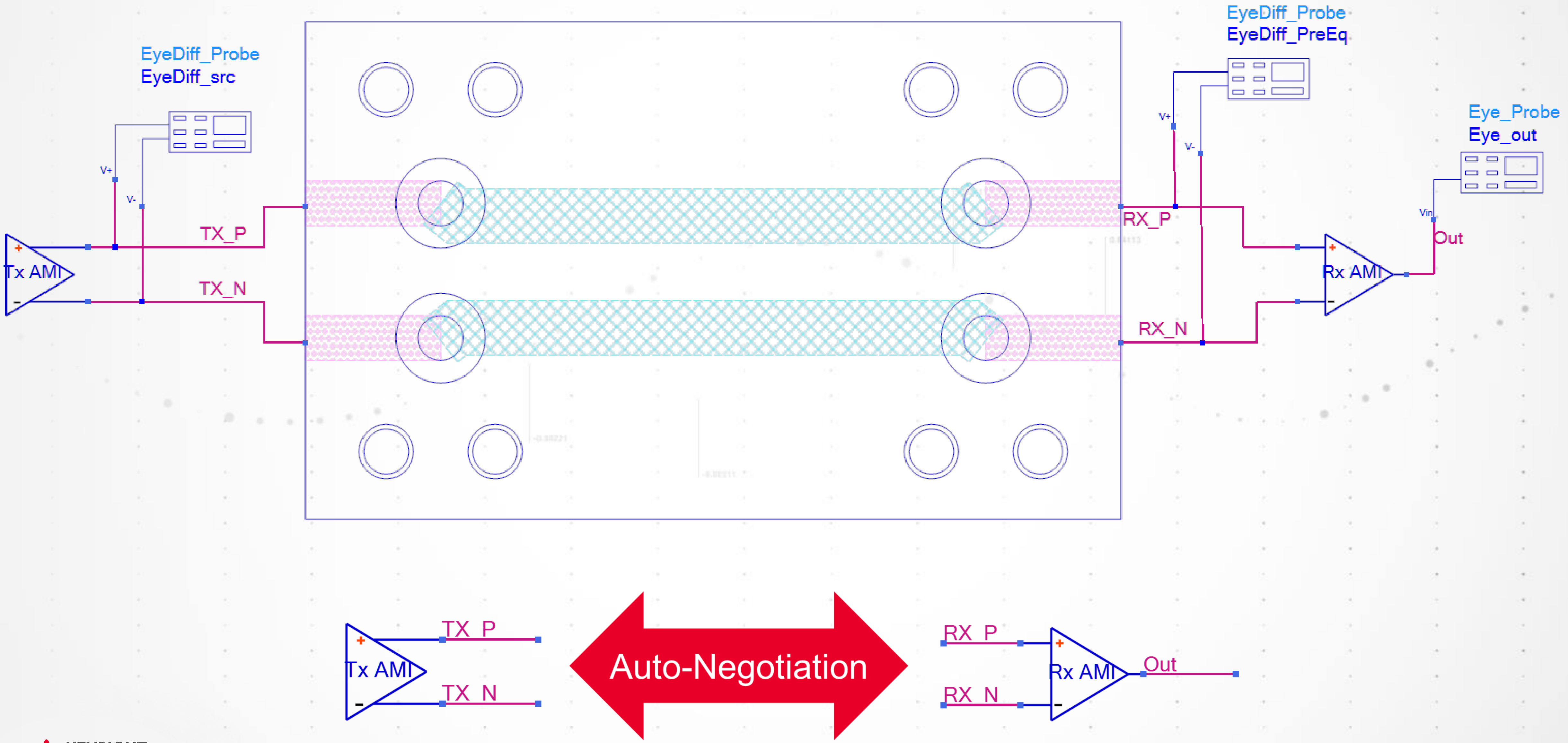
IBIS-AMI Simulation Setup and Result without BCI



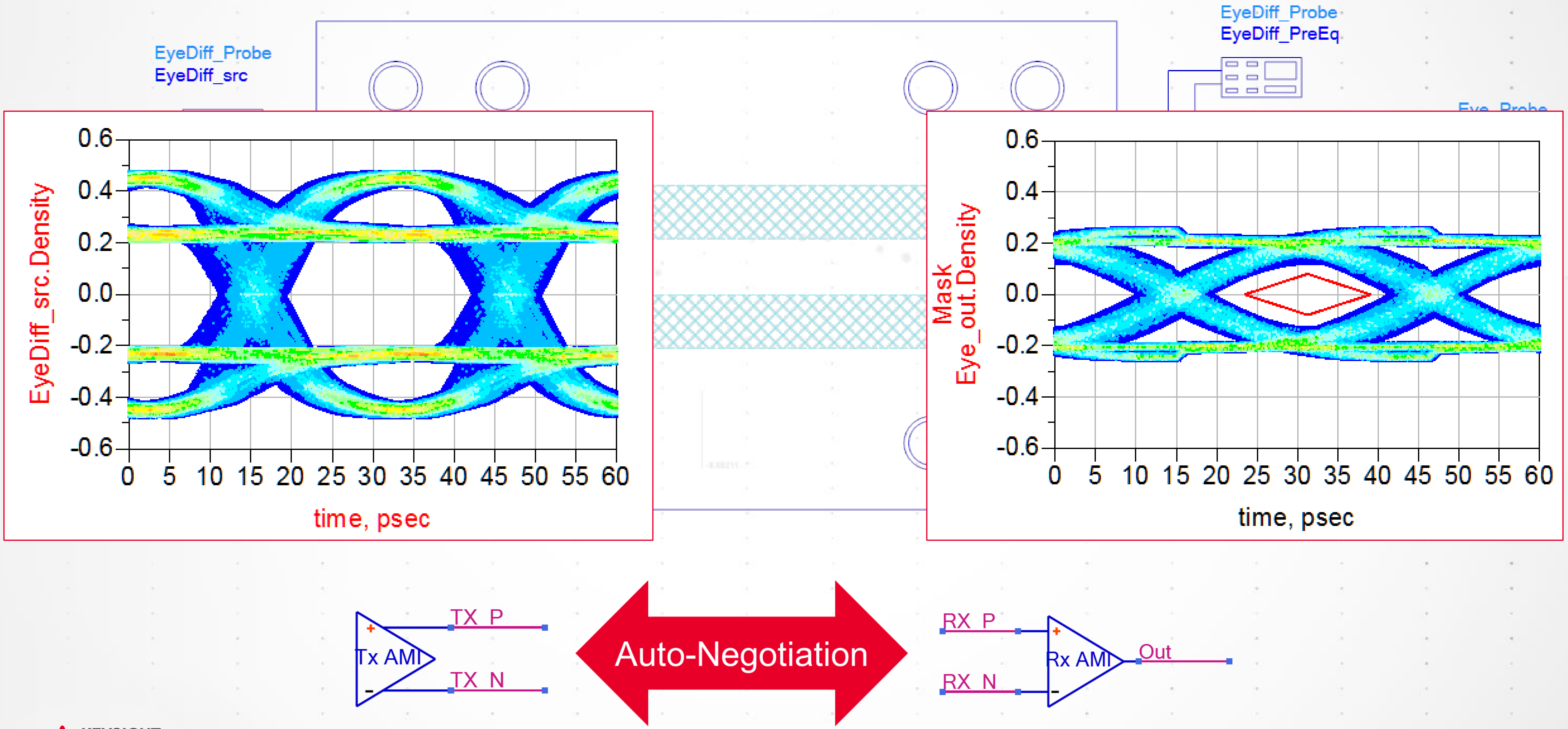
IBIS-AMI Simulation Setup and Result without BCI



IBIS-AMI Simulation Setup and Result with BCI



IBIS-AMI Simulation Setup and Result with BCI



Critical Steps to Taking a Measurement in the Real World

Establish a Robust Signal Integrity Measurement and Simulation Workflow
https://connectlp.keysight.com/DesignConKEF2018

Prepare instrument for measurement

- Calibration
- Fixture removal (de-embedding)

→ **Anticipate the measured result**

Acquire channel data

- Multi-port S-parameter measurement

Analyze channel performance

- Single-ended vs. differential
- Eye diagrams (NRZ, PAM4)
- COM

Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective		
Target		
Reference Structures		
Techniques		

Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective	Move reference plane	
Target		
Reference Structures		
Techniques		

KEYSIGHT TECHNOLOGIES

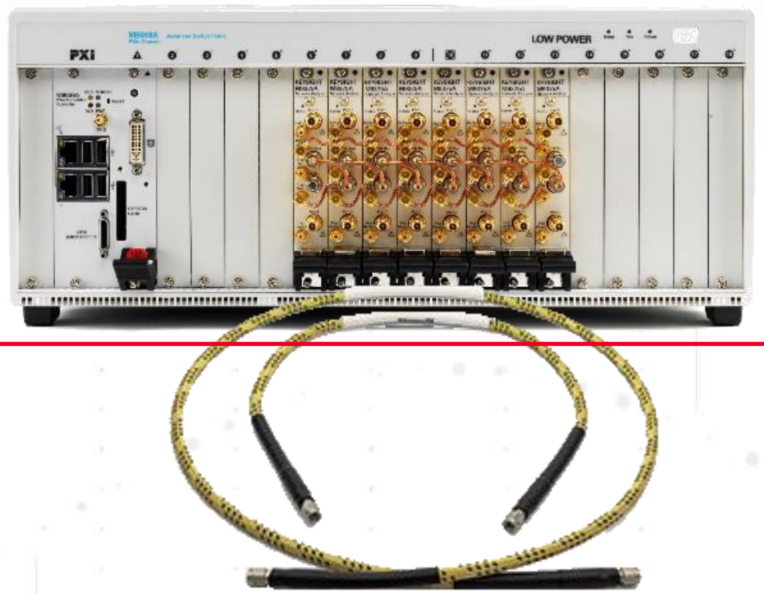
Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective	**Move reference plane**	
Target	Instrument	Measurement
Reference Structures		
Techniques		

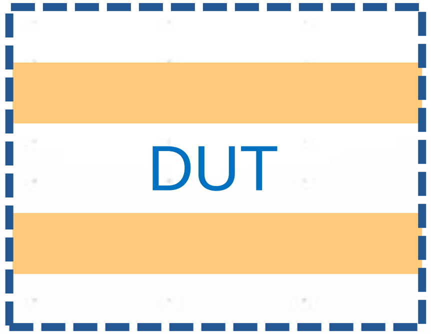
Comparison Between Calibration and De-embedding

	Calibration	De-embedding
Objective	**Move reference plane**	
Target	Instrument	Measurement
Reference Structures	• Short, Open, Load, Thru (SOLT) • Thru, Reflect, Line (TRL) • Thru, Reflect, Match (TRM)	• 2x Thru • 1x Open, 1x Short
Techniques	• Mechanical Calibration • Electronic Calibration	• Automatic Fixture Removal • Measurement-based Model

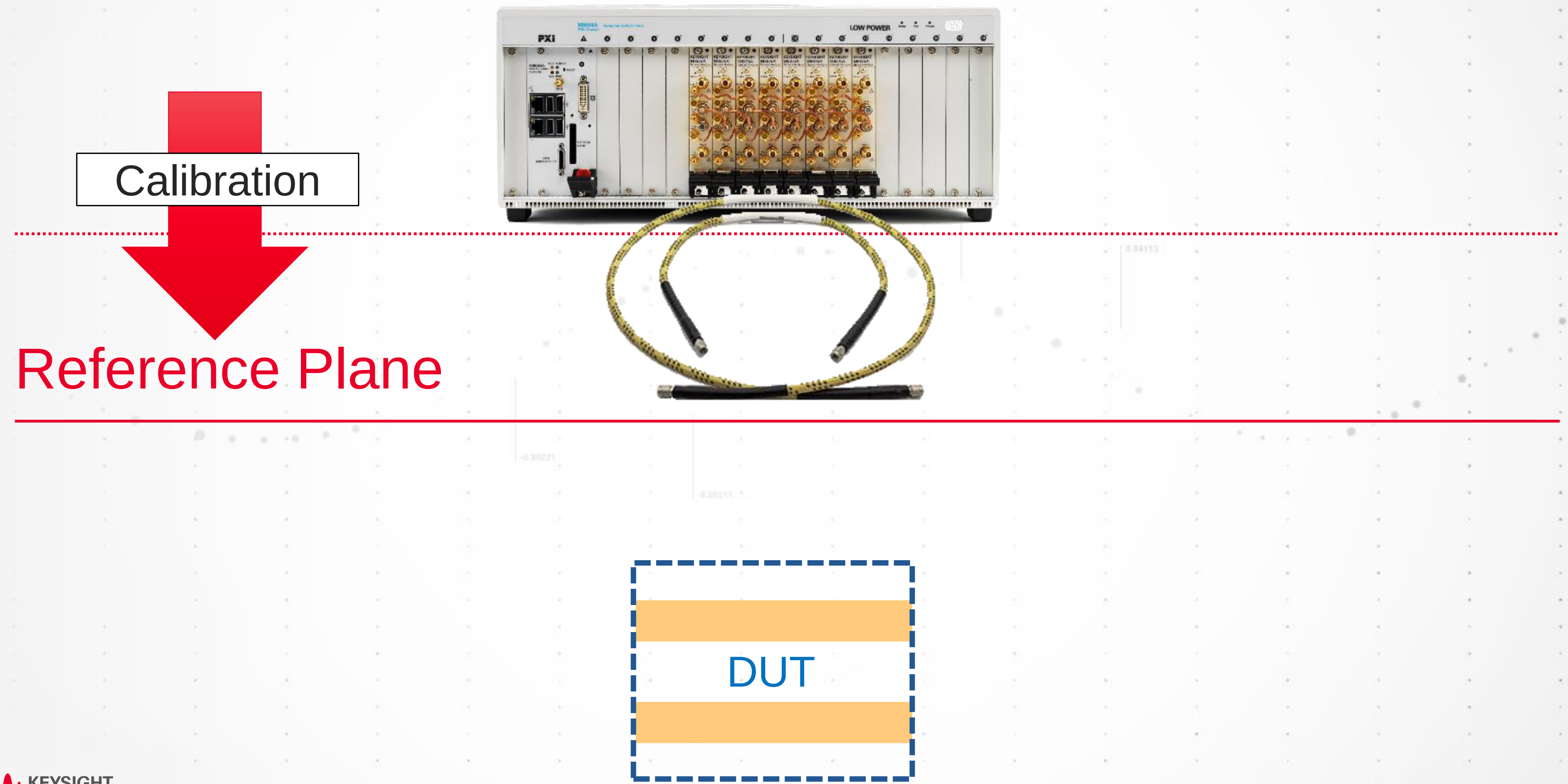
Measurement Setup and Default Reference Plane



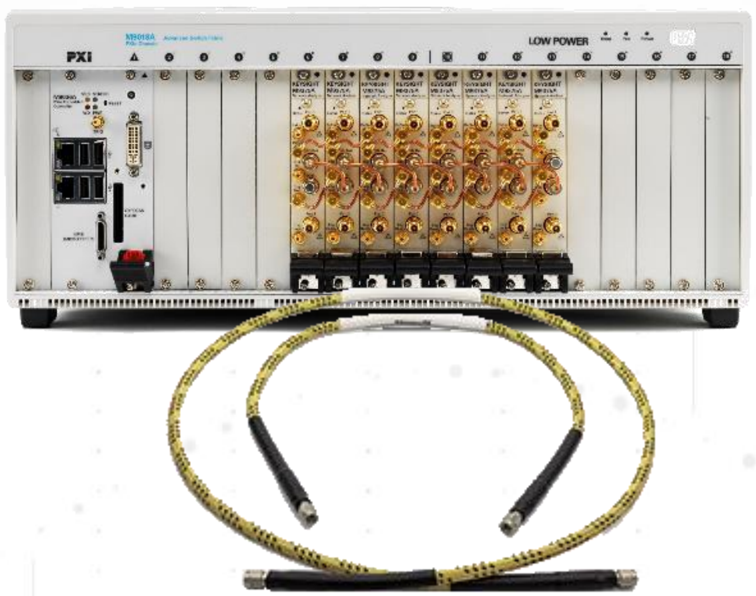
Reference Plane



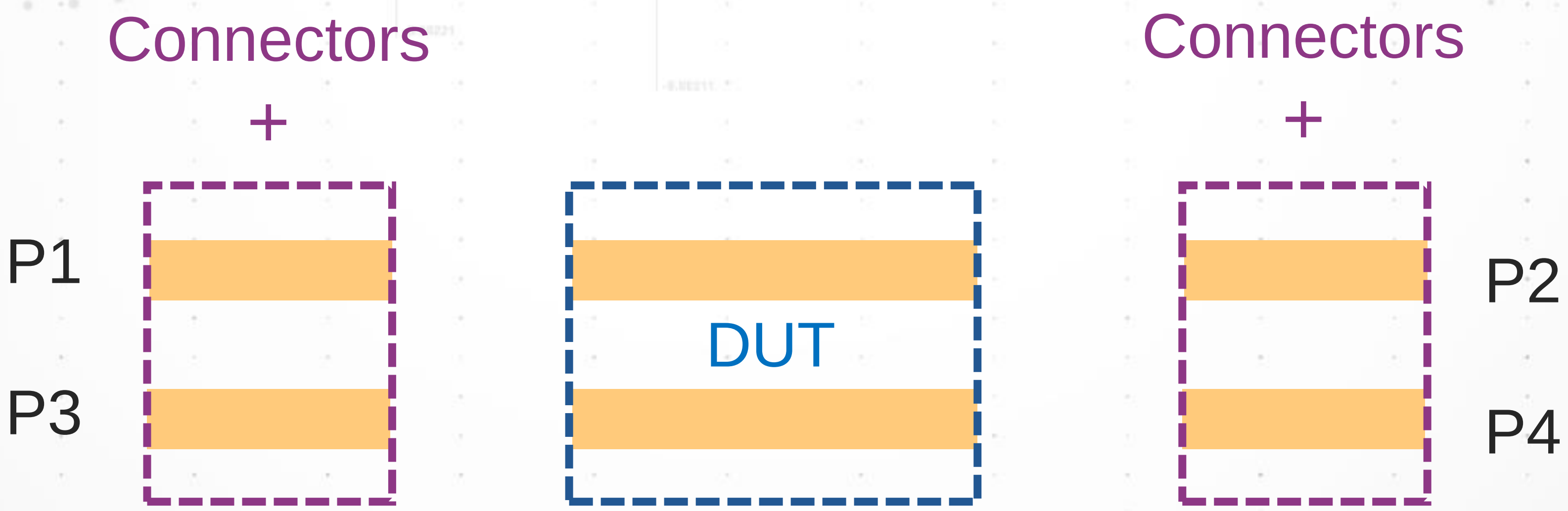
Calibration Moves the Instrument Reference Plane



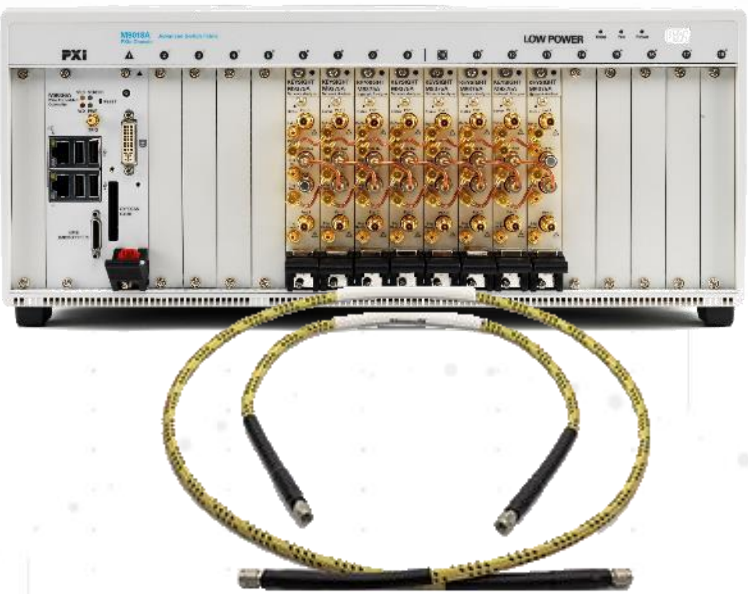
Measure Device Under Test Through Fixtures



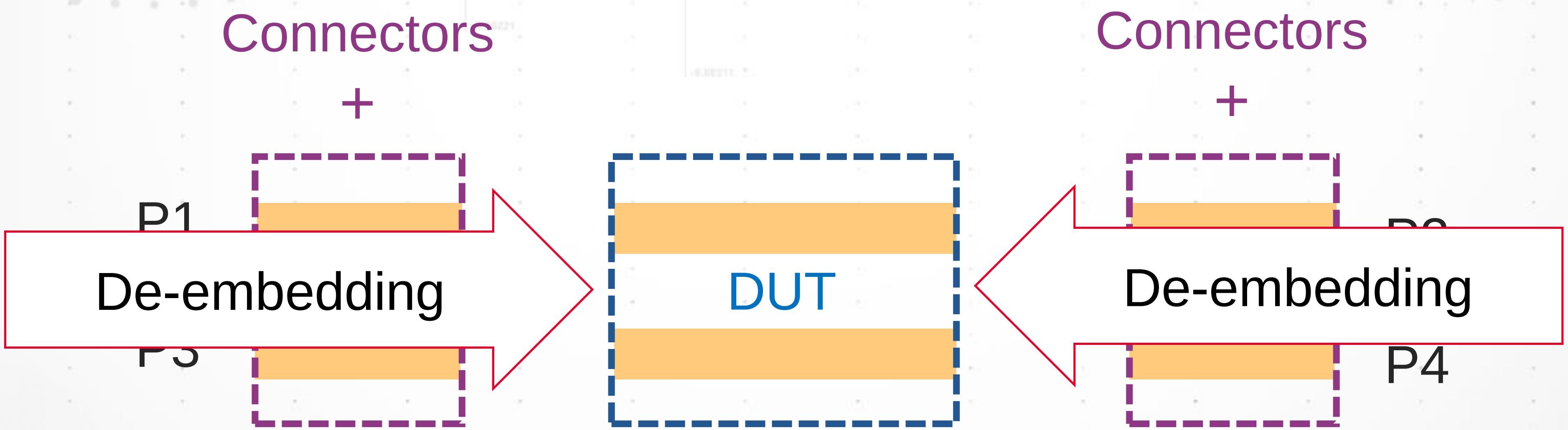
Reference Plane



De-embedding Moves the Measurement Reference Plane



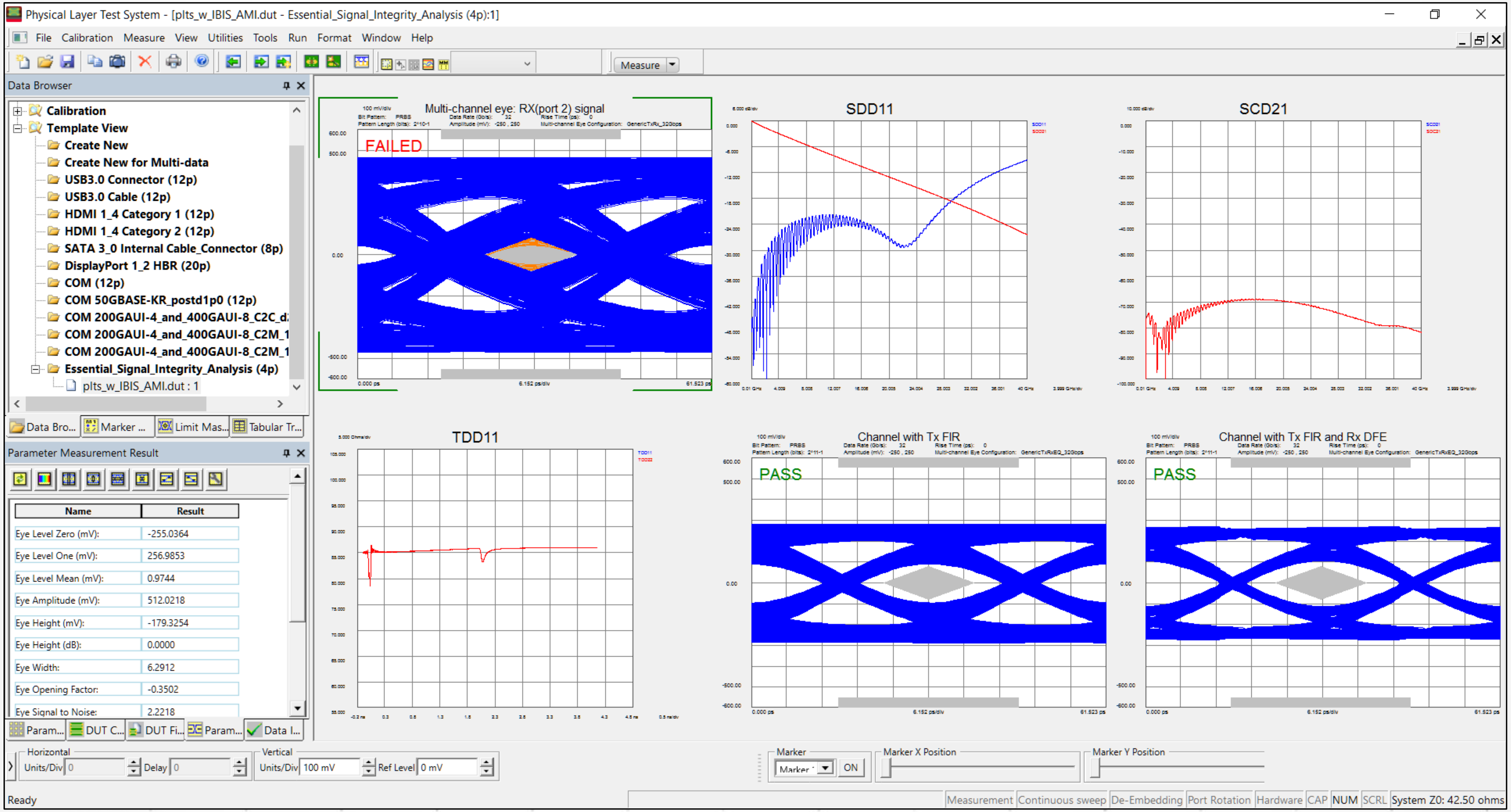
Reference Plane



KEYSIGHT TECHNOLOGIES

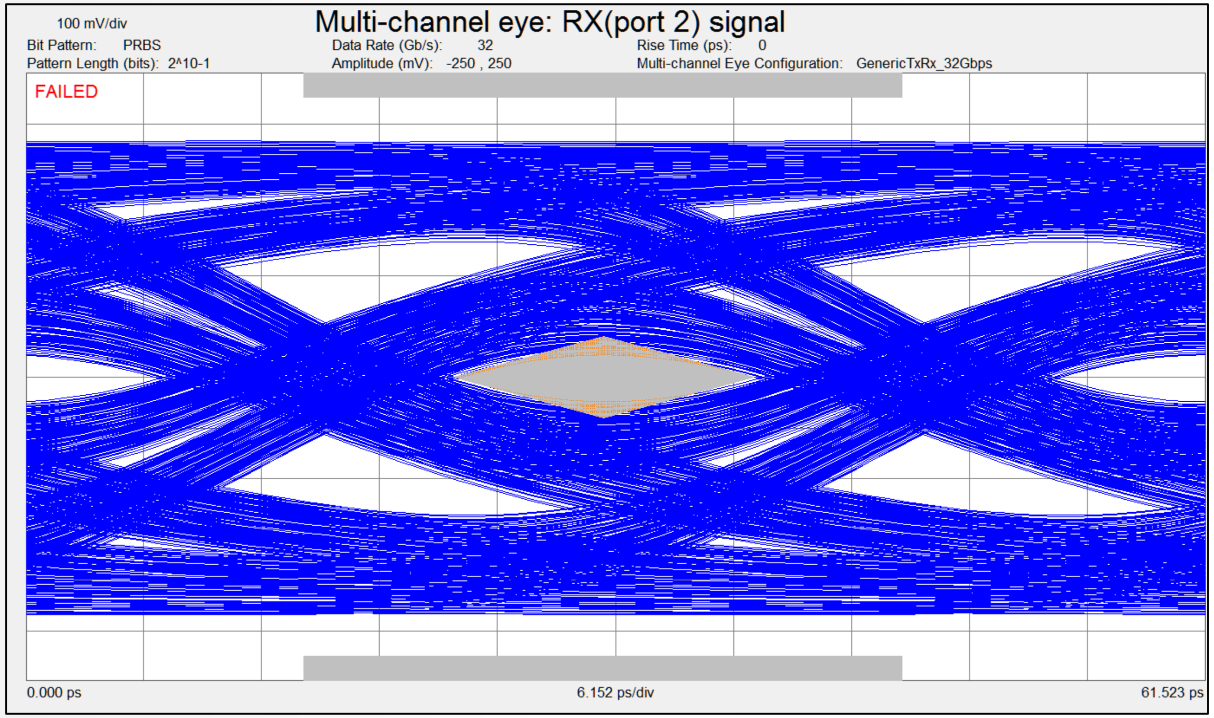
PLTS Rapid Testing Demo

Rapid Channel Testing with IBIS-AMI

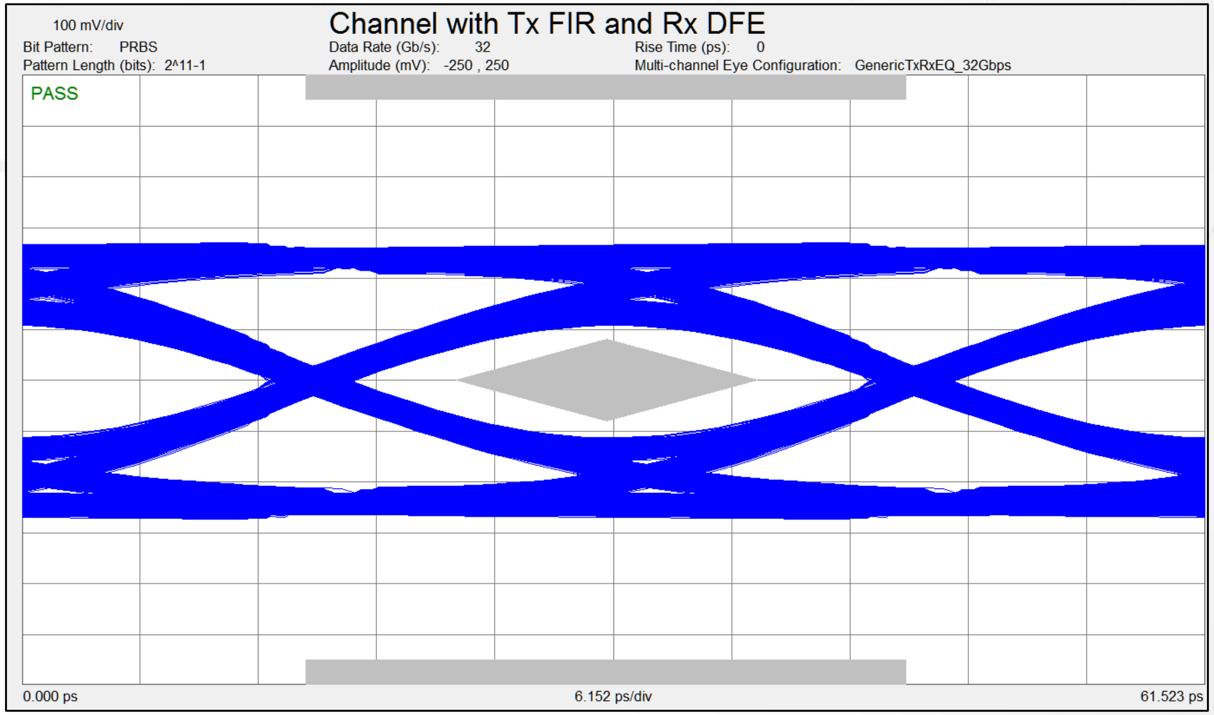


Channel Before and After Equalization

FAIL

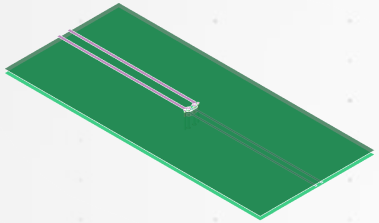


PASS



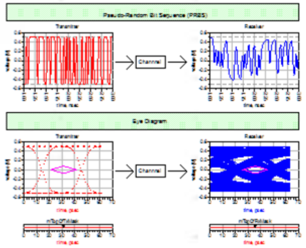
KEYSIGHT TECHNOLOGIES

Summary

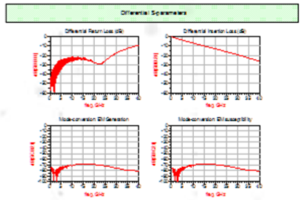


The case of the failing virtual channel

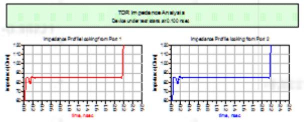
Eye diagrams



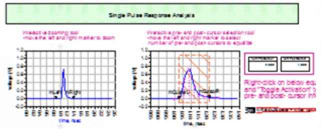
Mixed-mode S-parameters

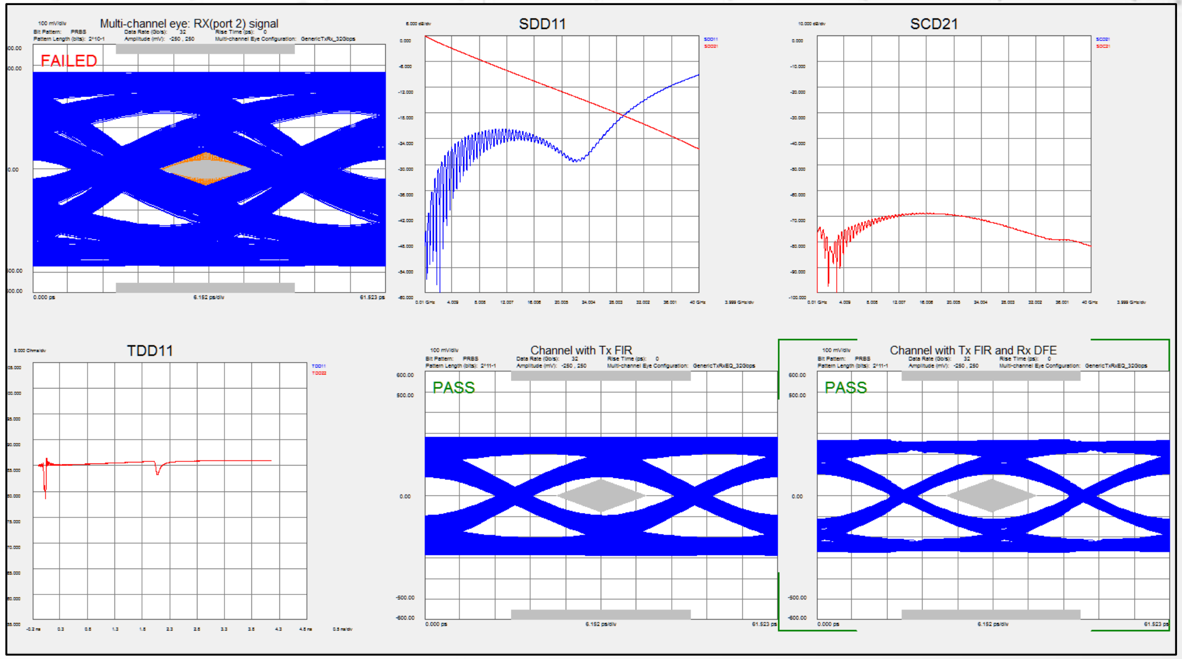


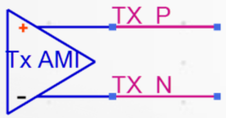
Time domain reflectometry



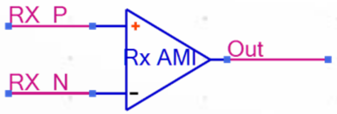
Single pulse response



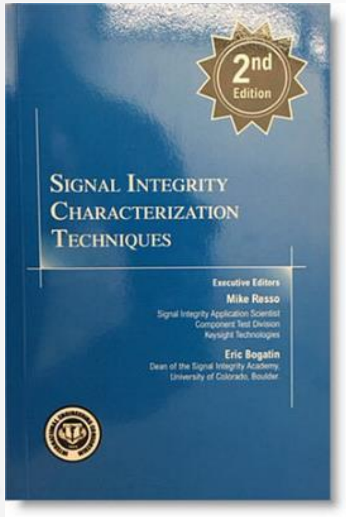




Auto-Negotiation

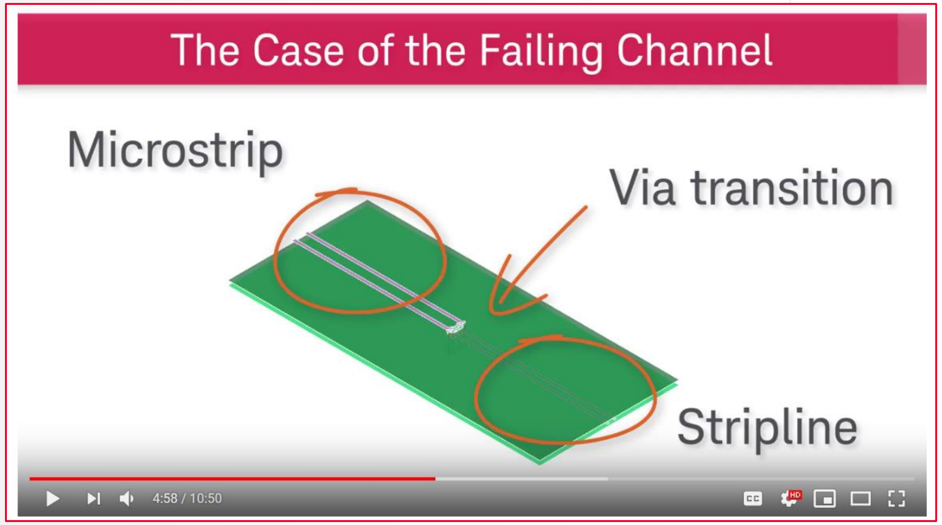


Resources



Physical Layer Test System (PLTS) 2019:
www.keysight.com/find/plts
Digital Interconnect Test System:
www.keysight.com/find/diref
Free Signal Integrity Book:
www.keysight.com/find/RessoBook

Establish a Robust Signal Integrity Measurement and Simulation Workflow
https://connectlp.keysight.com/DesignConKEF2018



Advanced Design System (ADS) 2019:
http://www.keysight.com/find/ads
YouTube Video:
https://youtu.be/mpyMWuVrKKc
Workspace Download: