# Keysight/ADS Workshop

# Power Integrity Target Impedance Says it All, Power Delivery is AC not

Heidi Barnes, (Keysight Technologies)

# SPEAKER Heidi Barnes

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Heidi Barnes is currently the Power Integrity Product Owner for High-Speed Digital applications in the Design Engineering Software Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and channel simulators to solve signal and power integrity challenges. Author of over 20 papers on SI and PI, active member in developing the new IEEE P370 Standard involving interconnect S-parameter quality after fixture removal, and recipient of the DesignCon 2017 Engineer of the Year. Heidi graduated from the California Institute of Technology in 1986 with a bachelor's degree in electrical engineering.

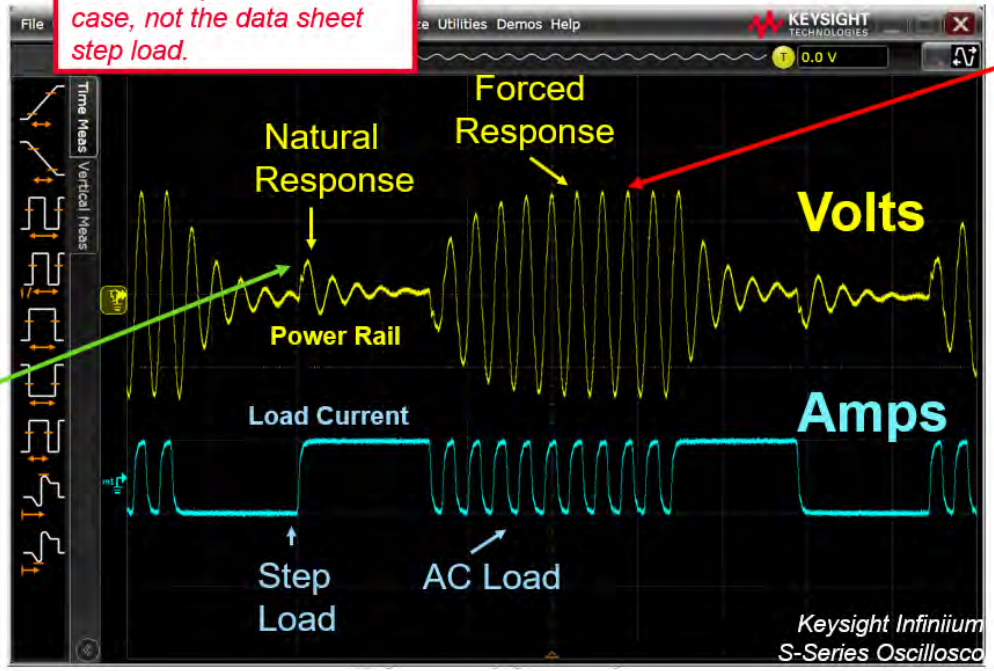
# Power Delivery for Digital Loads is AC not DC!

$$V = L\frac{dI}{dt}$$

**KEY TAKE AWAY**
*Forced response is worst case, not the data sheet step load.*

*New Method:*
*Finding the worst case Load*

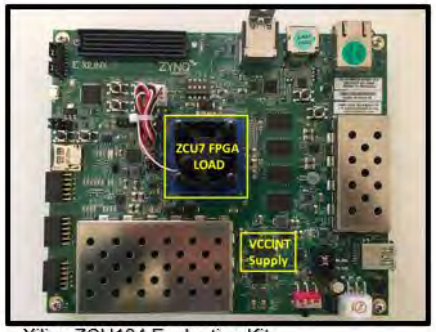
**FAIL**
**Over Voltage**
**Tx/Rx Bit Error**
**EMI**
**Crosstalk**



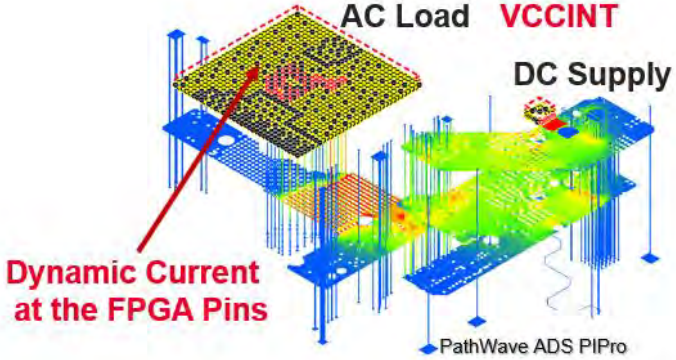

*Old Method:*
*Step Load Transient Test*
*(False Positive)*

**PASS**
**Datasheet Design**

# Power Rail Noise Ripple is Not Intuitive



Xilinx ZCU104 Evaluation Kit




**DesignCon 2020**

A Method for Dynamic Load Current Testing with a Benchtop Power Supply

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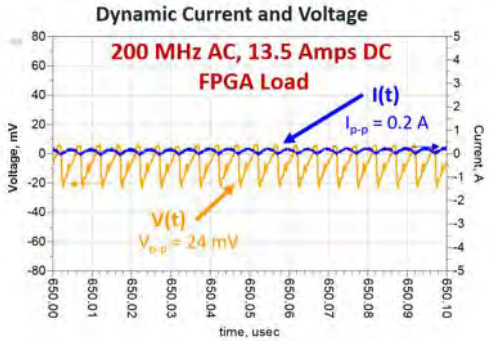
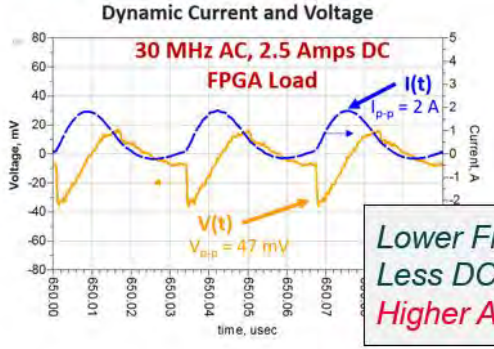



*Lower Frequency*
*Less DC Current*
*Higher AC Noise!*

# Agenda

- **Why Flat Impedance is the Design Goal**
  - Worst case PDN noise ripple is not intuitive
- **How to Measure Power Rail Impedances in the Micro-Ohms**
  - 2-Port Shunt Impedance where $Z_{DUT}$ is a function of S21
- **What is Wrong with Capacitor Vendor Data**
  - Vendor data for capacitor ESL typically includes mounting inductance which needs to be removed for connecting to EM simulations.

# Power Integrity Starts with Target Impedance

## Target Impedance Calculation

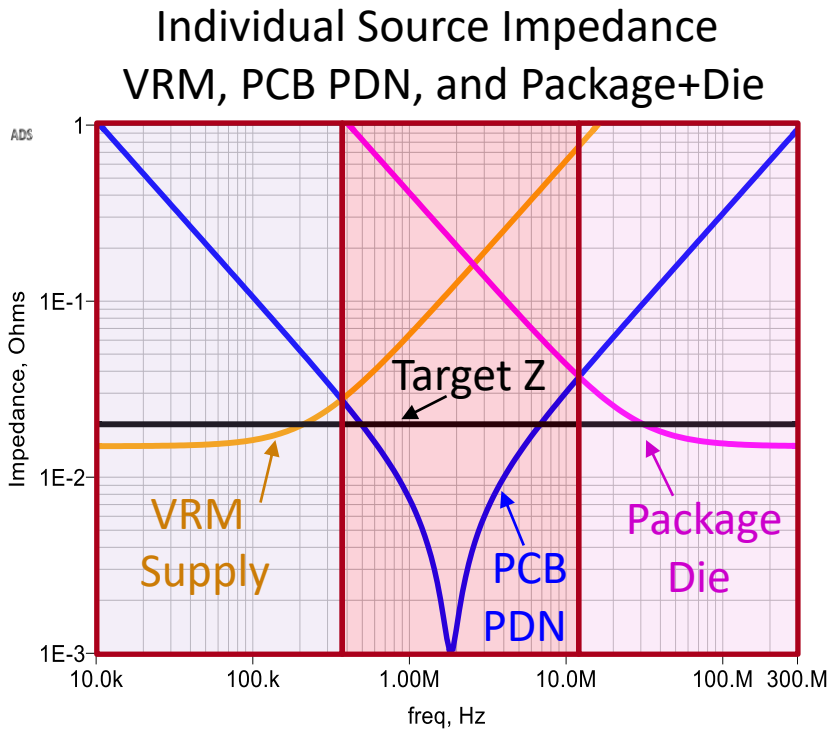
$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$

# Using Impedance to Find Worst Case Power Rail Ripple

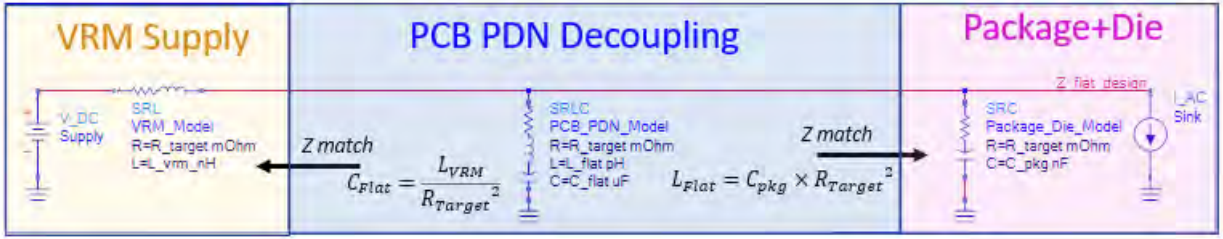
VRM = Low Pass Series R-L

Capacitors = Band Pass Series C-R-L

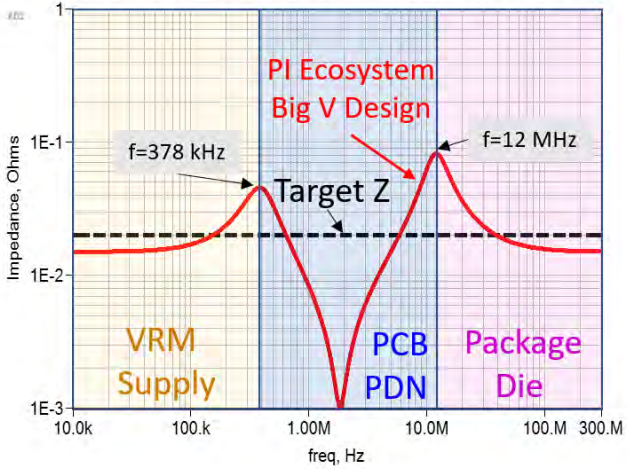
Package/Die = High Pass R-C



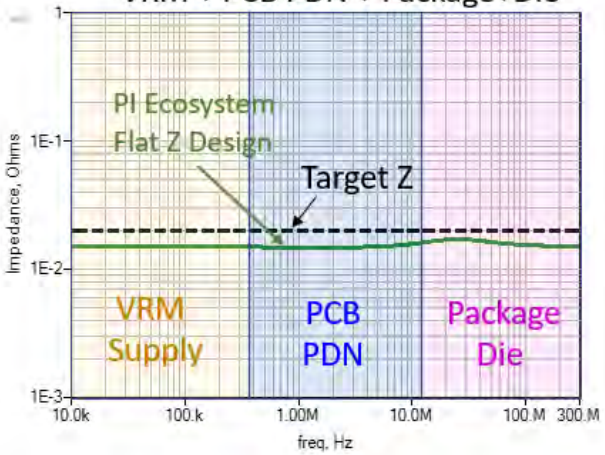
# PI Ecosystem Simulation: VRM + PCB PDN + Load



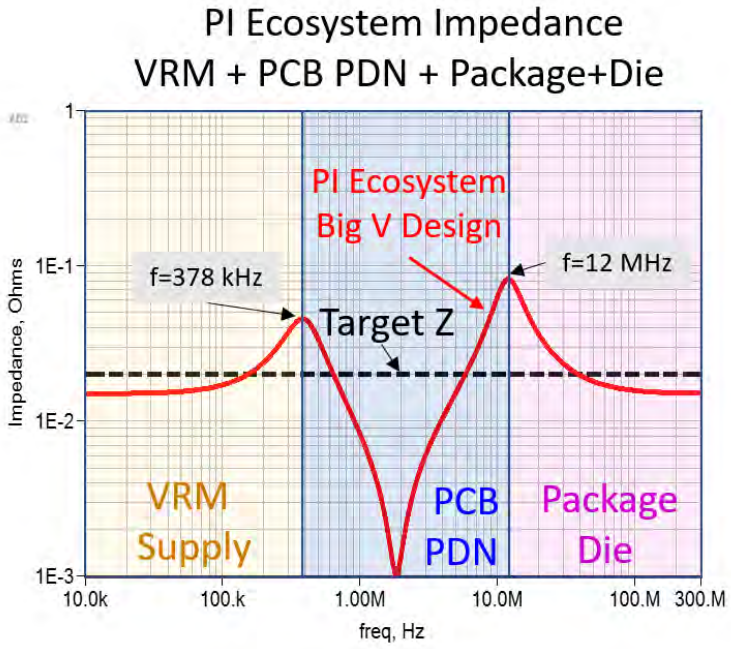

PI Ecosystem Impedance
VRM + PCB PDN + Package+Die

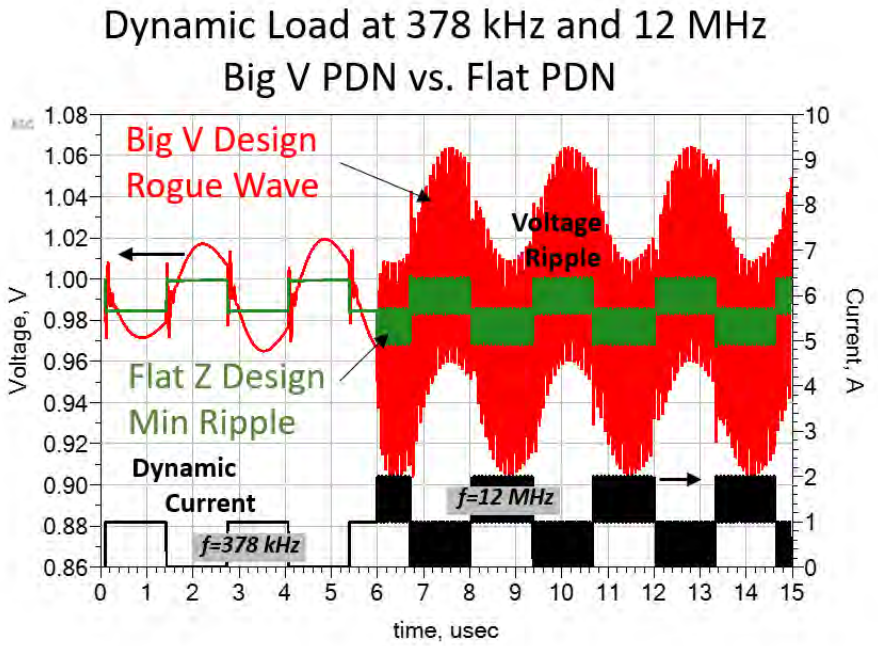



Flat Impedance Design
VRM + PCB PDN + Package+Die



# Worst Case Power Rail Noise Ripple

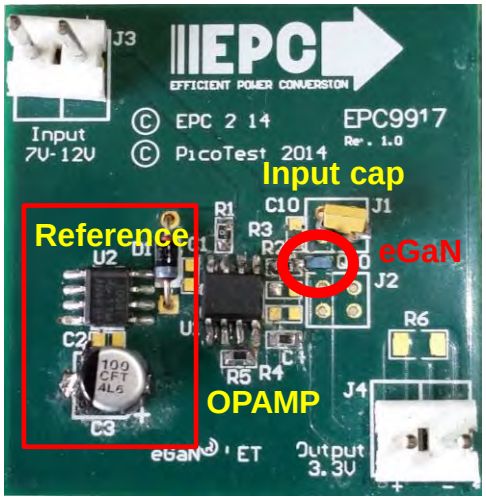


# Why GaN is So Exciting for Power Delivery

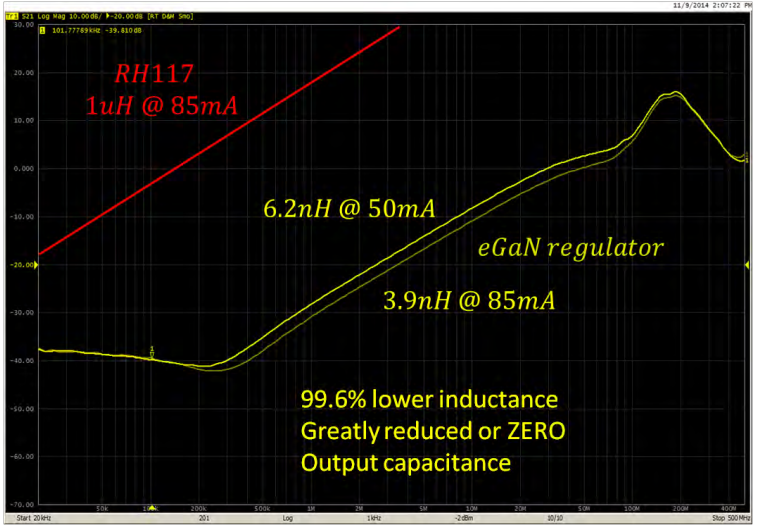
….not just the size

$$C_{Flat} = \frac{L_{VRM}}{R_{Target}{}^2}$$




Maintaining a 0.1Ω maximum PDN impedance up to 2MHz requires 80uF for a RH117 and NO output cap for the eGaN regulator.

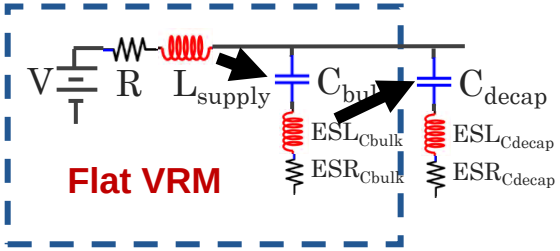
3.9nH is nearly equivalent to the ESL of a tantalum capacitor

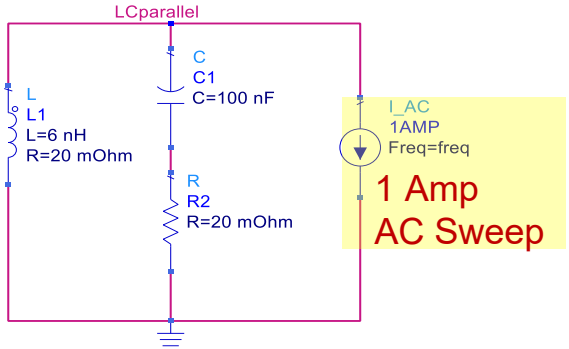


# Root Cause of Ringing on the Power Rail

*Parallel inductance can resonate with the decoupling capacitance*

**Parallel L-C in the PDN**




$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

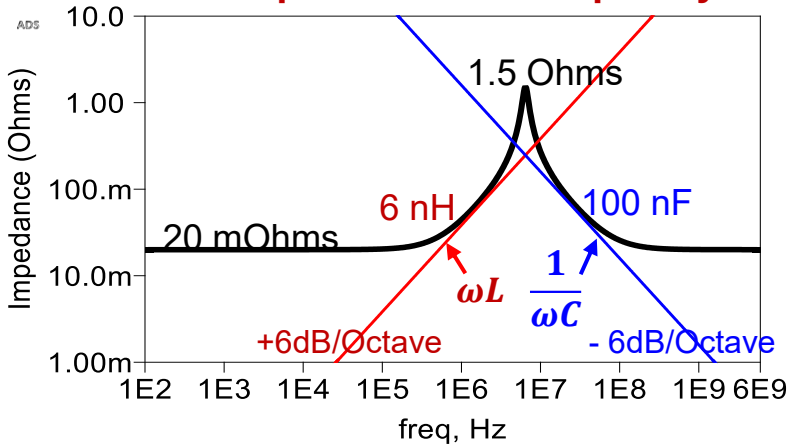
$$\Delta V = \Delta I \cdot Z_{peak}$$

$$\boldsymbol{Z_{peak} = Z_0 \cdot Q}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$Q = \frac{Z_0}{R_{total}}$$

**Impedance vs. Frequency**




Zpeak=1.5 Ohms

Zo=250 mOhms

# Natural Step Response vs. Forced Response

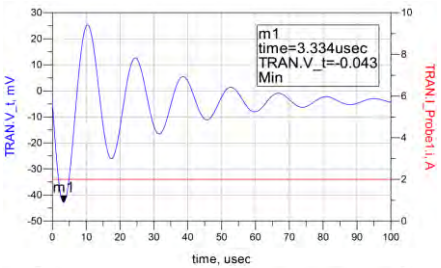
A 2 Amp change yields 3 different responses

**KEY TAKE AWAY**

*Watch the YouTube video "How to Design for Power Integrity: Finding Power Delivery Noise Problems"*

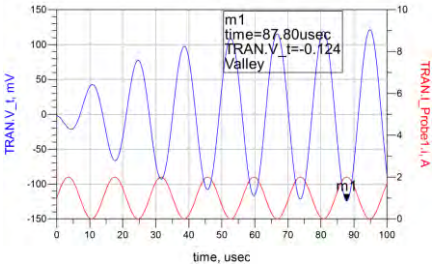

**Step natural**

$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot e^{\frac{-\pi}{4Q}} = 39mVpk$$



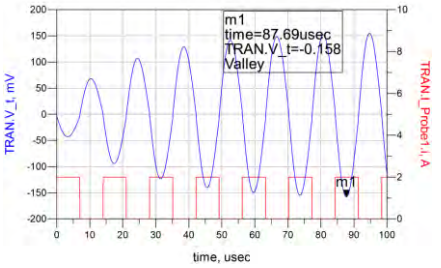

**Sine forced**

$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot \frac{Q}{2} = 123mVpk$$



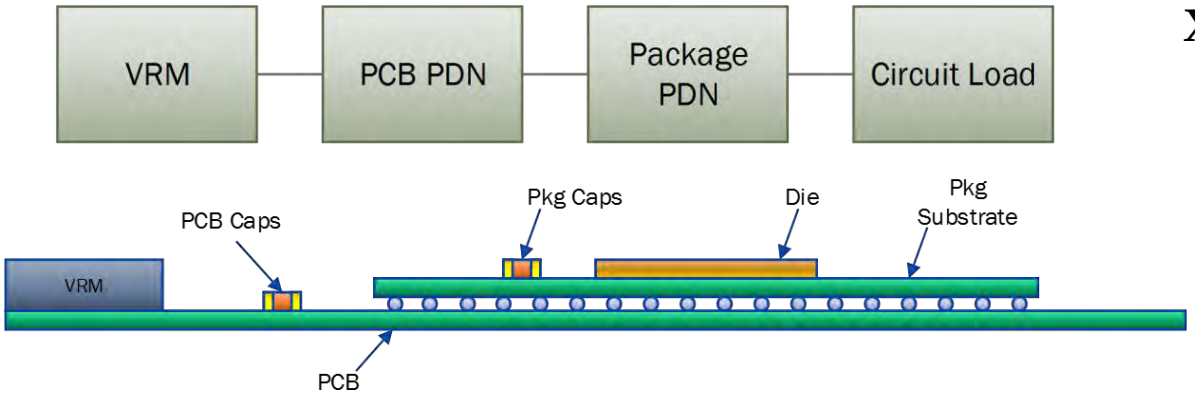

**Square forced**

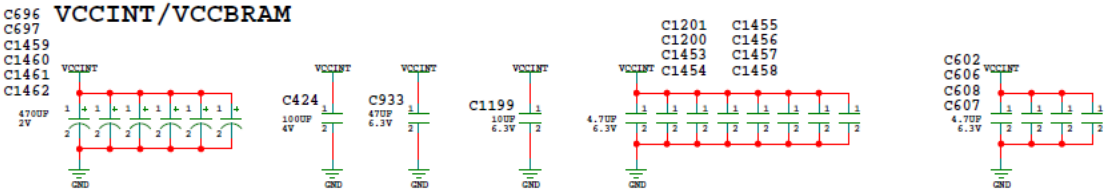
$$\Delta V = \Delta I \cdot \sqrt{\frac{L}{C}} \cdot \frac{2Q}{\pi} = 157mVpk$$



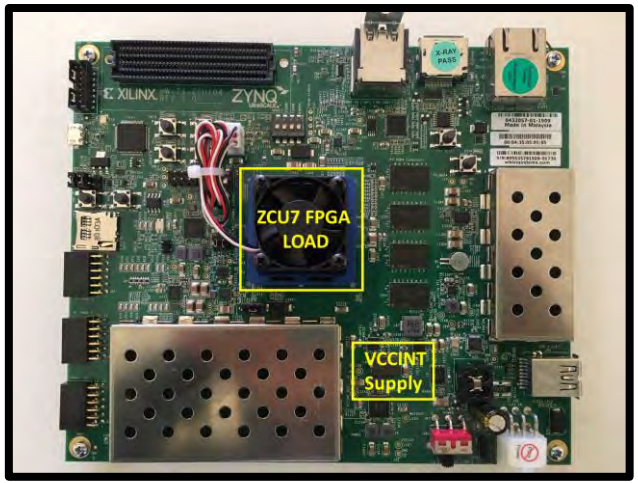

*sine and square ΔV ~Q times the step response*

# Why Lower ESR is Not Good, It Must be Matched

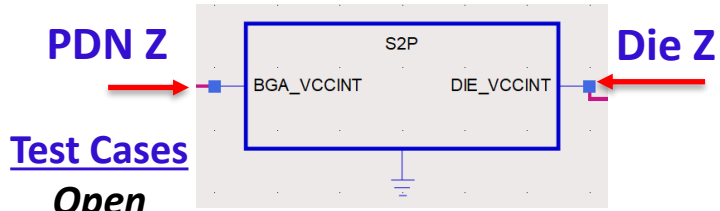



**Xilinx Zynq UltraScale+ XCZU7EV-2FFVC1156 MPSoC**



# FPGA Package/Die Model Connected to the PCB PDN

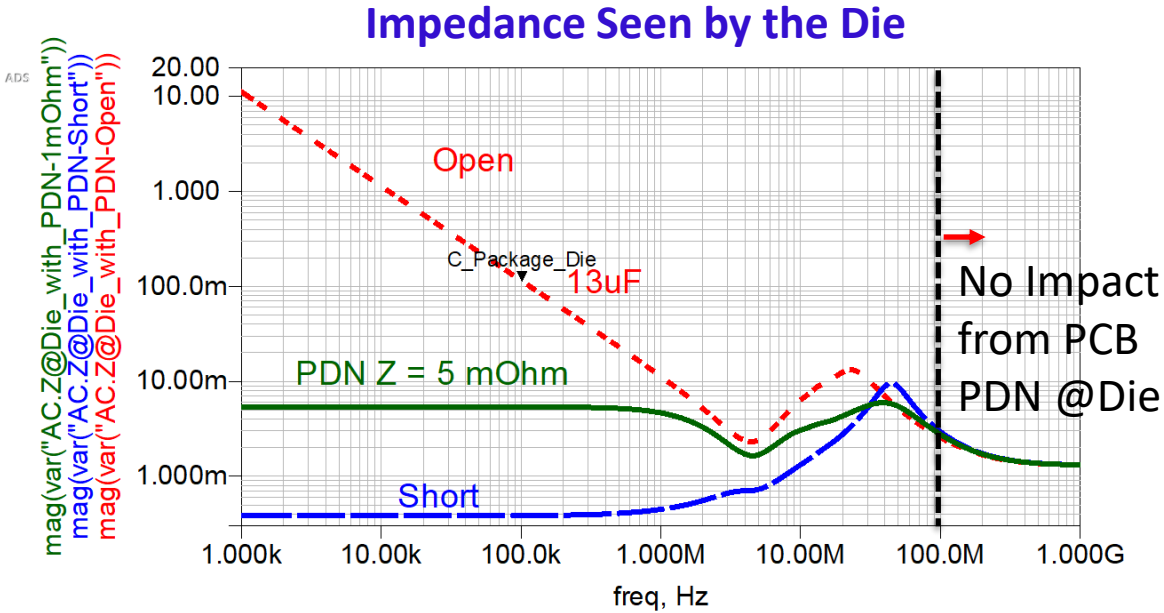



**Test Cases**

***Open***

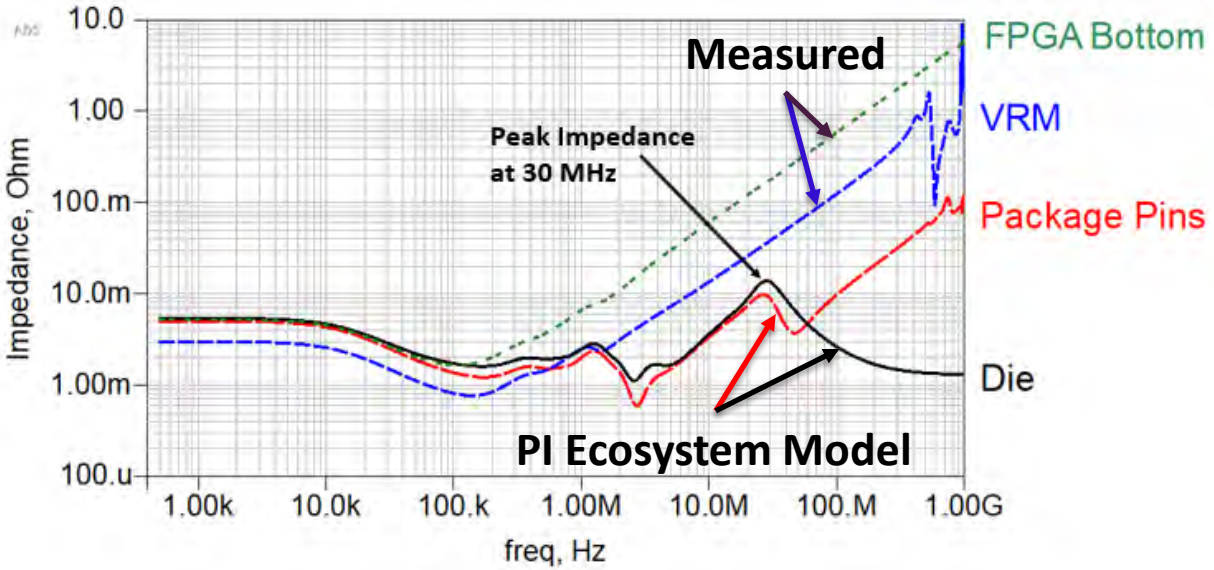
***5 milliohm***

***Short***



# FPGA Package/Die, PCB PDN EM, and Capacitor Models are Critical

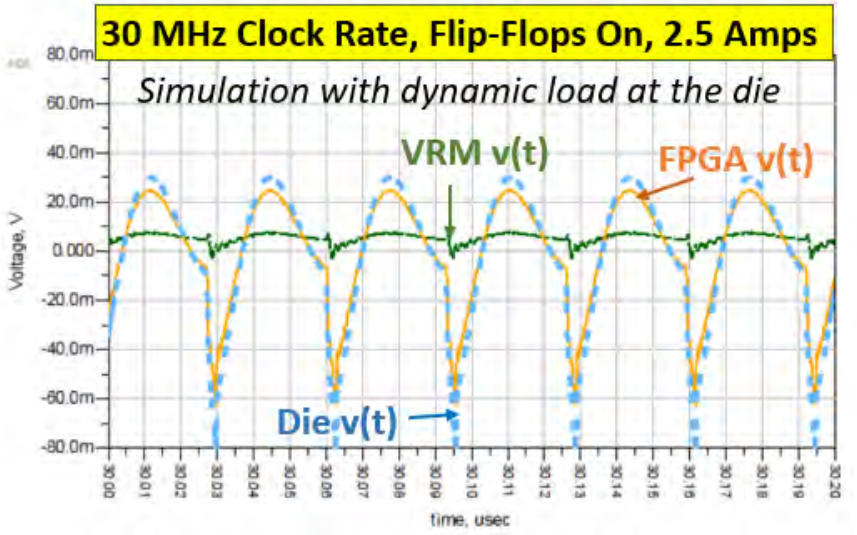
***Impedance measurements did not see the resonance at 30 MHz!***



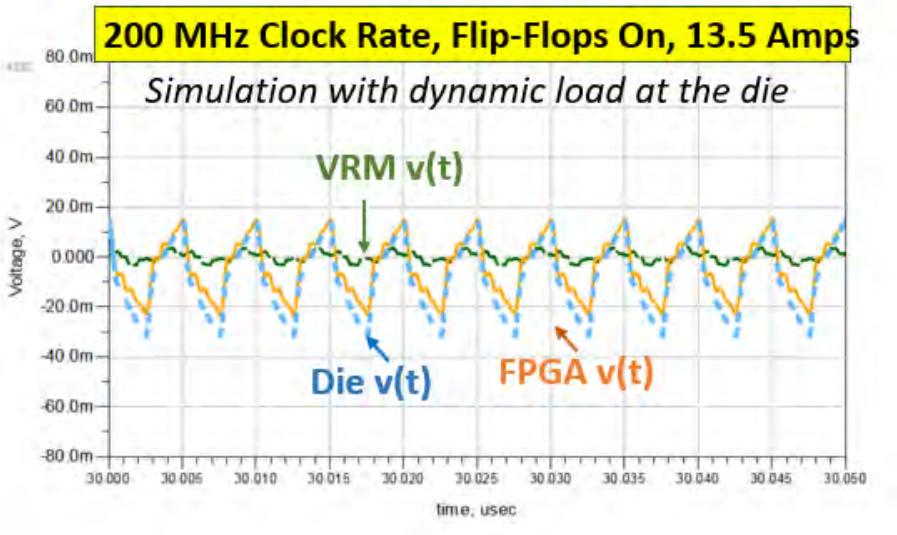

- Decoupling capacitors dominate the impedance of the VCCINT PDN.
- Measurements with VCCINT are only accessible on the bottom side of the FPGA and include the via inductance.
- PIPro PDN EM model with package/die (CPM) in ADS schematic accurately predicts impedance peak that measurement could not see.

# Simulation Shows 30 MHz Toggling has More Noise

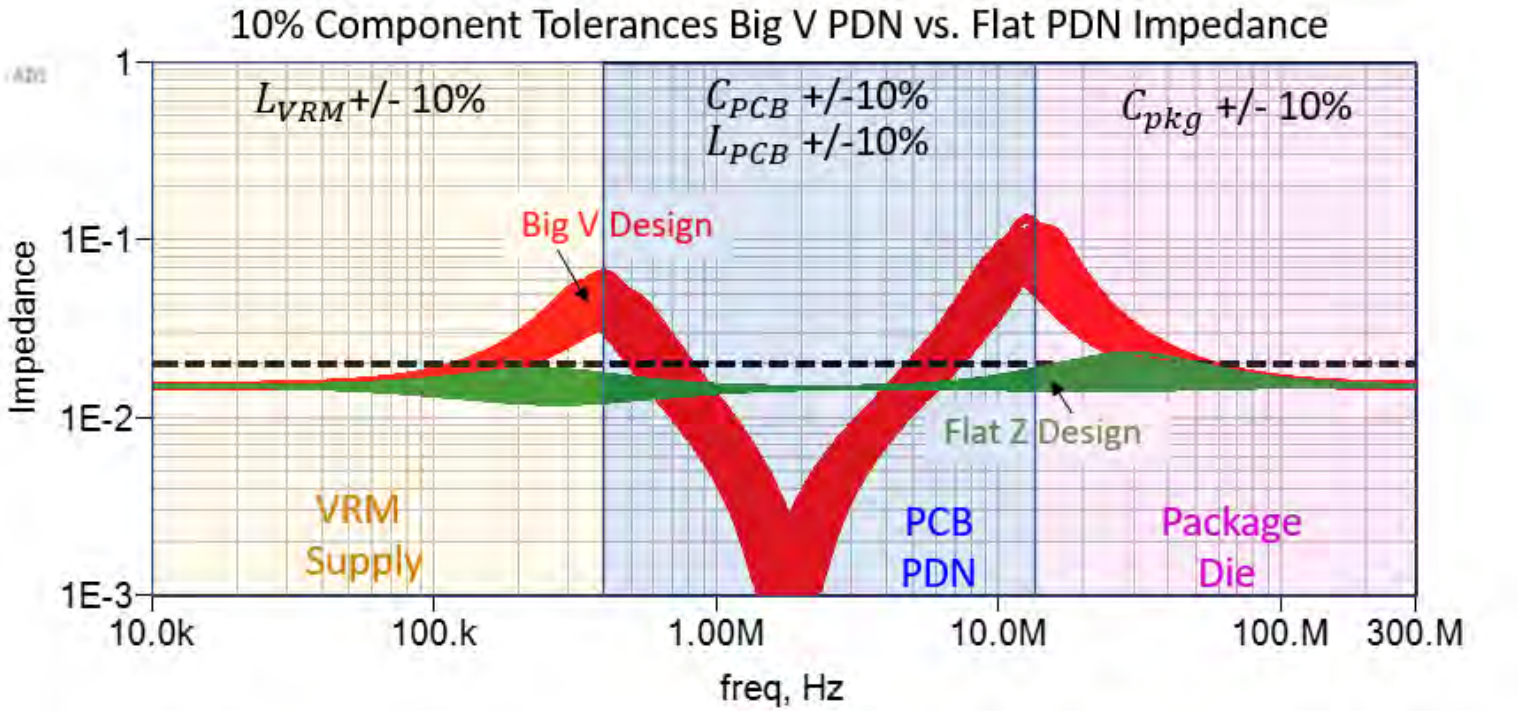
*Lower frequency and lower current has higher noise*




*Higher frequency and higher current has less noise*



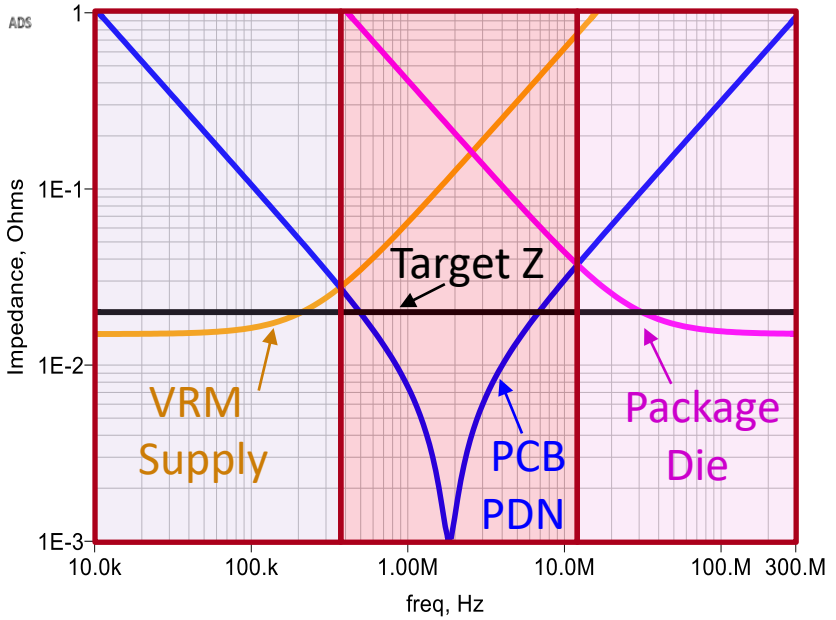
# Flat Impedance Design Provides Bigger Margins



# Remember

- Parallel L and C resonate in the time domain but are easier to find as impedance peaks in the frequency domain.
- Flat impedance minimizes the noise ripple by reducing the dynamic currents.
- Flat impedance is matched impedance with the simple rules of thumb based on $Z_0 = \sqrt{\frac{L}{C}}$

Individual Source Impedance
VRM, PCB PDN, and Package+Die



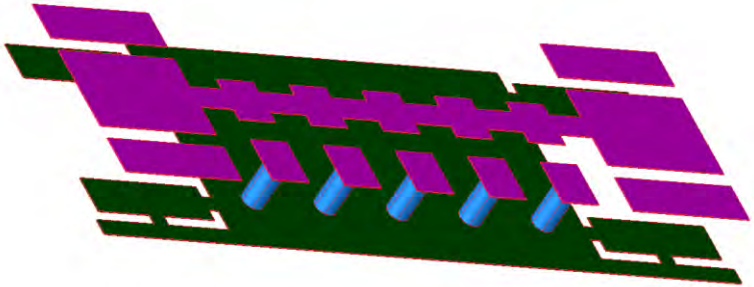

$$C_{Flat} = \frac{L_{VRM}}{R_{Target}{}^2} \qquad L_{PCB} = C_{Pkg} * R_{Target}{}^2$$

# Agenda

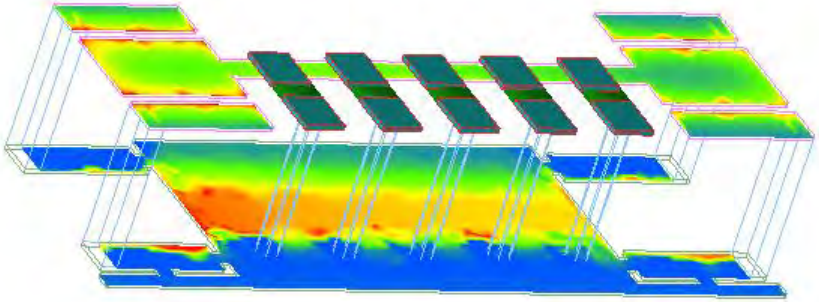
- **Why Flat Impedance is the Design Goal**
  - Worst case PDN noise ripple is not intuitive
- **How to Measure Power Rail Impedances in the Micro-Ohms**
  - 2-Port Shunt Impedance where $Z_{DUT}$ is a function of S21
- **What is Wrong with Capacitor Vendor Data**
  - Vendor data for capacitor ESL typically includes mounting inductance which needs to be removed for connecting to EM simulations.

# Parallel Capacitors Increase C and Decrease L and R

## Layout



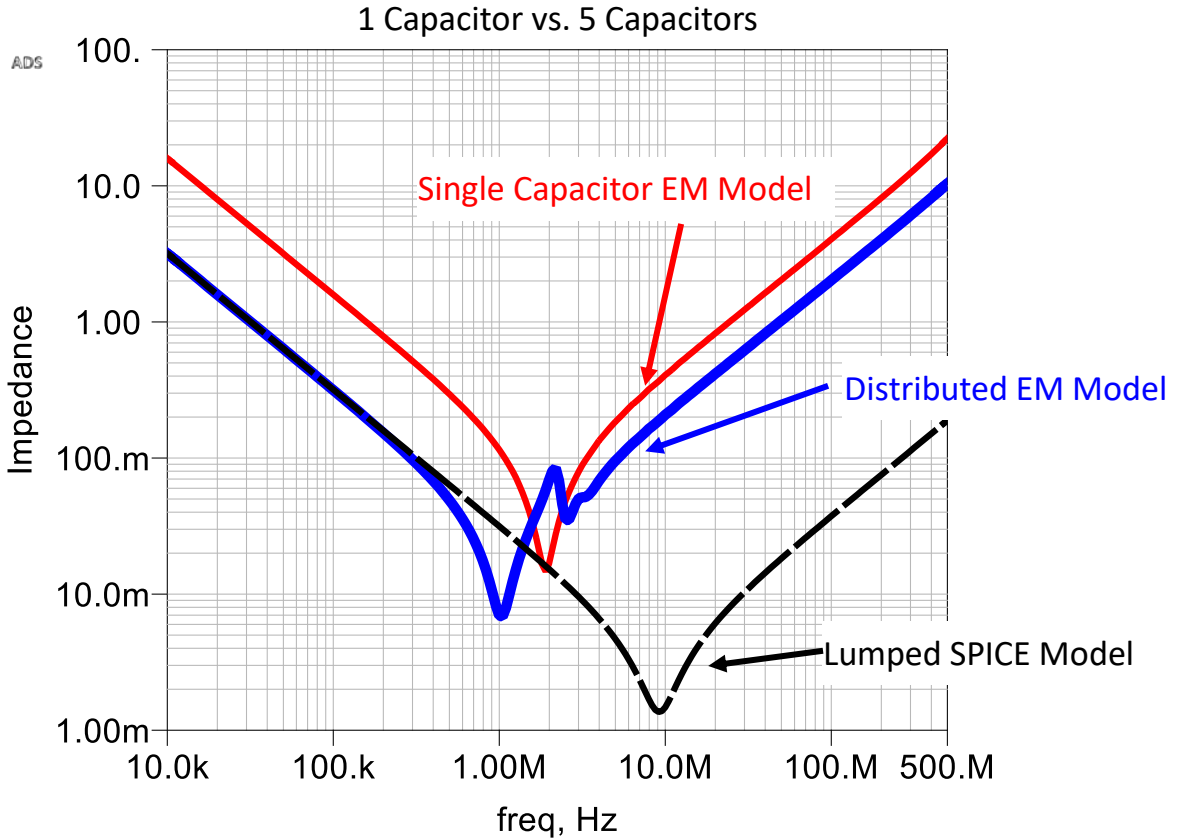
## EM Simulation with PIPro



# EM Models Capture Real World Parasitics – Parallel Caps

Paralleling same value caps

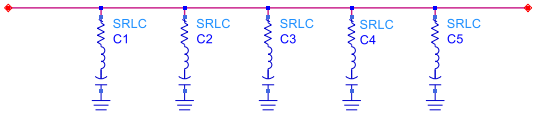
| | C | ESR | ESL |
|---|---|---|---|
| C1 | 1 uF | 7 mΩ | 300 pH |

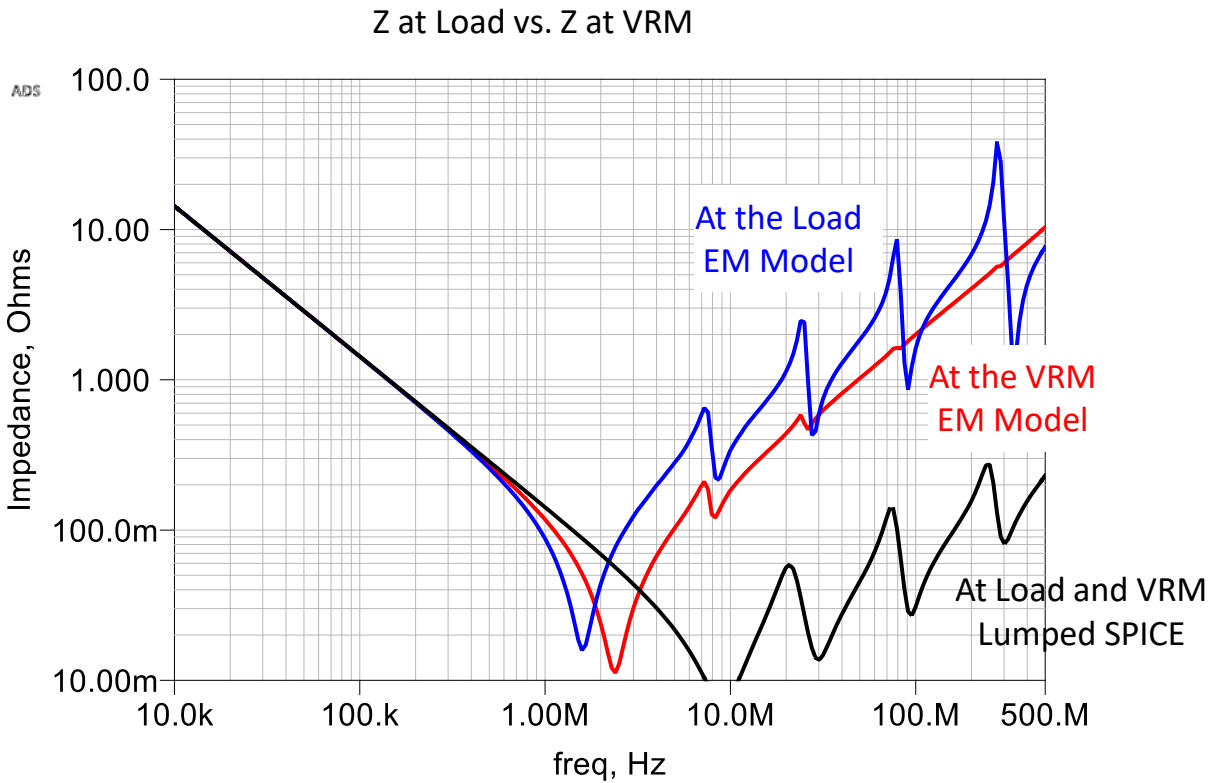


# EM Models Capture Real World PCB Parasitics $Z_{vrm} \neq Z_{load}$

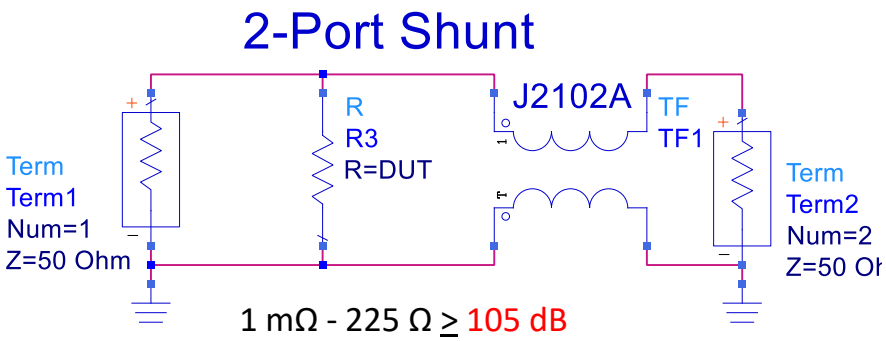
Capacitor Loading by the Decade

| | C | ESR | ESL |
|---|---|---|---|
| **C1** | 1 uF | 7 mΩ | 300 pH |
| **C2** | 0.10uF | 15 mΩ | 300 pH |
| **C3** | 0.01uF | 30 mΩ | 300 pH |
| **C4** | 0.001uF | 100 mΩ | 300 pH |
| **C5** | 100pF | 200 mΩ | 300 pH |

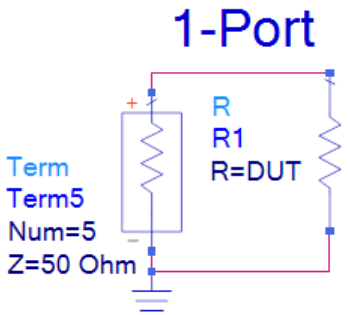


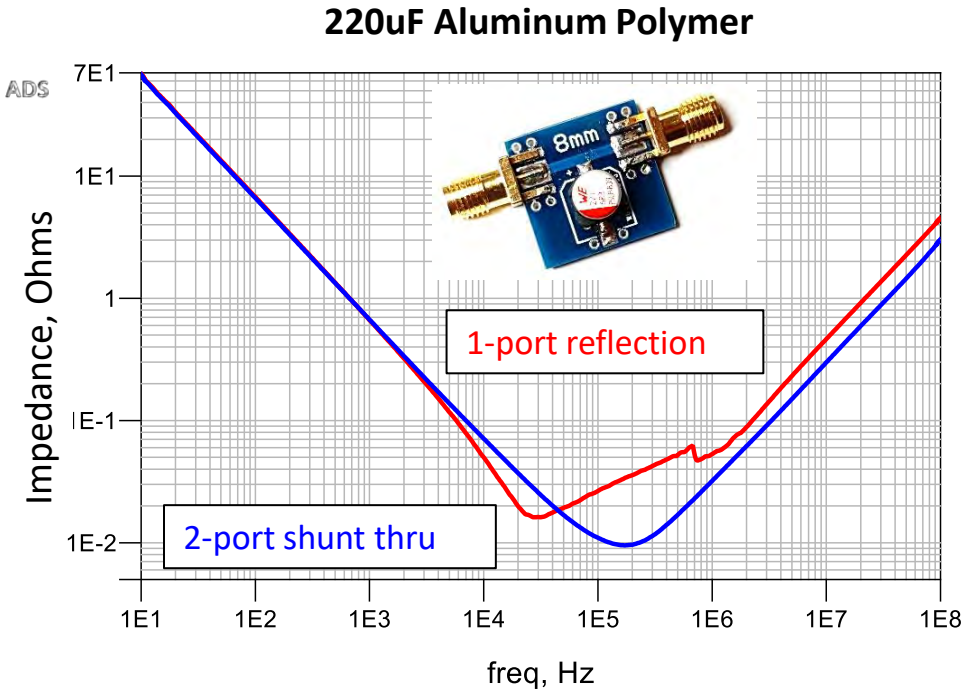
# 2-Port Shunt Impedance



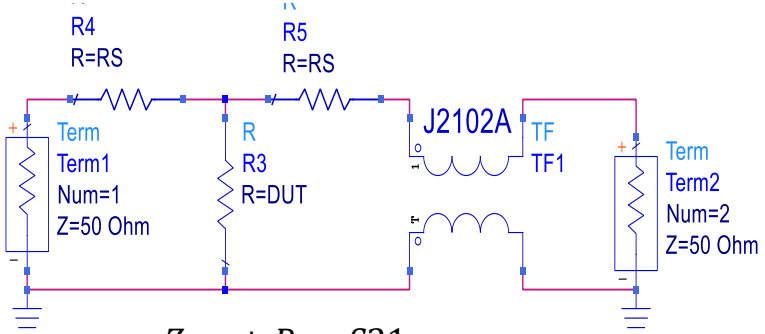

1 mΩ - 225 Ω ≥ 105 dB




1 Ω - 2 kΩ ≥ 66 dB



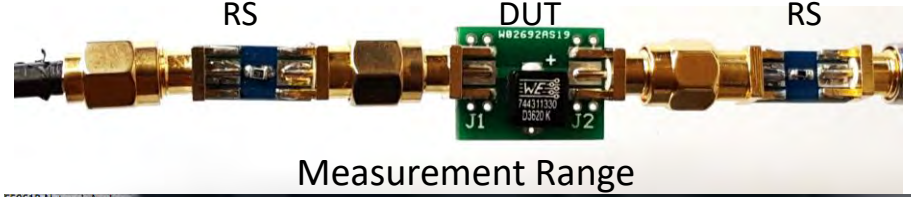
# Increase Port Impedance Shift the Measurement Range

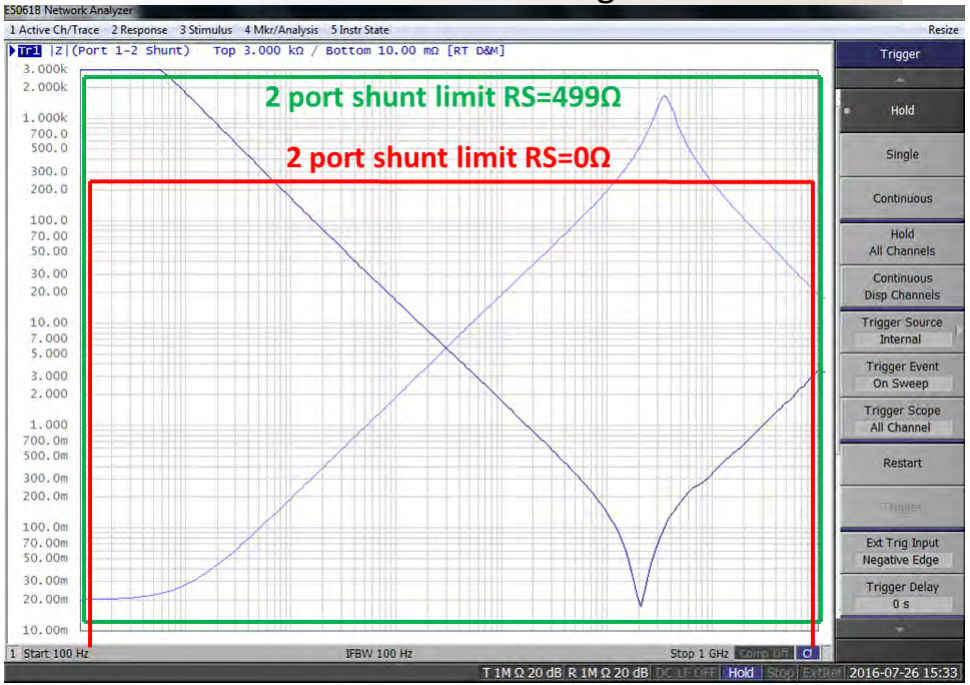



$$Z_{DUT} = \frac{Z_{ref} + R_s}{2} \frac{S21}{1 - S21}$$

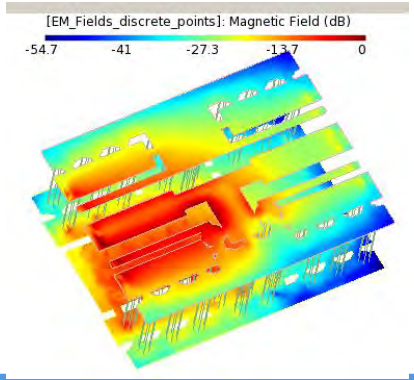
$$S21 = \frac{2 \cdot Z_{DUT}}{2 \cdot Z_{DUT} + Z_{ref} + R_s}$$

| Series Resistor | Min Z | Max Z |
|---|---|---|
| 200Ω | 5 mΩ | 1.125kΩ |
| 450Ω | 10 mΩ | 2.25kΩ |
| 499Ω | 11mΩ | 2.48kΩ |
| 950Ω | 20 mΩ | 4.5kΩ |

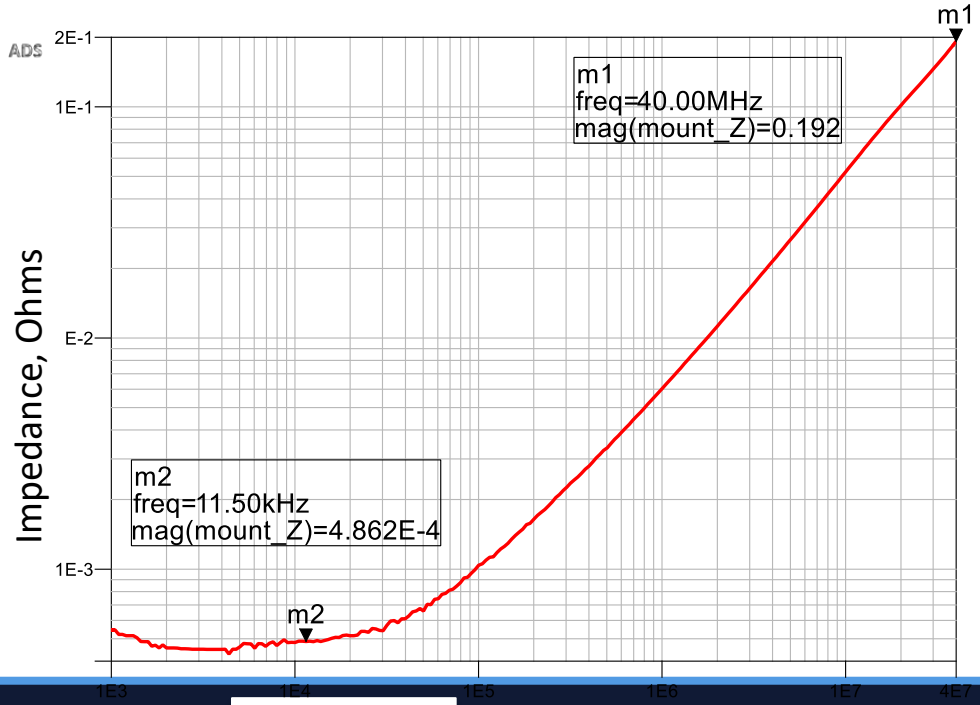


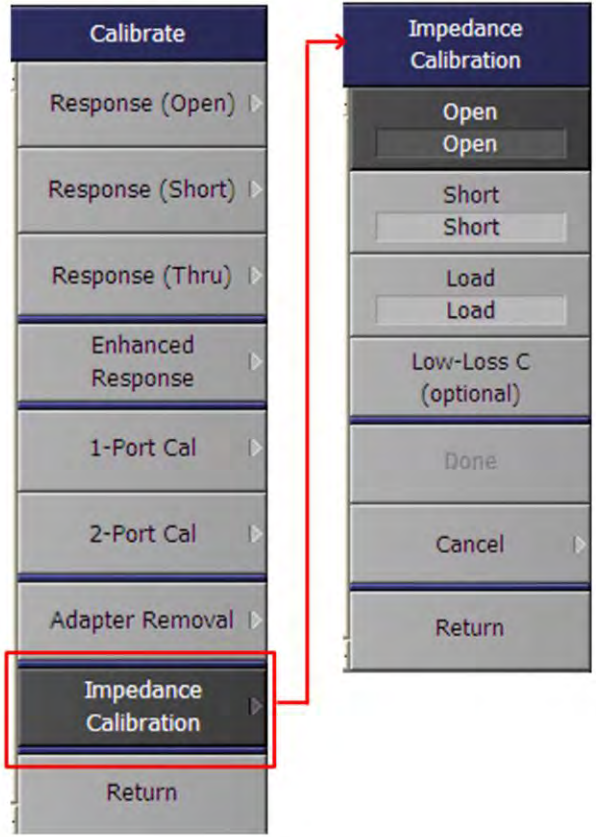
# Mounting Inductance Measured with Short to Ground

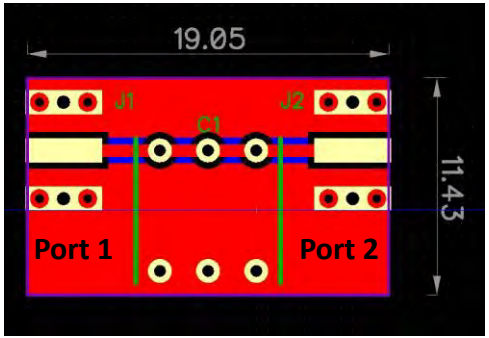




$$L_{mount} = \frac{0.192}{2\pi \cdot 40MHz} = 764pH$$

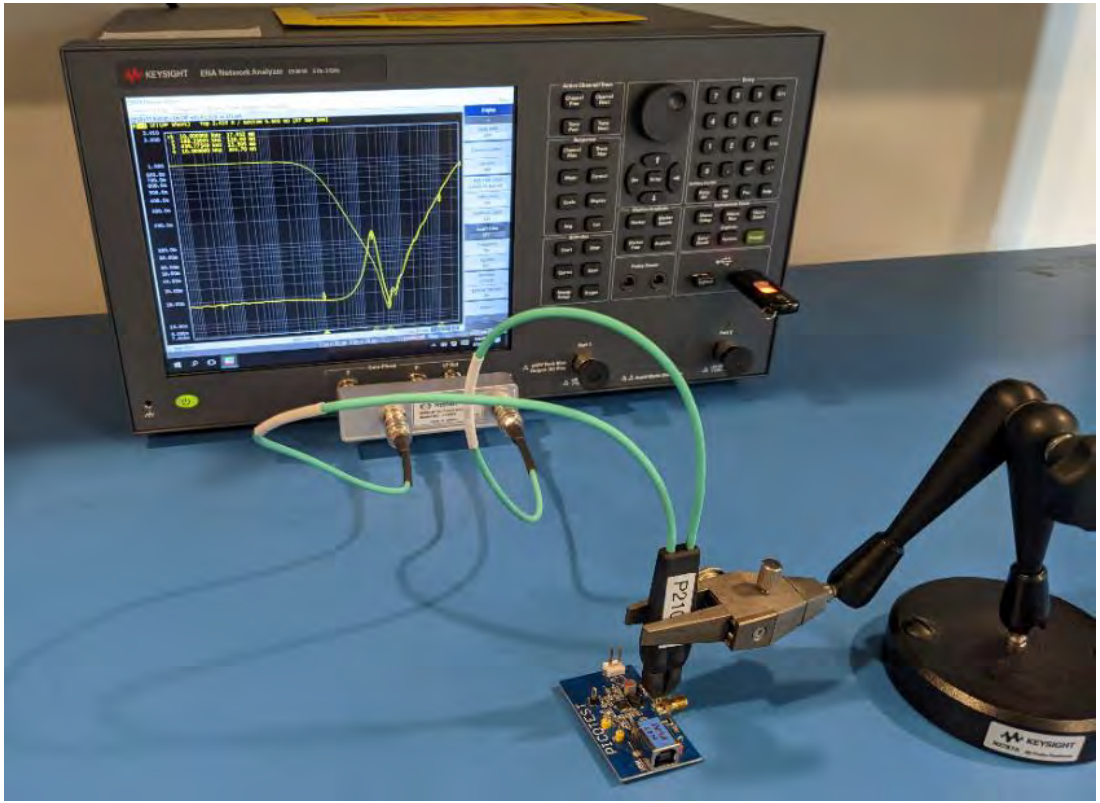


# 2-Port Shunt Impedance Setup Example

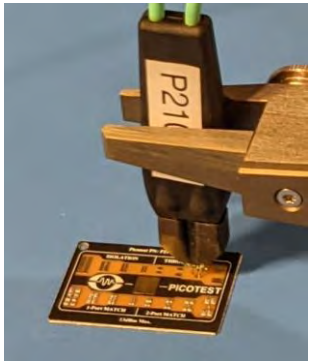



# 2-Port Shunt Impedance Browser Probe




Keysight E5061B and the Picotest P2102 Probe




SOL Calibration

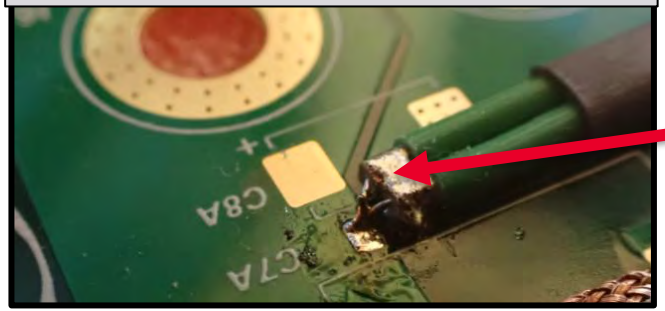
*Courtesy of Benjamin Dannan and Steve Sandler*

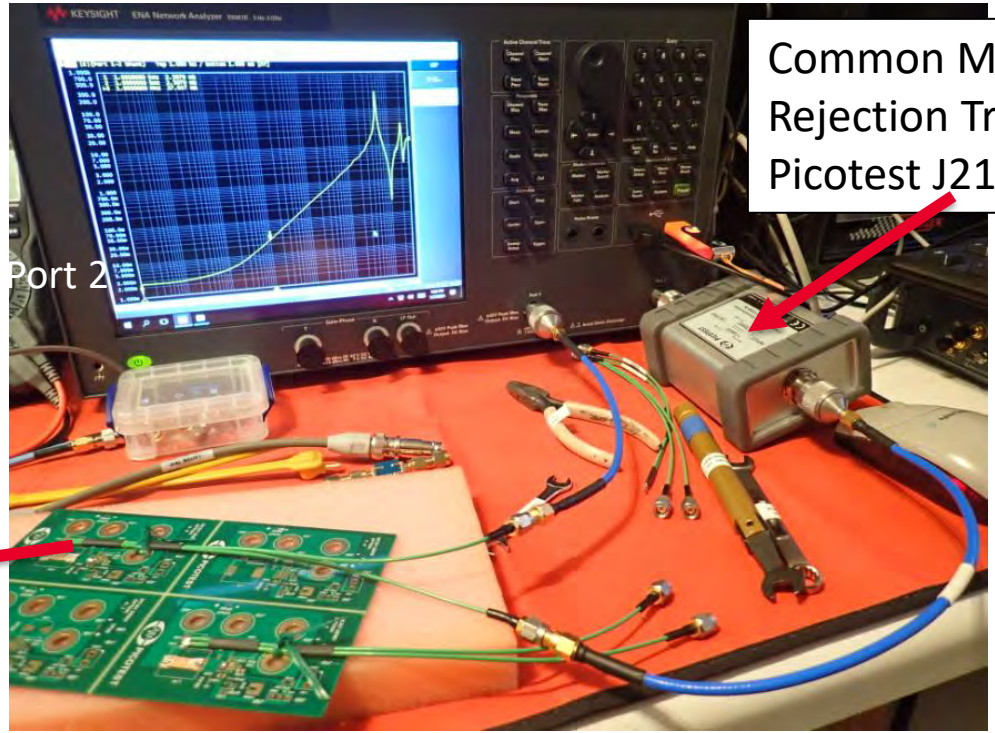
# Avoiding Ground Loops between Port 1 and Port 2

*High Frequency 5Hz to 3GHz S-parameter Ports*

Simple response thru calibration with the two soldered together cables before attaching to the DUT.

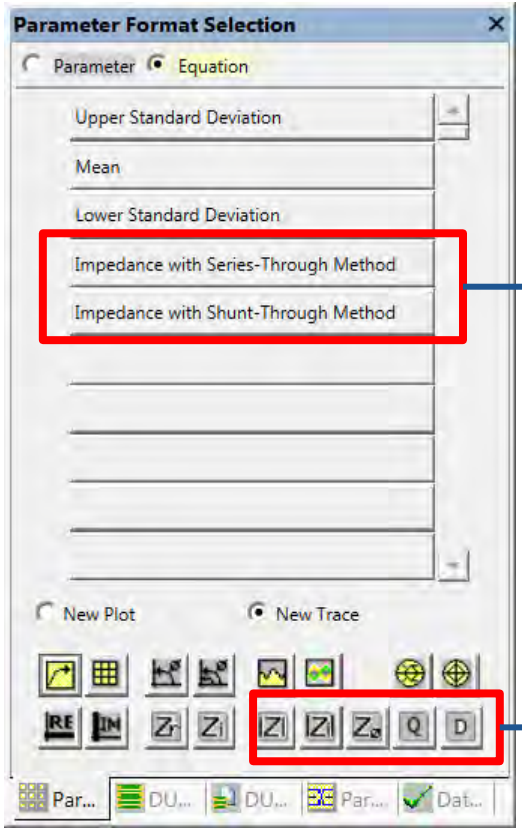
Two 50 Ohm Coax Cables Soldered together at the DUT






Common Mode Rejection Transformer Picotest J2102B

# VNA Tool Options for 2-Port Shunt Z:  PLTS Can Help


Python Equations:

a. For the Series-through method of measuring a power plane

$$Z_{DUT} = (50x2) \times ((1-S_{21})/S_{21})$$

b. For the Shunt-through method of measuring a power plane

$$Z_{DUT} = 50 \times S_{21} / (2 \times (1-S_{21}))$$

Five Power Integrity formats:

|Z|: impedance magnitude

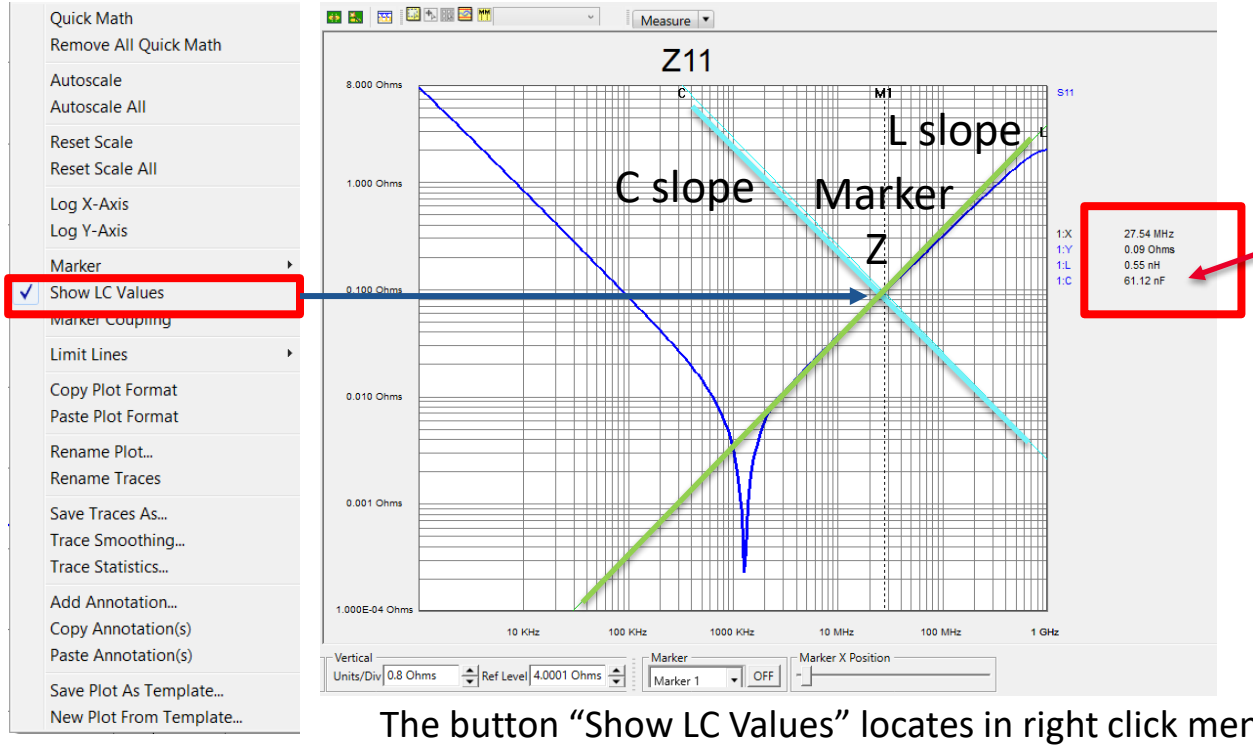
|Zi|: impedance imaginary magnitude

$Z_{\emptyset}$: impedance angle

Q : quality factor

D : dissipation factor

# Show LC Values for Power Integrity Measurements




- *Line up the C-slope to measure C*
- *Line up the L slope to measure L*

61nF

The button “Show LC Values” locates in right click menu.

The button only works for the new five impedance formats.

When it is selected, the L C value will be shown in marker.

# Remember

- Parallel L and C resonate in the time domain but are easier to find as impedance peaks in the frequency domain.

- Flat impedance minimizes the noise ripple by reducing the dynamic currents.

- Flat impedance is matched impedance with the simple rules of thumb based on $Z_0 = \sqrt{\frac{L}{C}}$

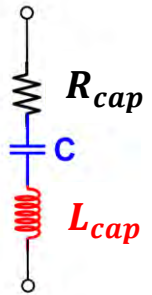
$$C_{Flat} = \frac{L_{VRM}}{R_{Target}{}^2} \qquad L_{PCB} = C_{Pkg} * R_{Target}{}^2$$

# Agenda

- **Why Flat Impedance is the Design Goal**
  - Worst case PDN noise ripple is not intuitive
- **How to Measure Power Rail Impedances in the Micro-Ohms**
  - 2-Port Shunt Impedance where $Z_{DUT}$ is a function of S21
- **What is Wrong with Capacitor Vendor Data**
  - Vendor data for capacitor ESL typically includes mounting inductance which needs to be removed for connecting to EM simulations.

# Capacitors Have Series L and Series R

**Capacitor Model**



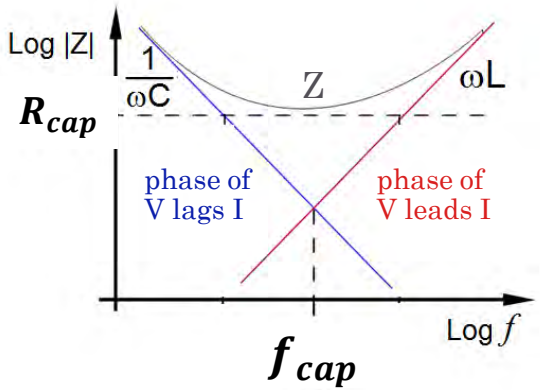

**Impedance Equation**

$$Z = R_{cap} + \left(j\omega L_{cap} - j\frac{1}{\omega C}\right)$$

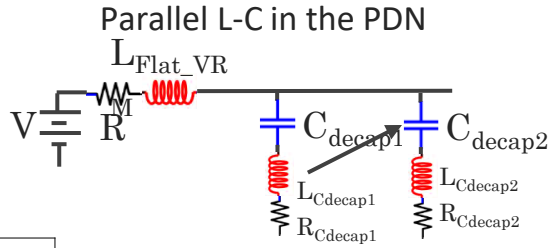
$$f_{cap} = \frac{1}{2\pi\sqrt{L_{cap} \times C}}$$

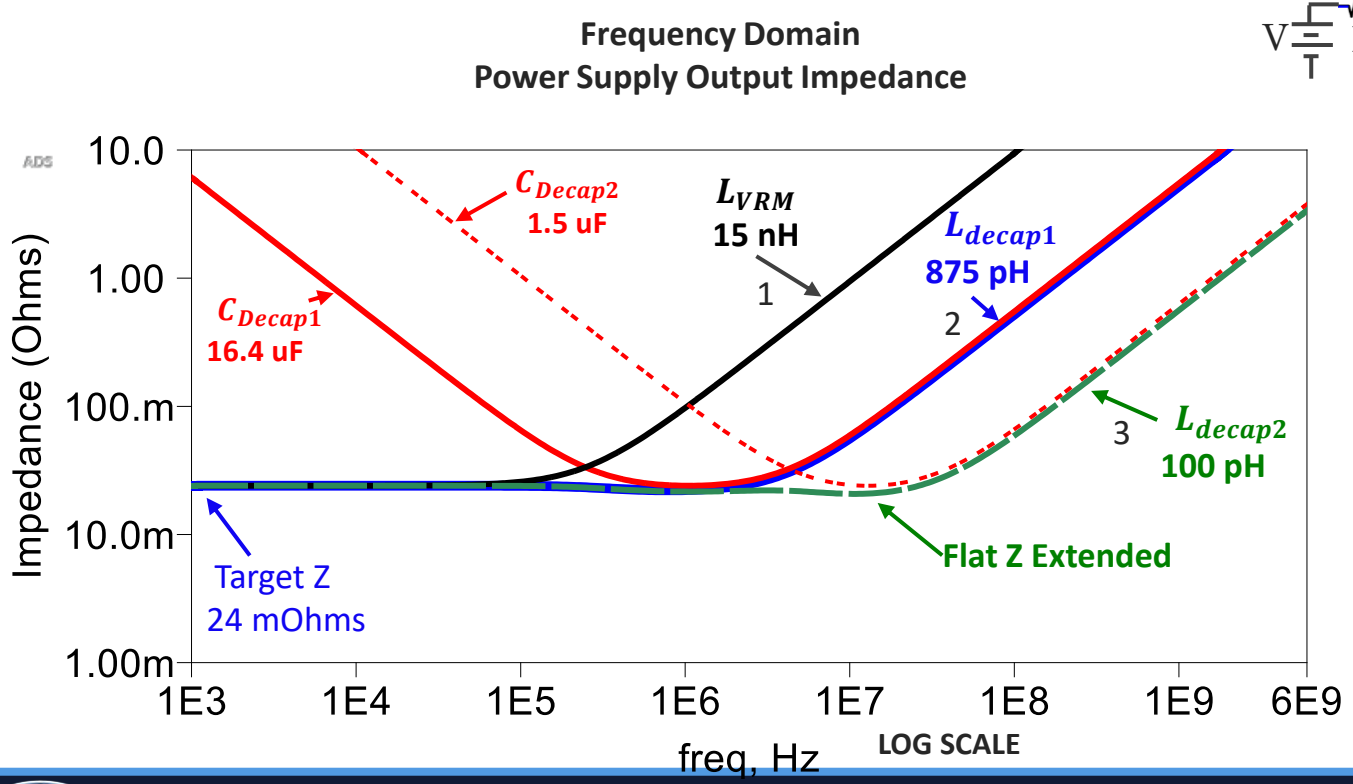
Voltage and current are in phase at $f_{cap}$

**Series RLC Impedance vs. Frequency**



# Adding Decoupling Capacitors to Reduce L



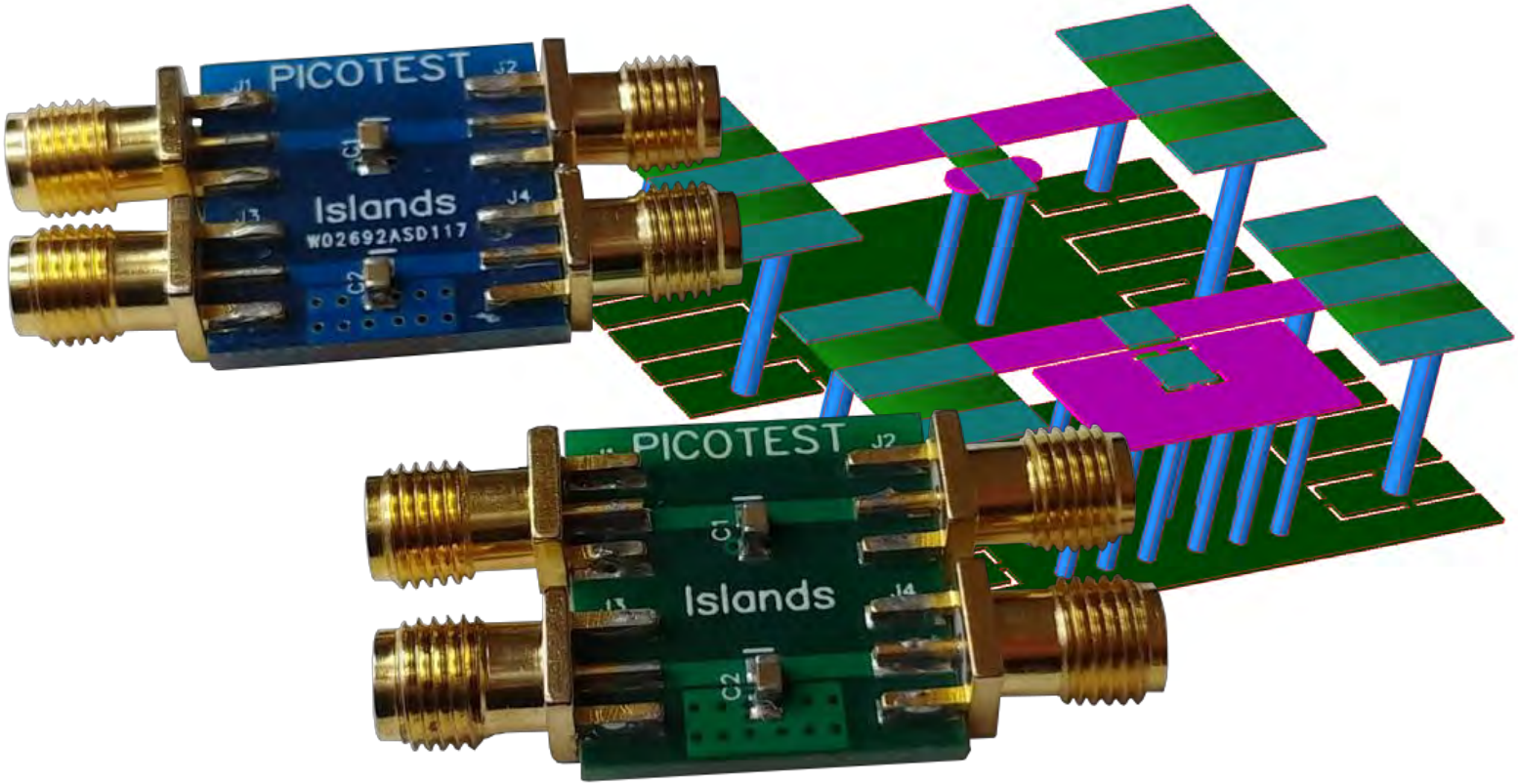




$$C_{decap2} = \frac{L_{decap1}}{Z_{Target}^2}$$

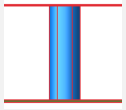
$$= \frac{875pH}{(24\ mOhm)^2}$$

$$\approx 1.5\ uF$$

# Surface Mount Capacitors with the Lowest L

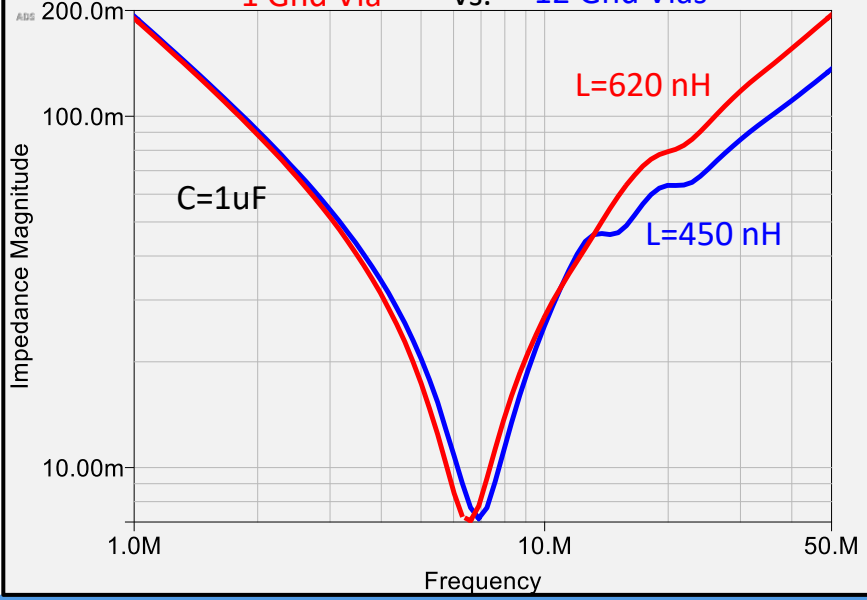


# Ground Vias and PCB Stack-up Reduce Inductance



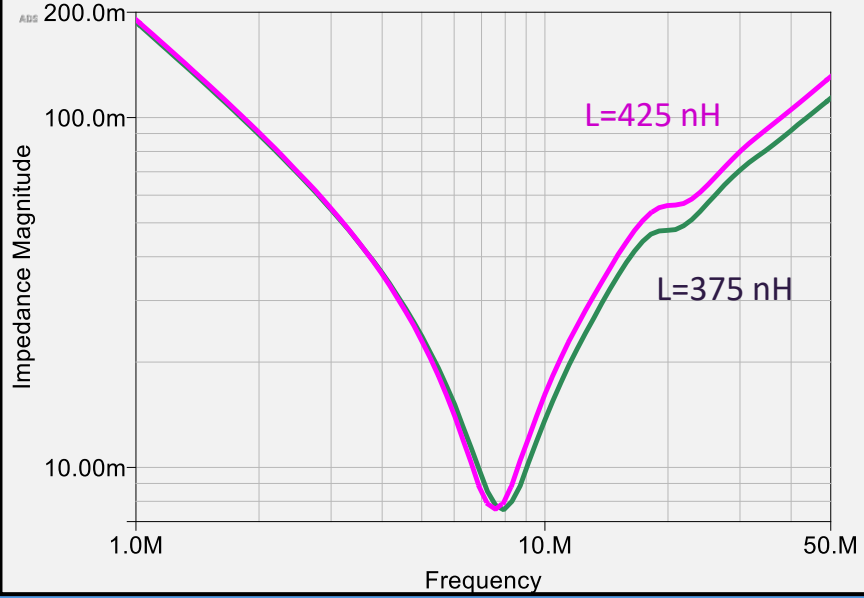
## 63 mil PCB Stack-up


1 Gnd Via vs. 12 Gnd Vias

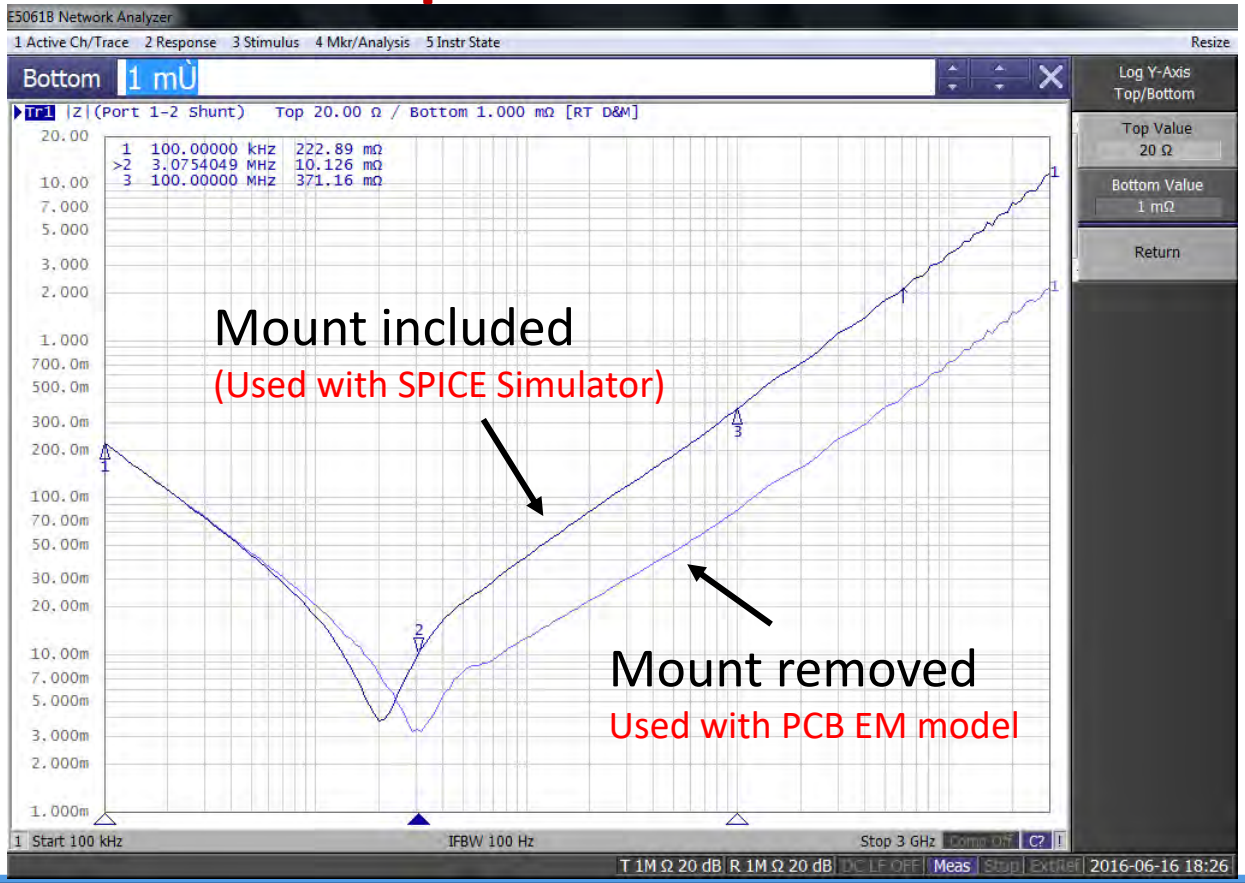




## 8 mil PCB Stack-up

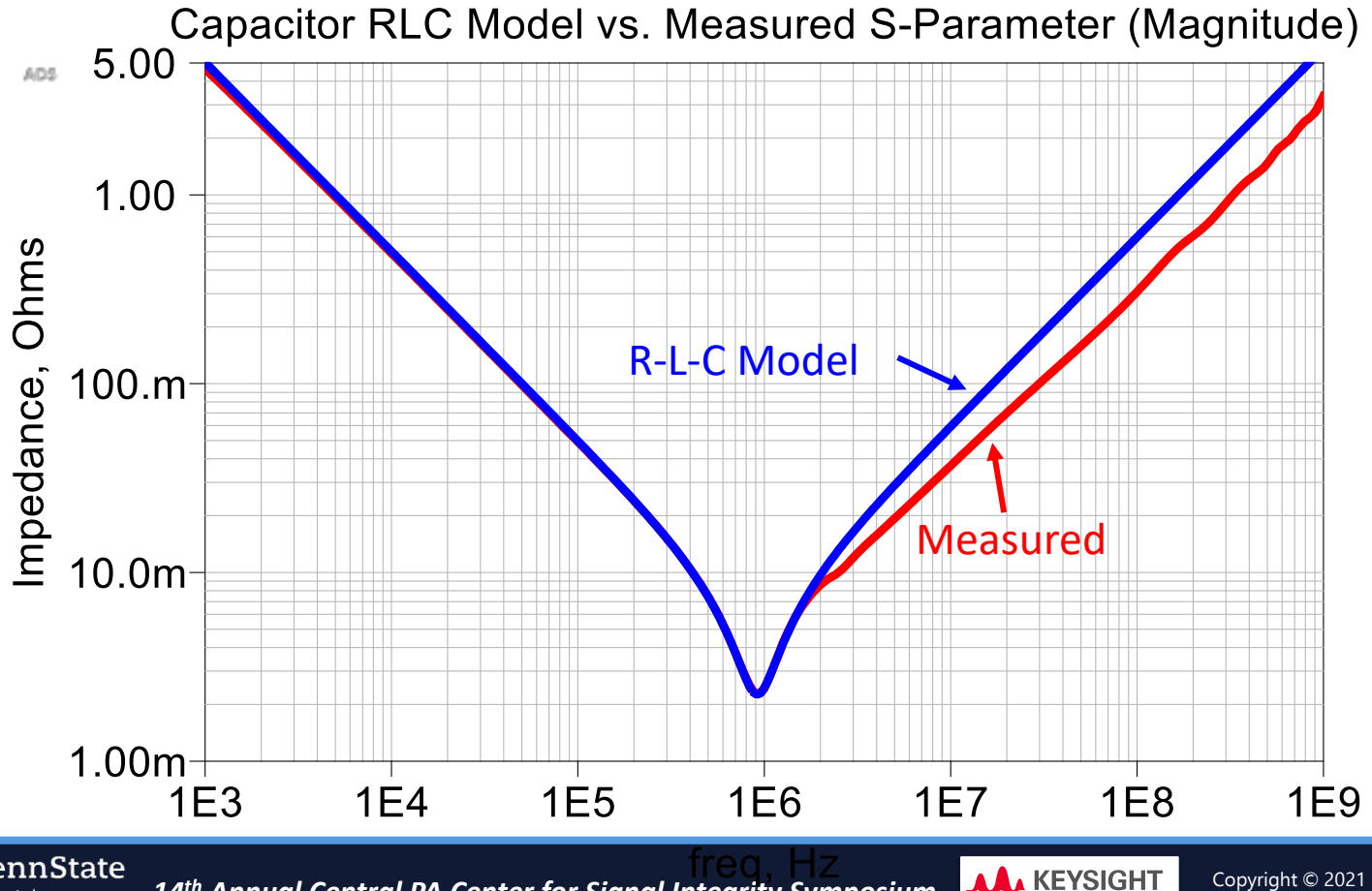

1 Gnd Via vs. 12 Gnd Vias

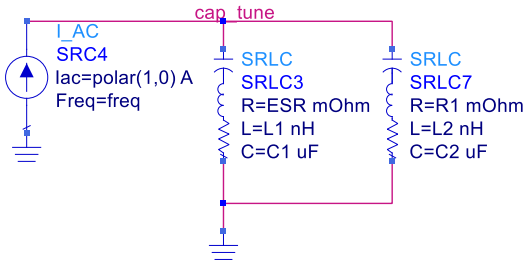
# How to Measure the Capacitor…..



# Series R-L-C Model Doesn't Match the Measurement

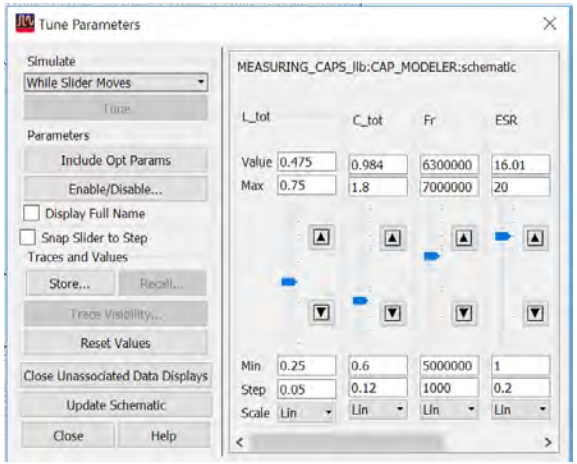


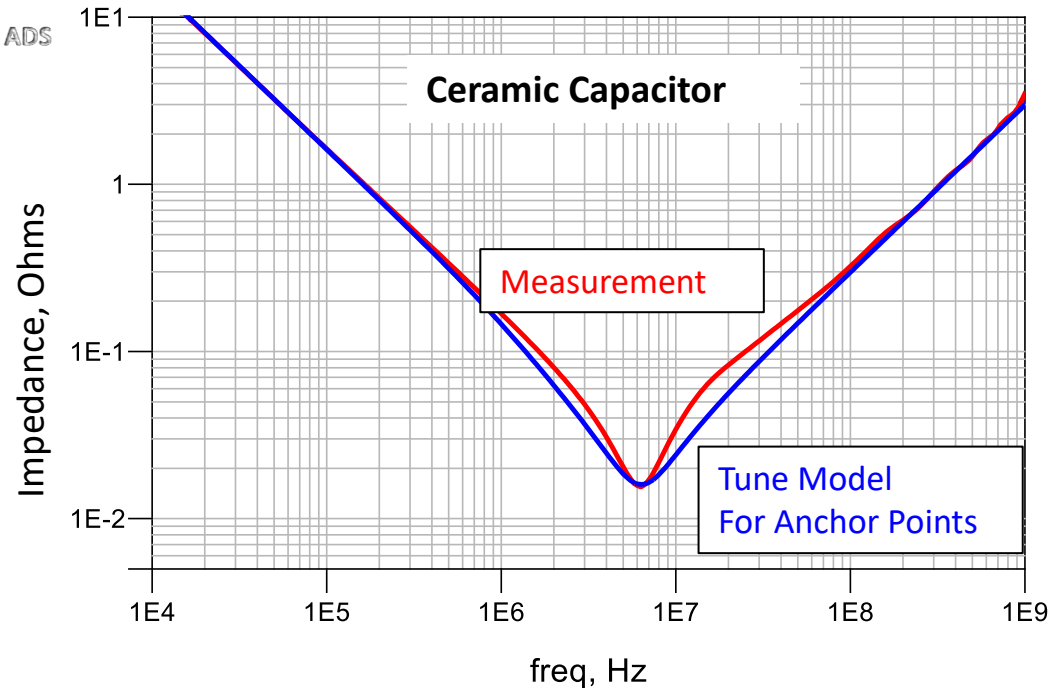
# Ceramic Capacitors Can be Modeled as Parallel Caps



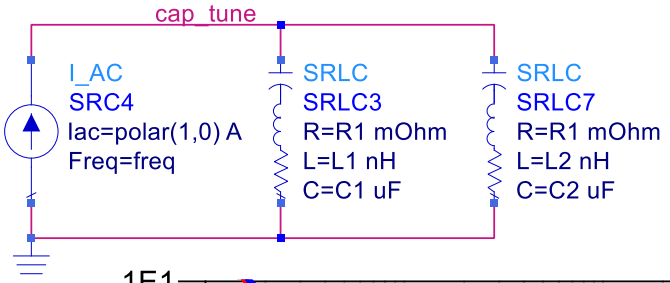

Anchor values

Var Eqn VAR
VAR1
L_tot=0.475 {t}
C_tot=0.984 {t}
Fr=6300000 {t}
ESR=16.01 {t



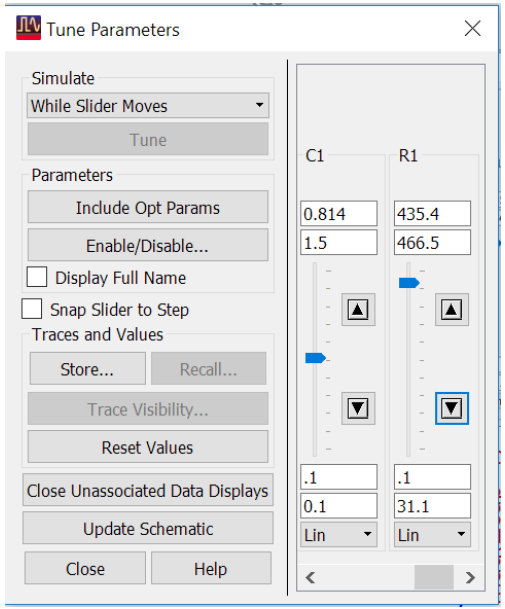
# After Tuning

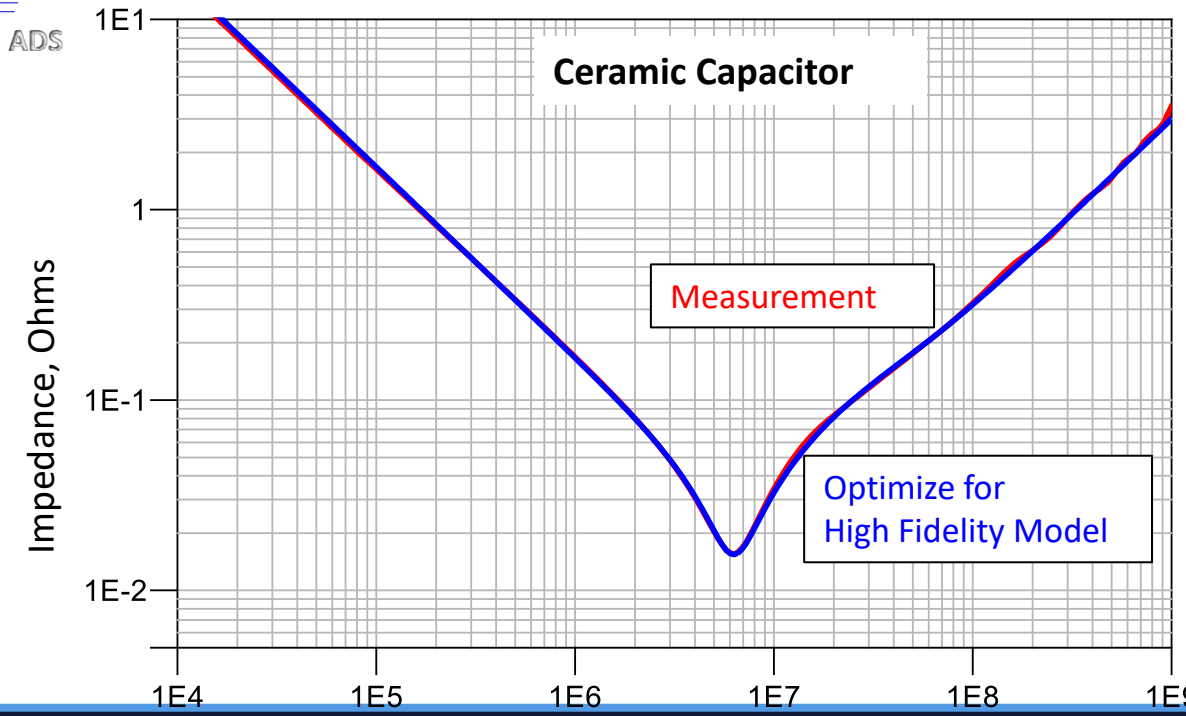



Shaping values

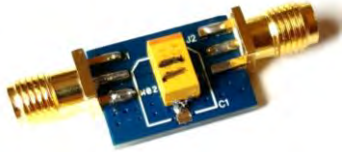
Var Eqn

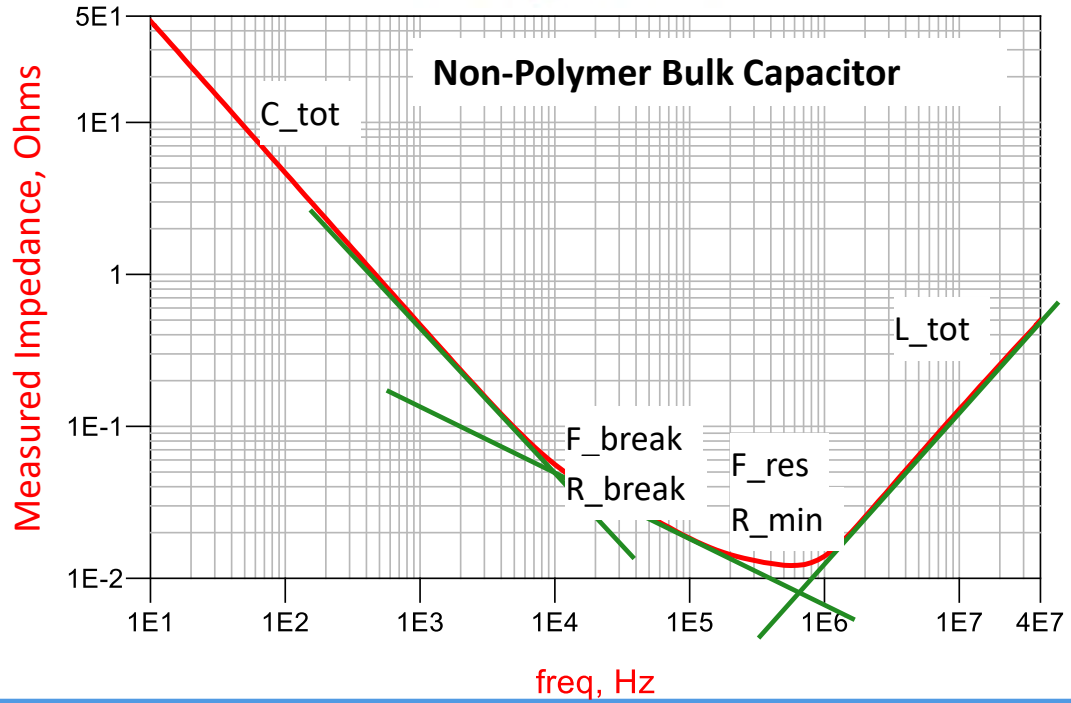
VAR
VAR3
C1=0.75 {t}
R1=311 {t}



# Tantalum Capacitors Require a Different Model



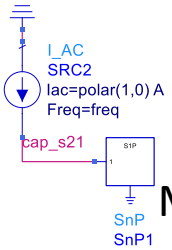



Default values and tuning

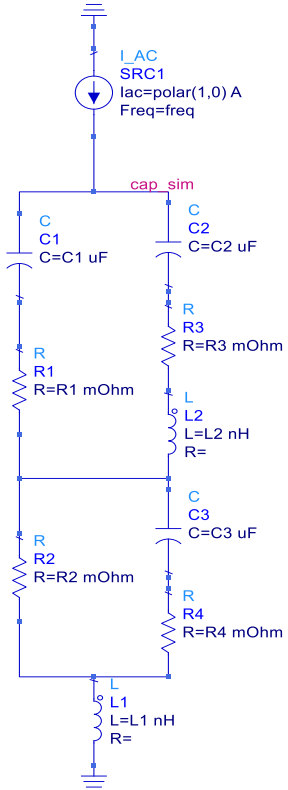
Var Eqn
VAR
VAR6
C1=K1*1E9/(8.89*F_break*R_break)
R2=K2*R_res
L2=K3*5E15/(39.5*F_res*F_res*C_tot)
C3=K4*1E9/(15*F_res*R2)
R4=K5*R_res
R3=K6*R_res

Anchor values

Var Eqn
VAR
VAR9
L_tot=1.76 {t}
C_tot=330 {t}
F_break=11520 {t}
R_break=42 {t}
F_res=600000 {t}
R_res=12 {t}

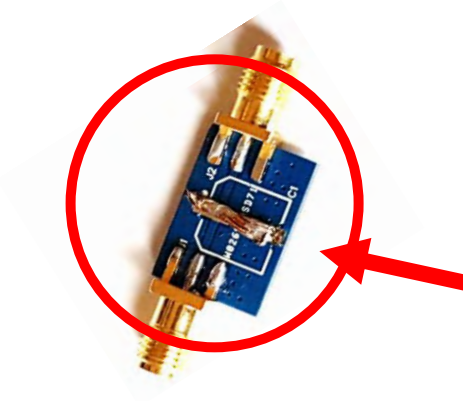


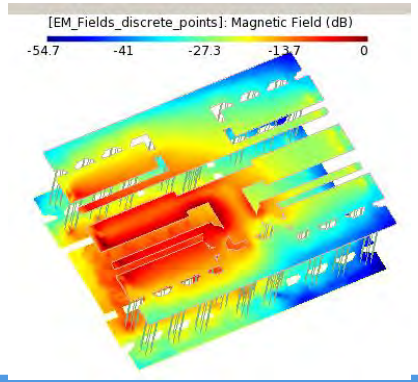

Measurement



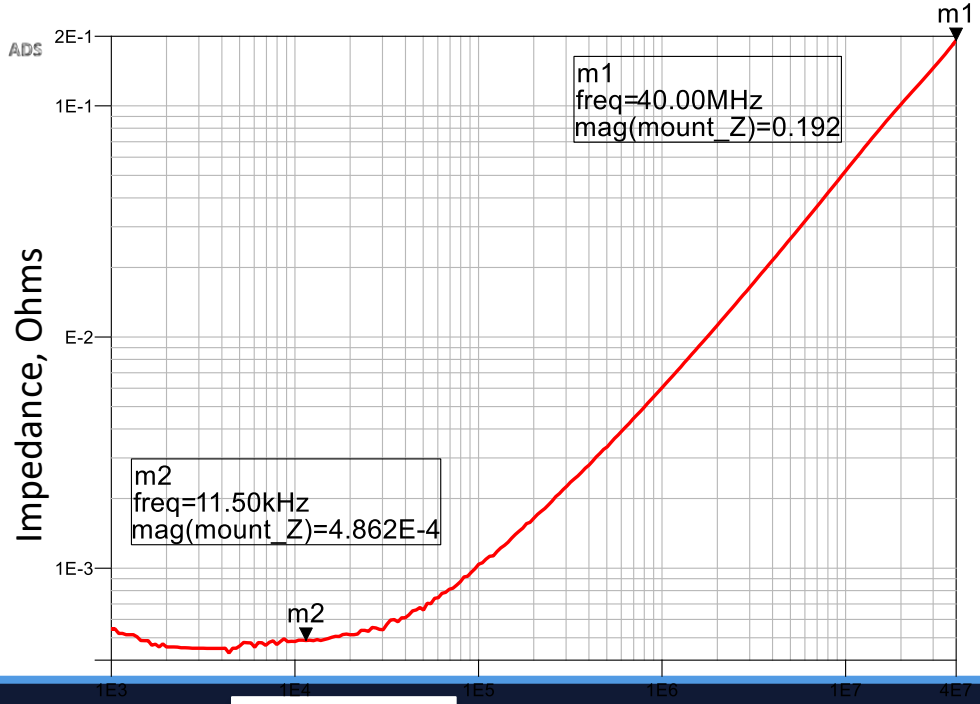

Model

# Mounting Inductance Can be Added as R-L to Ground




$$L_{mount} = \frac{0.192}{2\pi \cdot 40MHz} = 764pH$$



# An Optimizer Avoids Tedious Hand Tuning and Guessing

Meas Eqn

```
MeasEqn
cap_err
cap_err=mag(cap_meas)-mag(cap_sim)
cap_meas=cap_s21*25/(1-cap_s21)
```

GOAL

```
Goal
OptimGoal1
Expr="cap_err"
SimInstanceName="AC1"
Weight=1
LimitName[1]="limit1"
LimitType[1]="EqualTo"
LimitMin[1]=0
LimitMax[1]=0
```

OPTIM

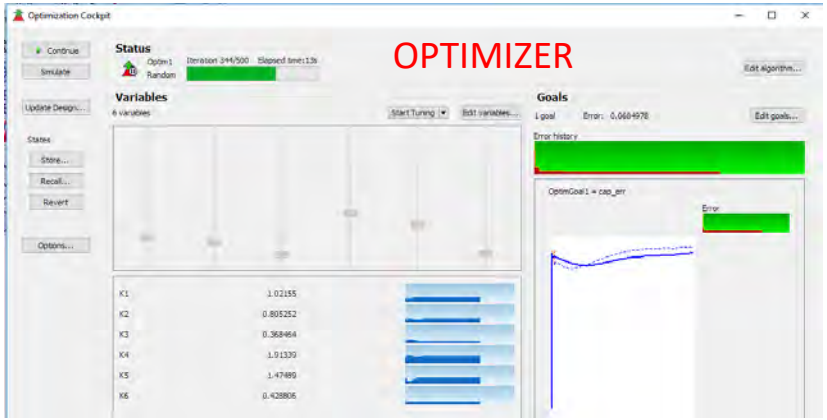
```
Optim
Optim1
OptimType=Random
MaxIters=1000
UseAllOptVars=yes
UseAllGoals=yes
GoalName[1]=
SaveAllTrials=no
```

## Before OPT

Shaping values

Var Eqn

```
VAR
VAR12
K1=1 {t} {o}
K2=1 {t} {o}
K3=1 {t} {o}
K4=1 {t} {o}
K5=1 {t} {o}
K6=1 {t} {o}
```



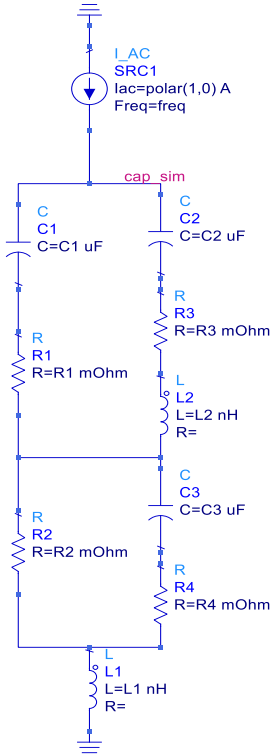

## After OPT

Shaping values

Var Eqn

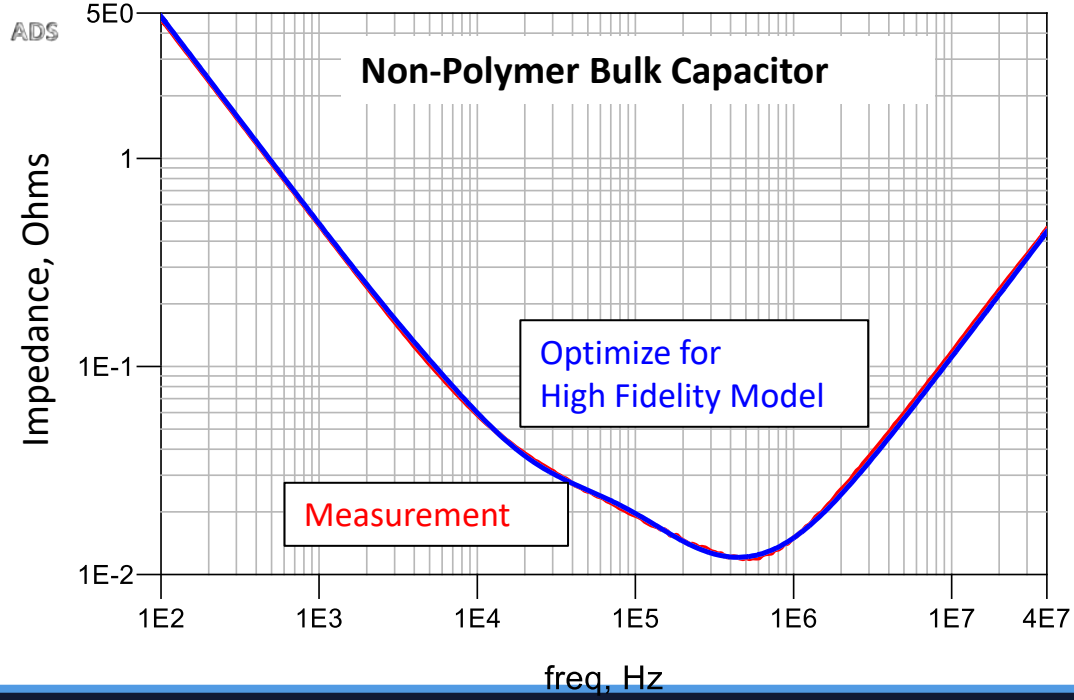
```
VAR
VAR11
K1=1.00876 {t} {o}
K2=0.837194 {t} {o}
K3=0.41982 {t} {o}
K4=2.09546 {t} {o}
K5=1.56776 {t} {o}
K6=0.409425 {t} {o}
```

# After Optimization



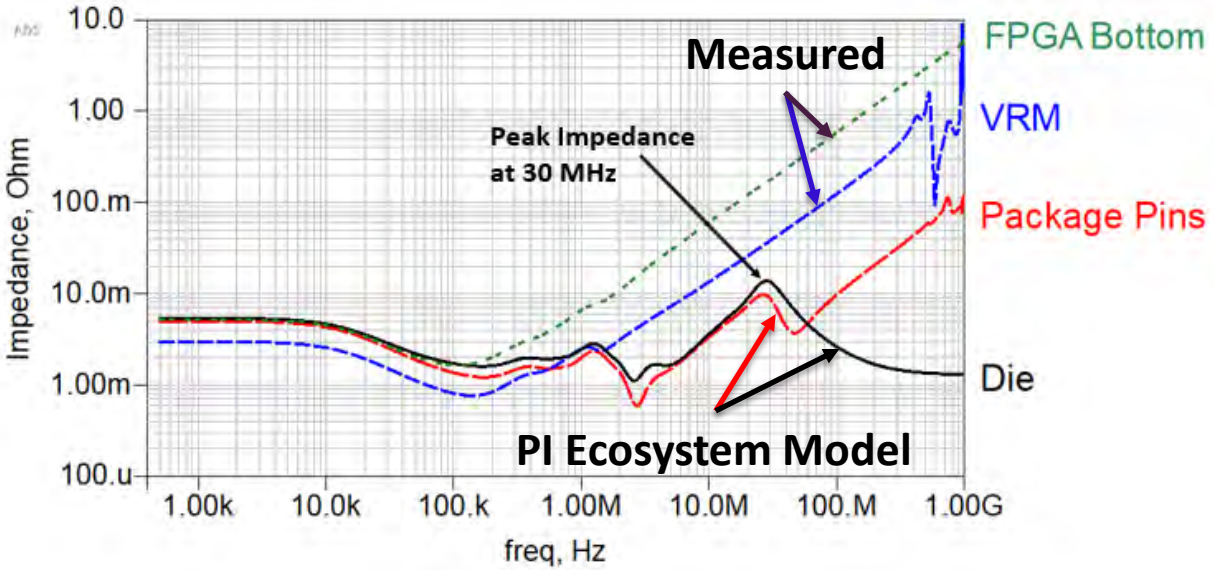

OPTIMIZER DETERMINED COMPONENT VALUES

| C1_val | C2_val | C3_val | L1_val | L2_val | R1_val | R2_val | R3_val | R4_val |
|---|---|---|---|---|---|---|---|---|
| 234.522 | 95.478 | 23.176 | 1.760 | 0.447 | 30.000 | 10.046 | 4.913 | 18.813 |



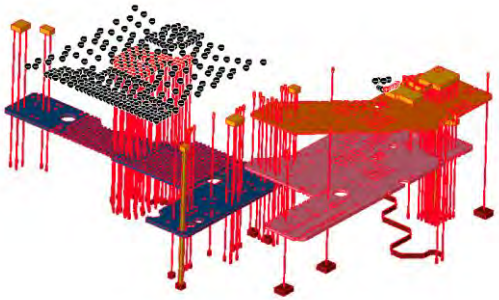
# FPGA Package/Die, PCB PDN EM, and Capacitor Models are Critical

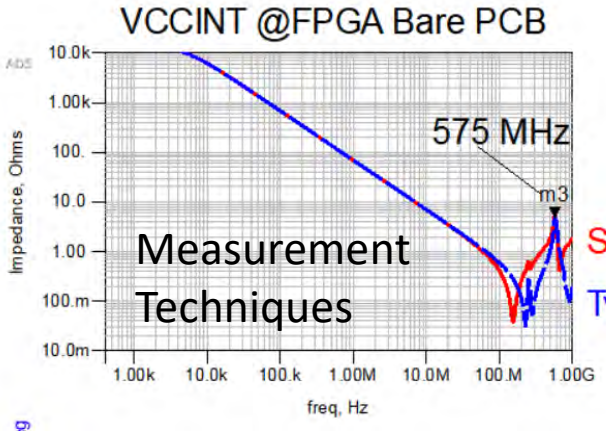
***Impedance measurements did not see the resonance at 30 MHz!***




- Decoupling capacitors dominate the impedance of the VCCINT PDN.
- Measurements with VCCINT are only accessible on the bottom side of the FPGA and include the via inductance.
- PIPro PDN EM model with package/die (CPM) in ADS schematic accurately predicts impedance peak that measurement could not see.

# PCB PDN Model

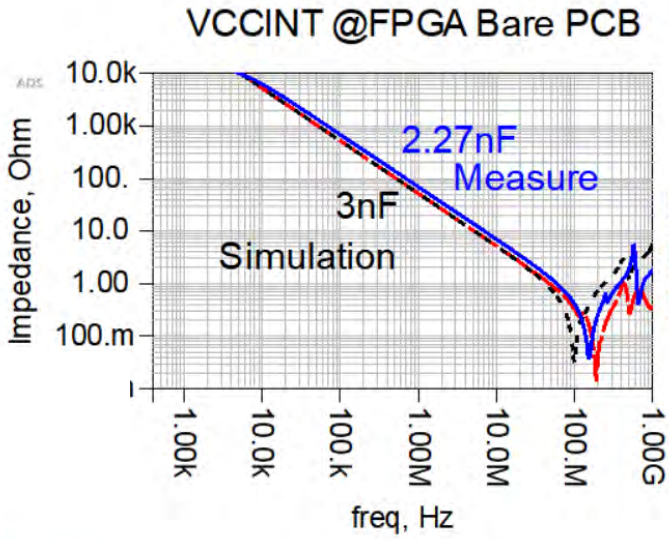





Same Side Probing

Two Sided Probing

## Simulation vs. Measurement



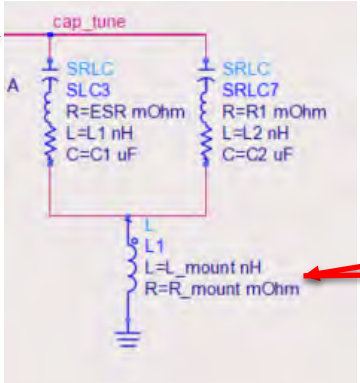

Measure_Via_Bottom

PIPro FPGA Via Bottom

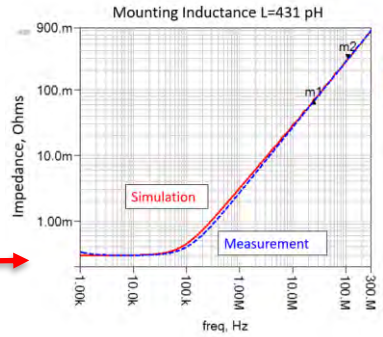
PIPro at VRM C1269

# Capacitor Models without Mounting Inductance

S11

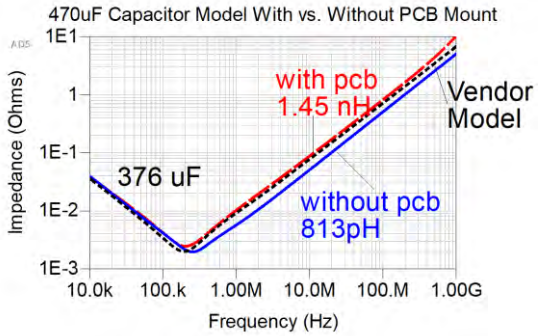


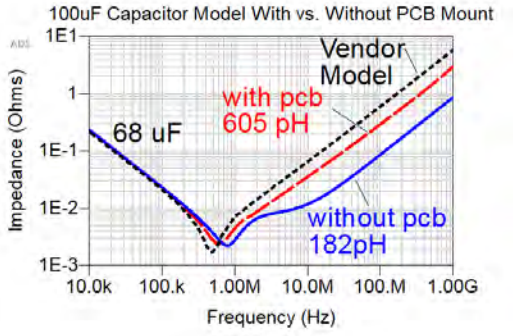

**PCB EM Model includes this… remove from capacitor model.**

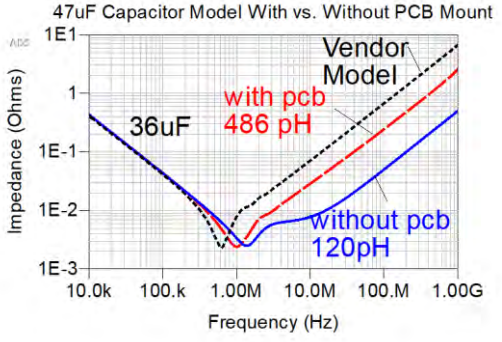




Shorted to Ground

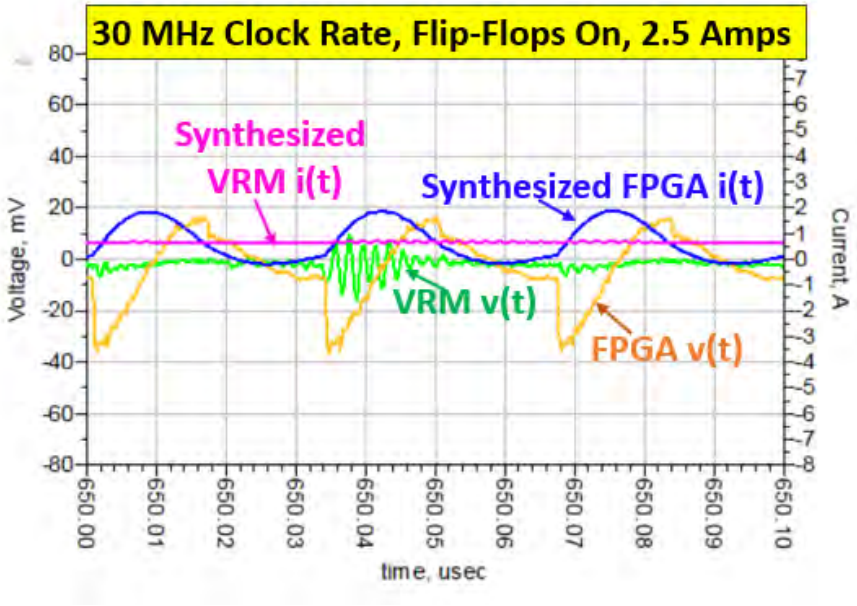


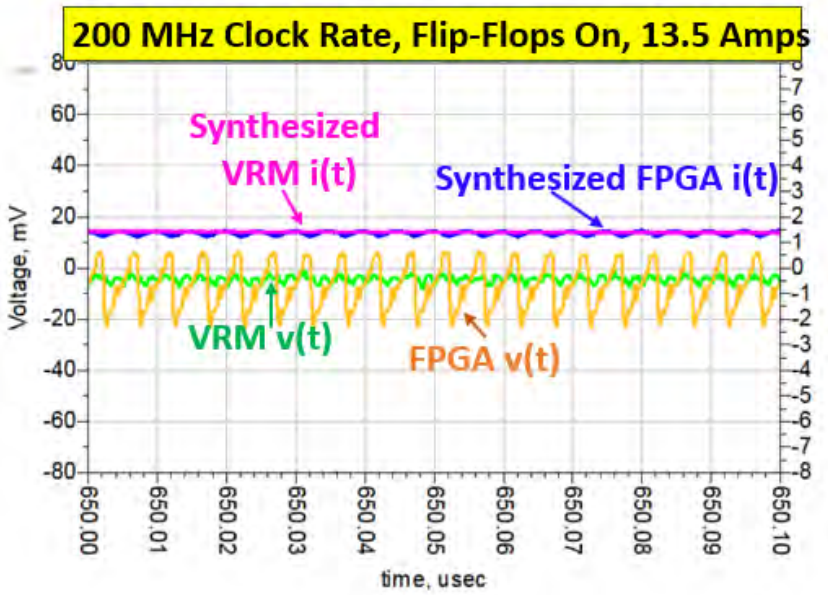



# Measured Data Confirms the Simulated Results

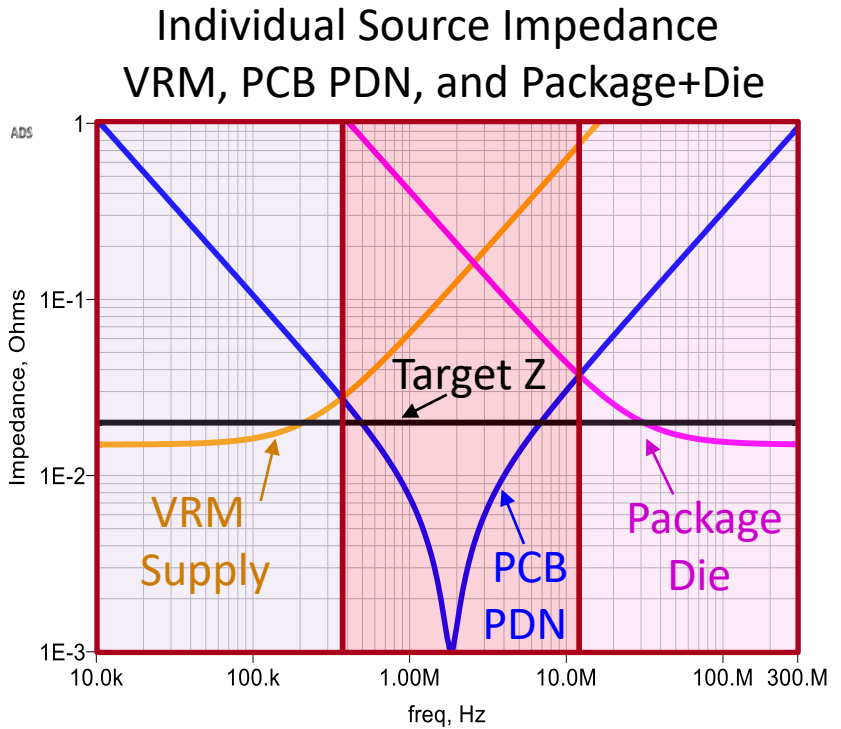
***Power Integrity is not intuitive! Simulation with measurement enables predictive models for design optimization and troubleshooting ☺***



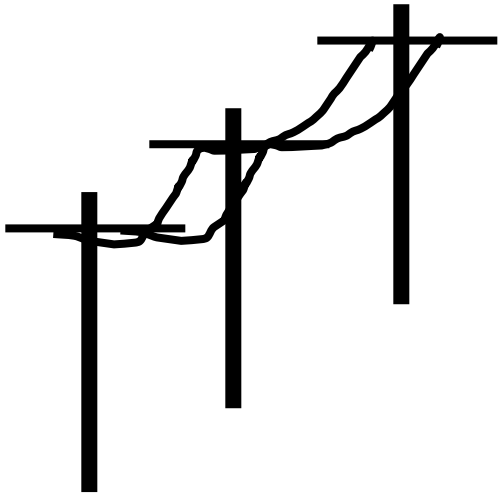
# Summary

- Flat impedance is the PI design goal!
- Learn how to make 2-port shunt impedance measurements to get good models, verify simulations, and debug noise problems.
- Beware of vendor capacitor models….avoid double counting the mounting inductance when used with EM models of the PCB.



# History Lesson – The Transatlantic Cable

## Engineered design vs. Costly Debug/redesign



*What is so hard about stringing a wire between the transmitter and the receiver?*

***Where was the SI Engineer in 1858?***

**Transatlantic telegraph cable**

In 1858…signal quality declined rapidly, slowing transmission to an almost unusable speed. The cable was destroyed the following month when Wildman Whitehouse applied excessive voltage to it while trying to achieve faster operation.

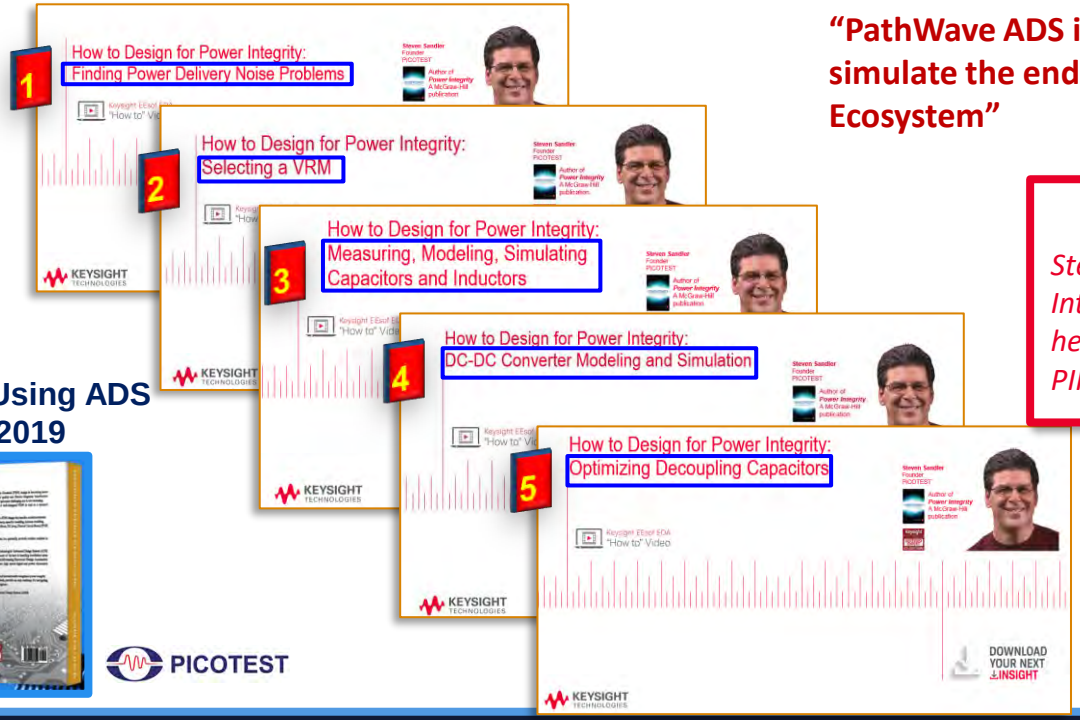
# Questions For Your Next Design

**PI Engineers require simulation and measurement tools**

1. Are your designs still leveraging decade capacitor values?
2. Are poor designs band-aided with added filters and more capacitors?
3. Where is the PI engineer?

# PathWave ADS Simulates the Power Integrity Ecosystem

## How to Design for Power Integrity
### 5 Part Series on YouTube




**Power Integrity Using ADS**
**Published 2019**

PICOTEST

Keysight CERTIFIED EXPERT EDA SOFTWARE

**Steve Sandler, Founder of Picotest**
*Over 40 years of experience in Power Electronics*

**"PathWave ADS is the only tool that can simulate the end to end Power Integrity Ecosystem"**

**KEY TAKE AWAY**

*Steve Sandler is an expert at Power Integrity Ecosystem simulations, and he does it all in PathWave ADS with PIPro!*

# Resources:


- H. Barnes, J. Carrel, S. Sandler, “A Method for Dynamic Load Current Testing with a Benchtop Power Supply” DesignCon 2020.
- Keysight sponsored “How to Design for Power Integrity” YouTube video series with Steve Sandler of Picotest: http://www.keysight.com/find/how-to-videos-for-pi
- Keysight PathWave ADS for Power Integrity: https://www.keysight.com/us/en/products/software/pathwave-design-software/pathwave-advanced-design-system/pathwave-ads-high-speed-digital-design.html
- Picotest Power Integrity Measurement Test Accessories: www.Picotest.com
- Xilinx ZCU104 Evaluation Kit: https://www.xilinx.com/products/boards-and-kits/zcu104.html


# Acknowledgements-


**Co-collaborators Steve Sandler of Picotest and Jack Carrel of Xilinx**

# Thank you!

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## QUESTIONS?