PCB Effects for Power Integrity

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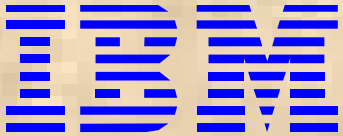
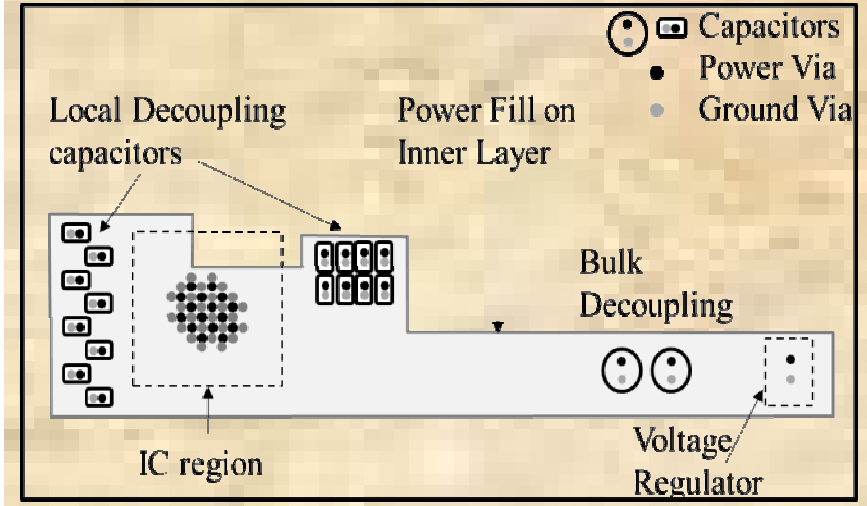
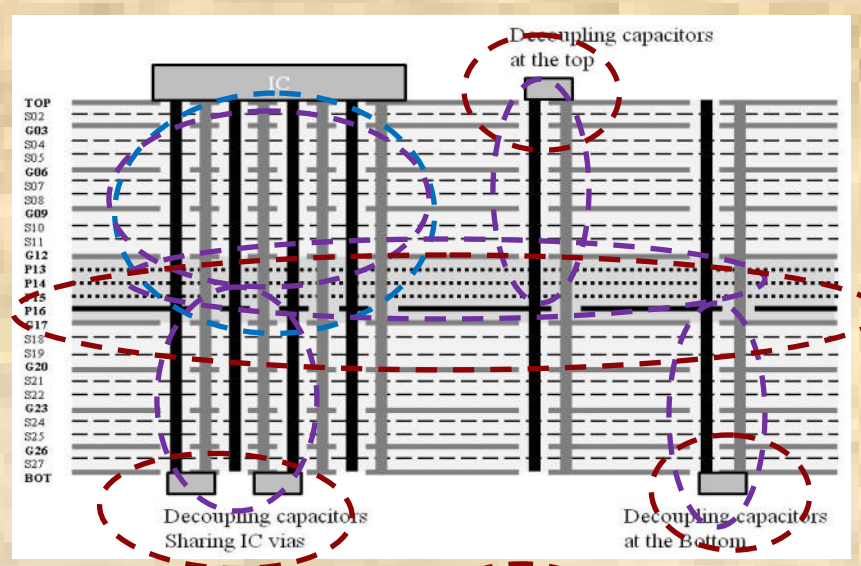


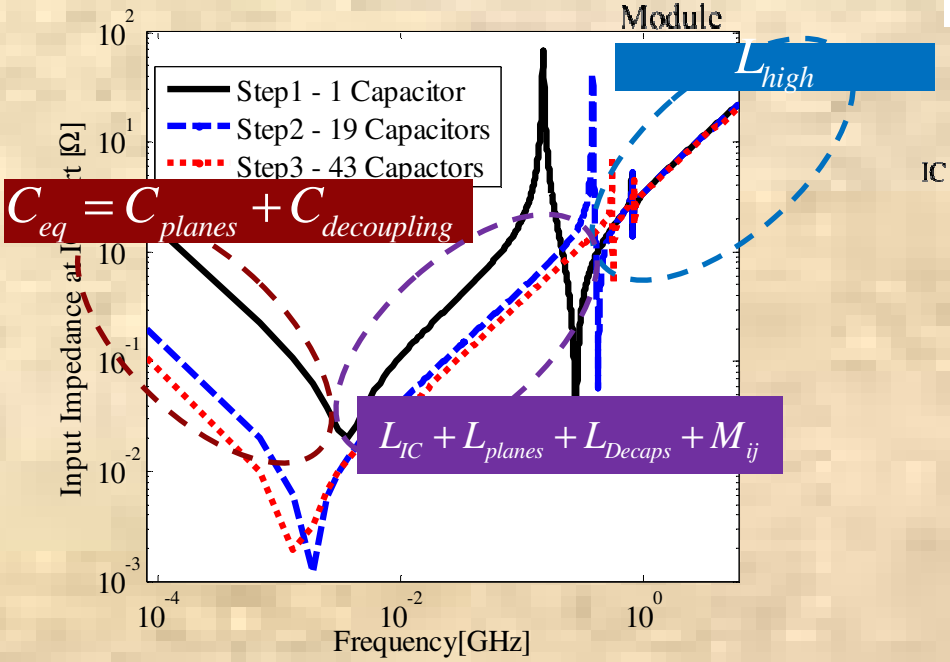
PCB Issues for Optimum Power Integrity

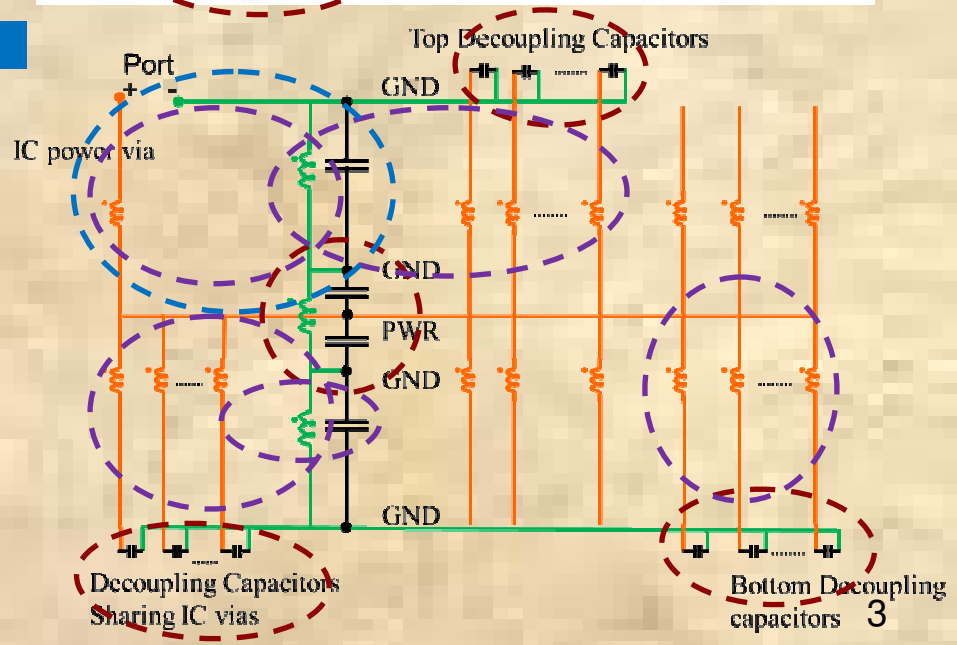
- Inductance dominates performance
  - Which inductance? Under what circumstances?
- Effect of capacitance value
- Effect of number of capacitors
- Effect of capacitor density
- Effect of capacitor via configuration
- Case Study

Design Geometry, Current Path, and Z_{PDN}









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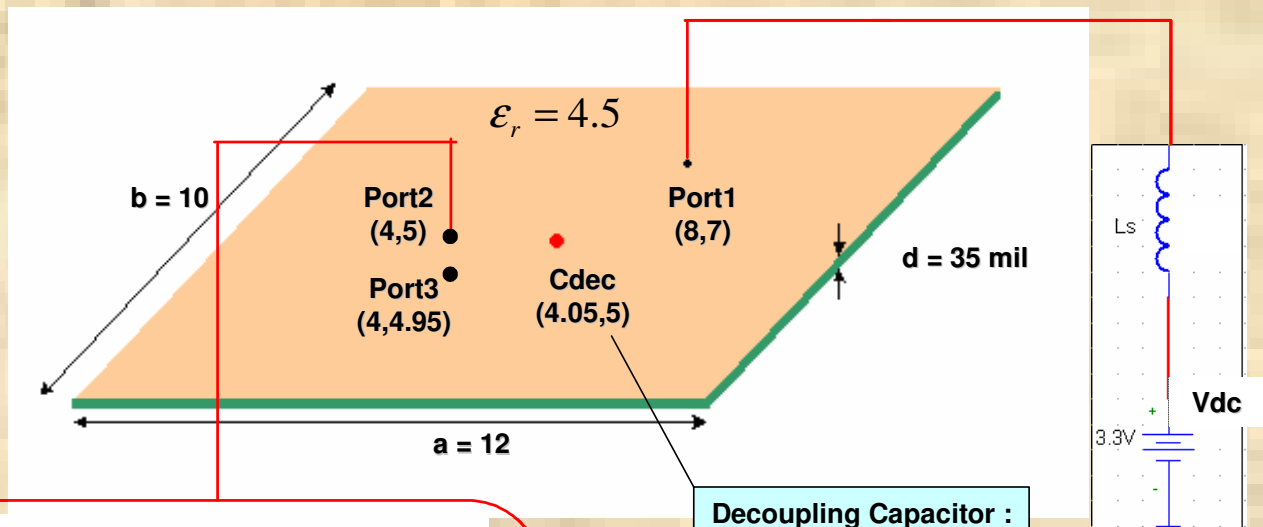
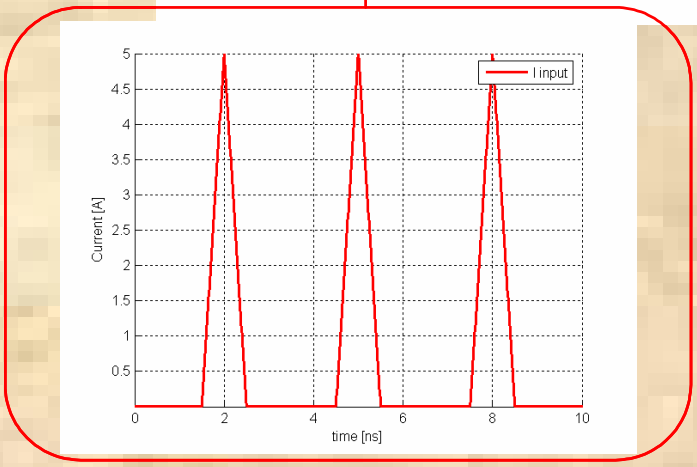
Model for Plane Recharge Investigations





Decoupling Capacitor :
C = 1uF
ESR = 30mOhm
ESL = 0.5nH

DC voltage used to charge the power plane

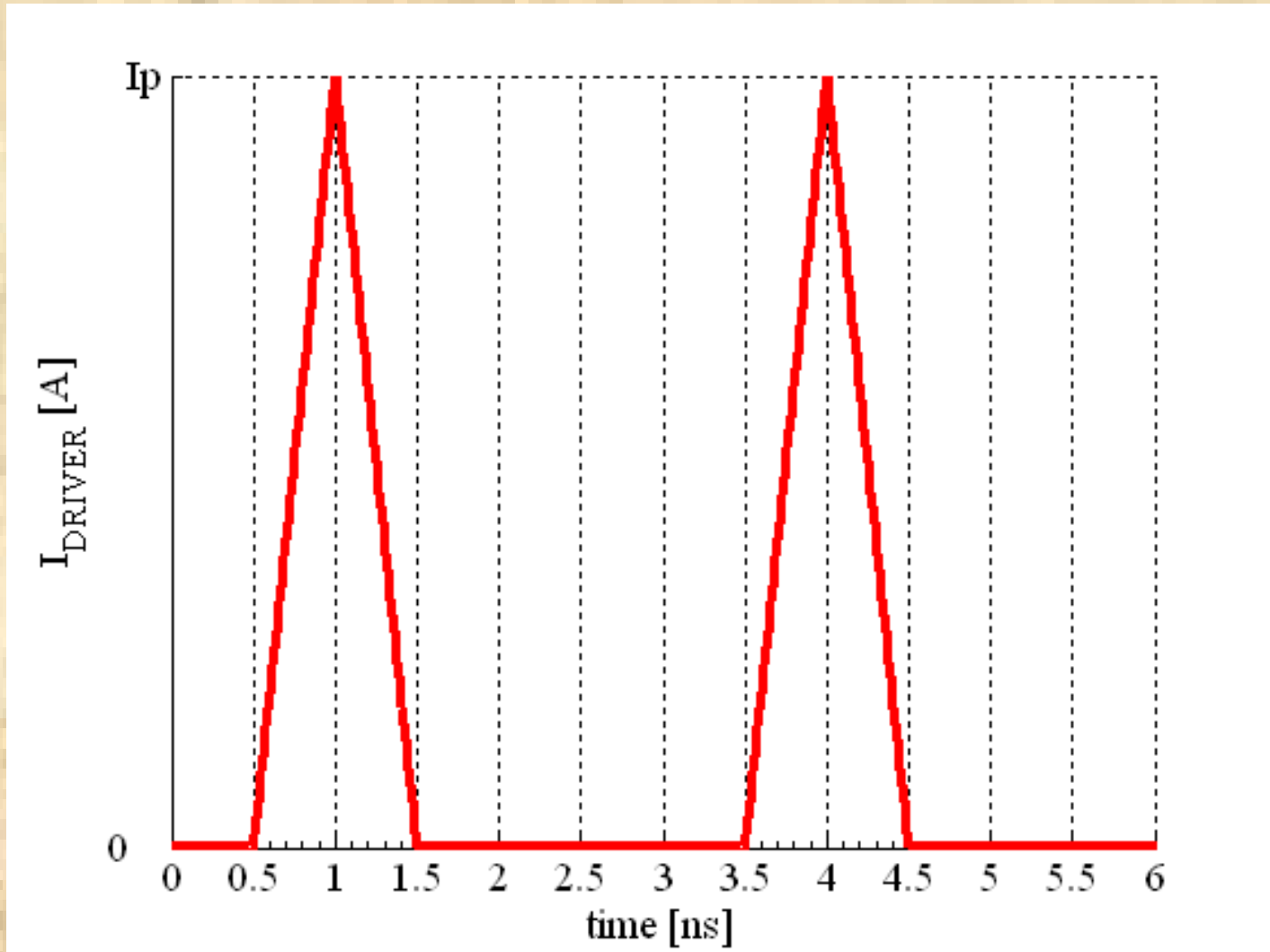
Port 2 represents IC current draw

Charge Between Planes vs.. Charge Drawn by IC

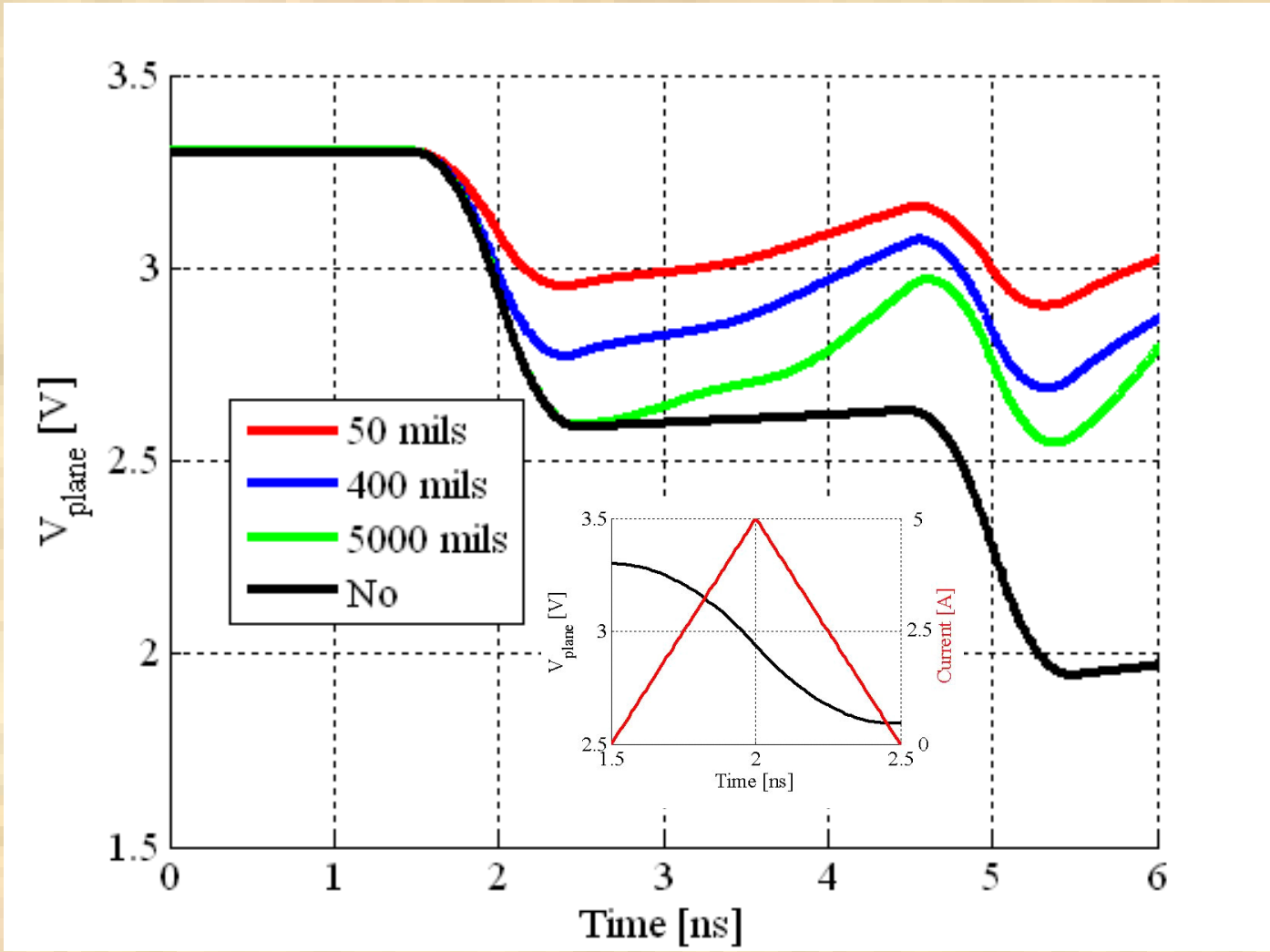
Board total charge : C*V = 3.5nF*3.3V = 11nC

Pulse charge 5A peak : I*dt/2 = (1ns*5A)/2=2.5nC

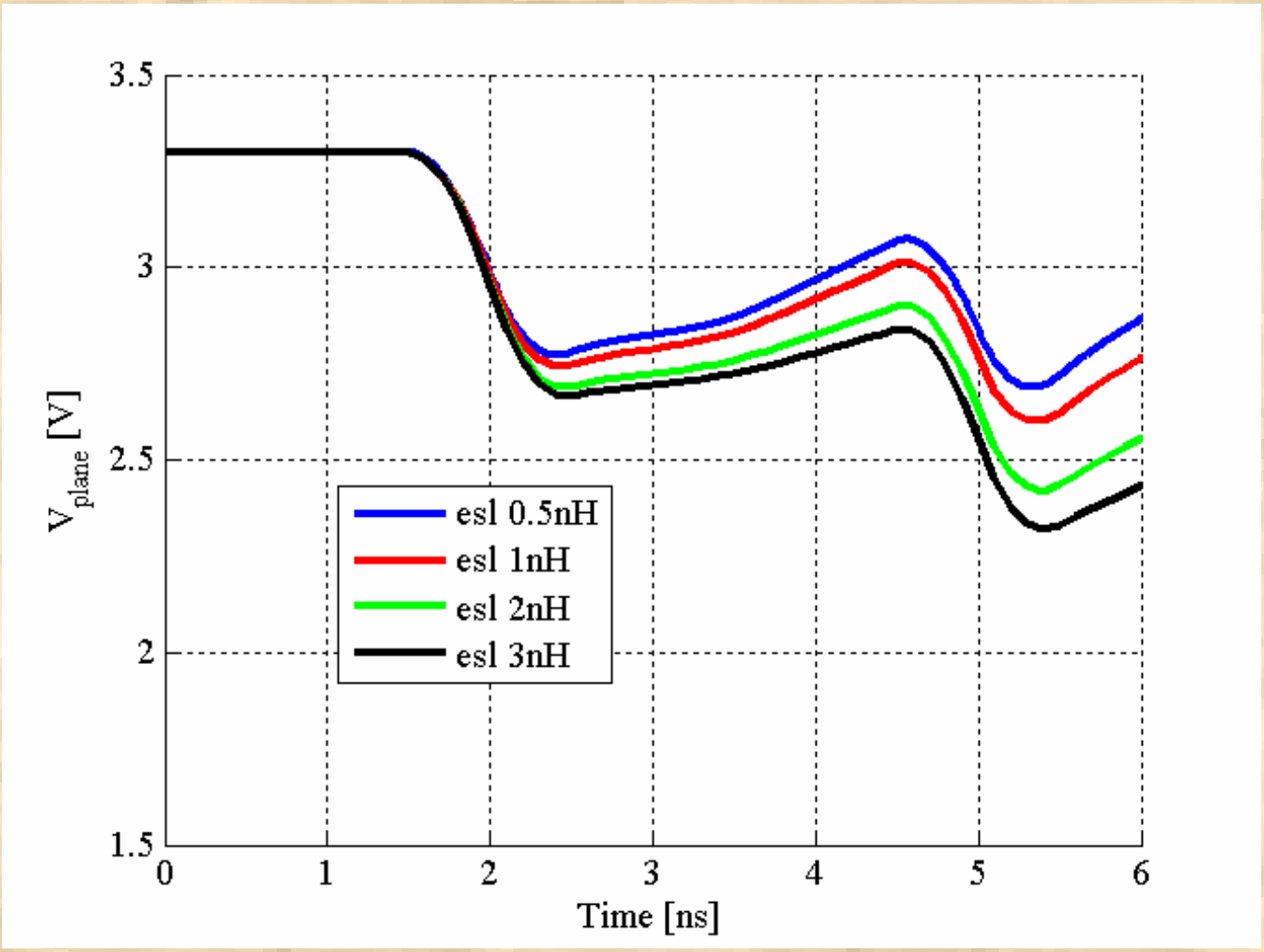
Triangular pulses (5 Amps Peak)



Charge Depletion vs. Capacitor Distance



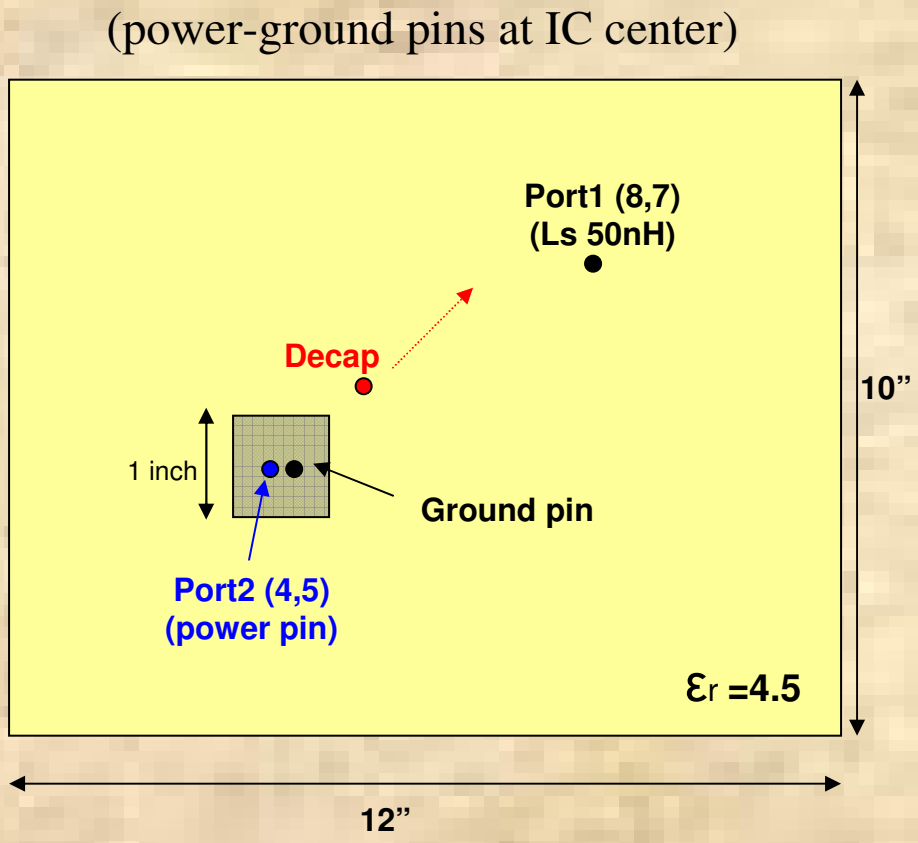
Charge Depletion for Capacitor @ 400 mils for Various connection Inductance



Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils from the power pin

- C=1uF
- ESL=0.5nH
- ESR=1Ω



Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils from the power pin

- C=0.5uF
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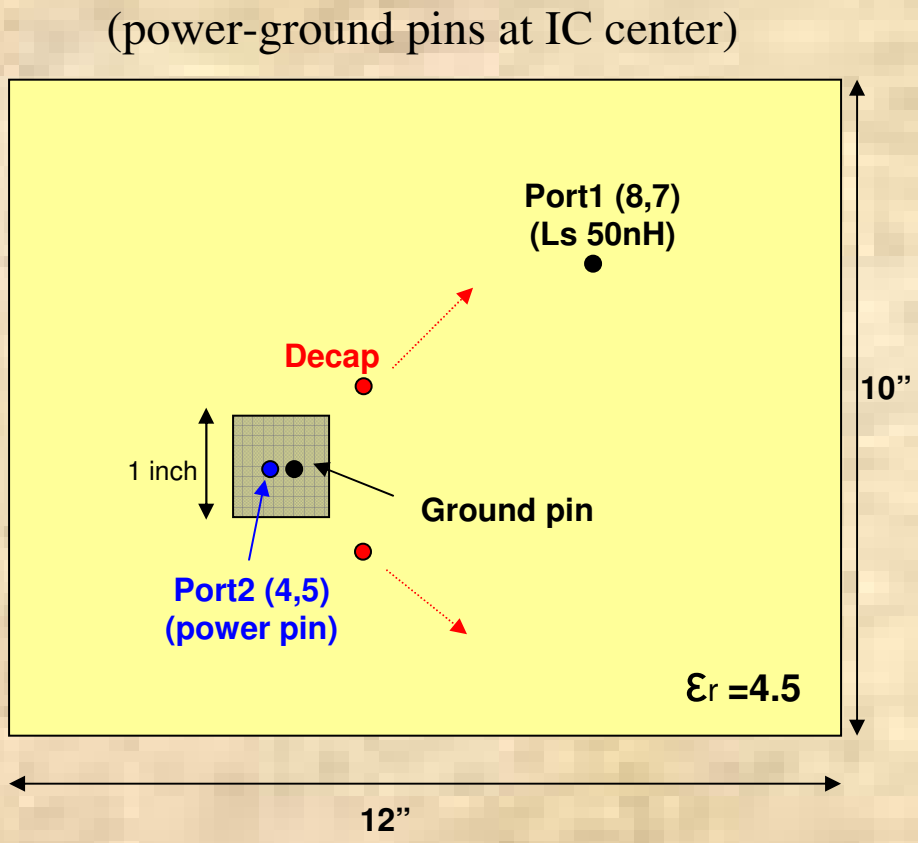
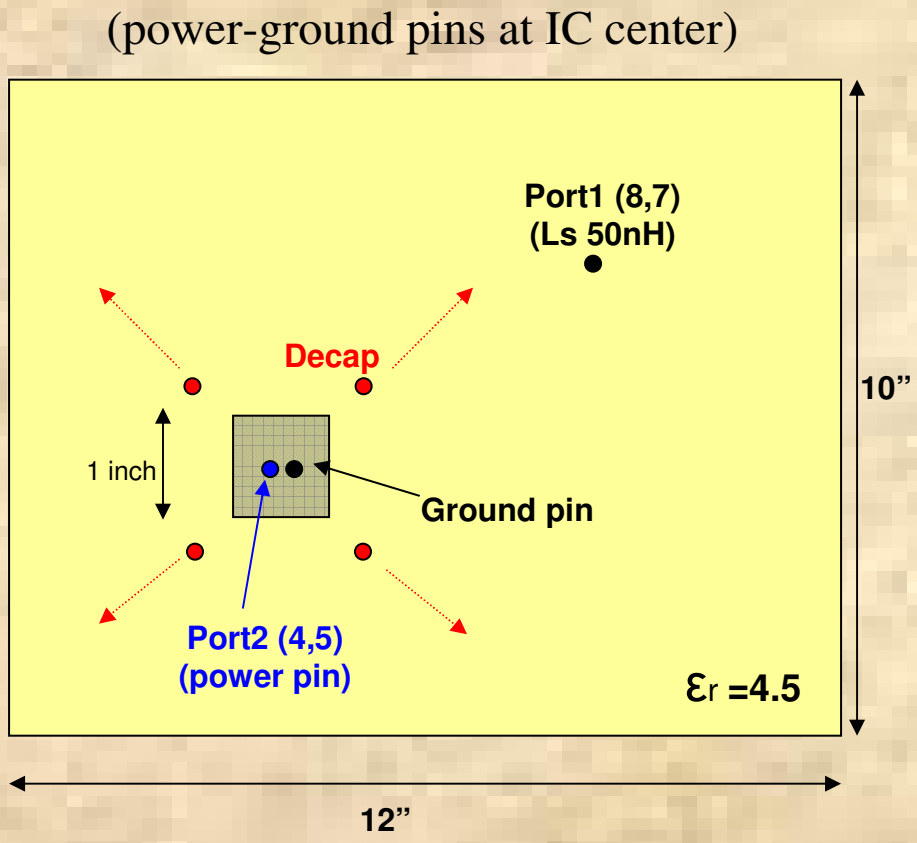
- ESR=1Ω



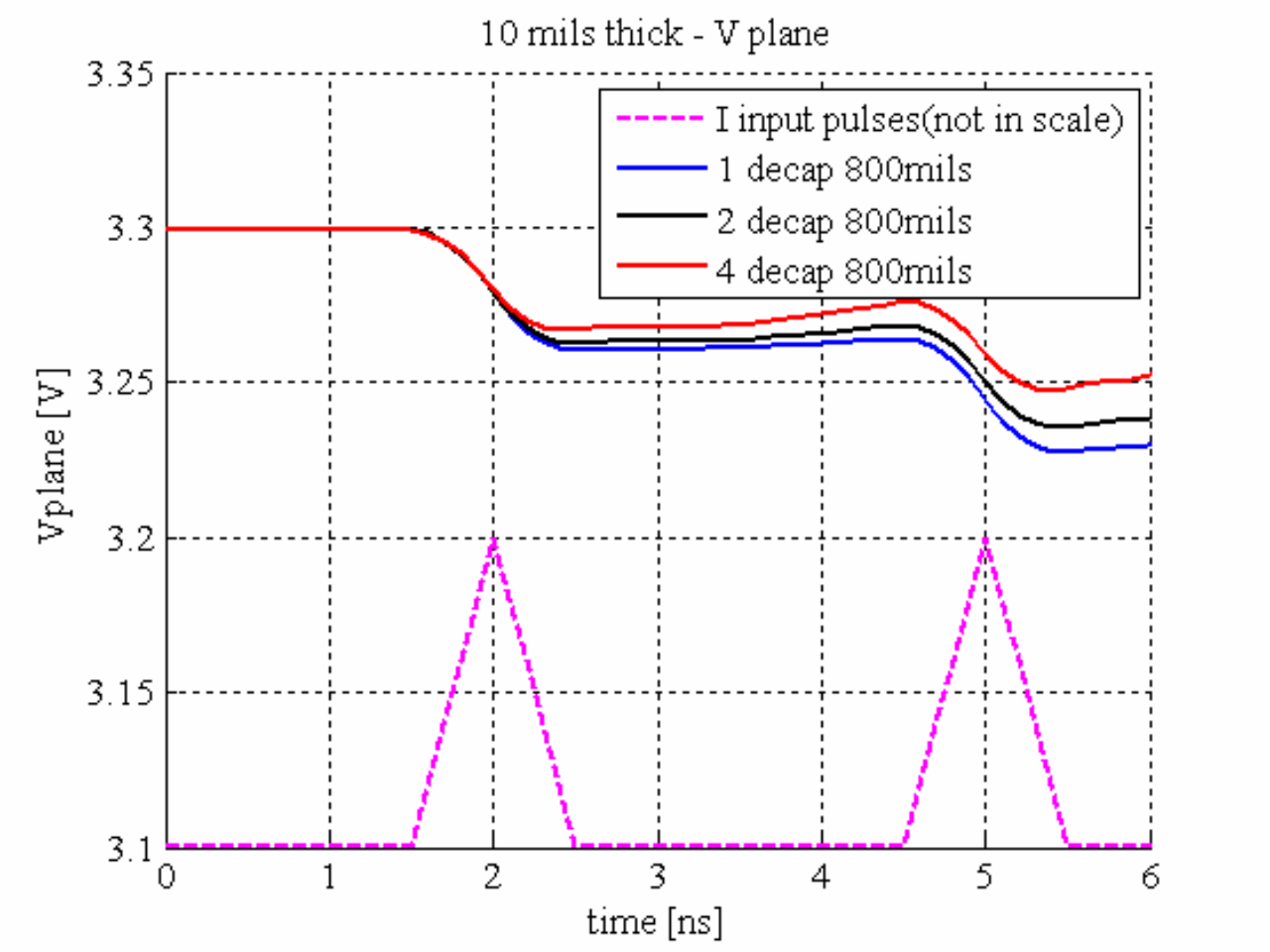
Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils from the power pin

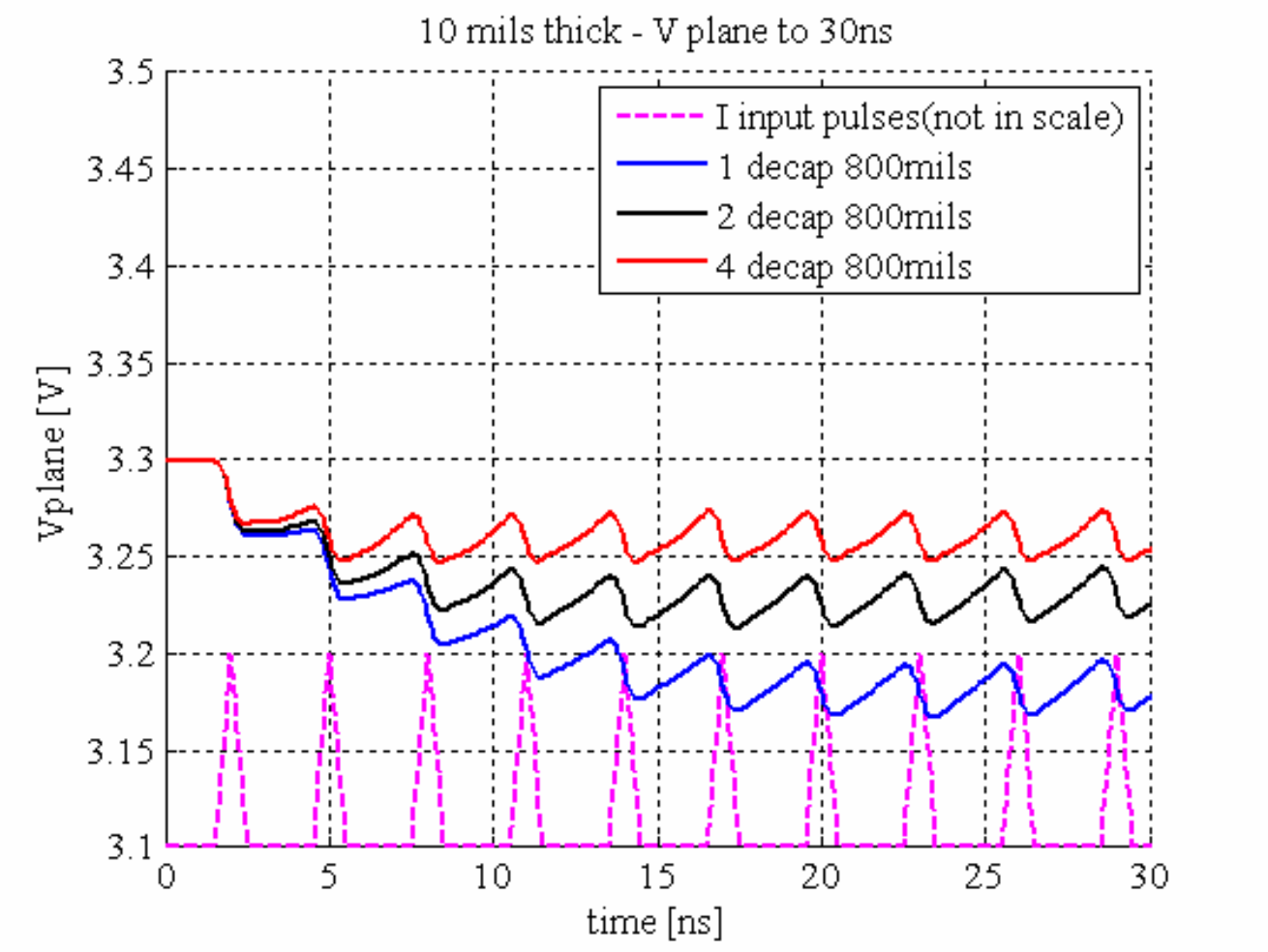
- C=0.25uF
- ESL=0.5nH
- ESR=1Ω



Constant Capacitance 800 mil Distance



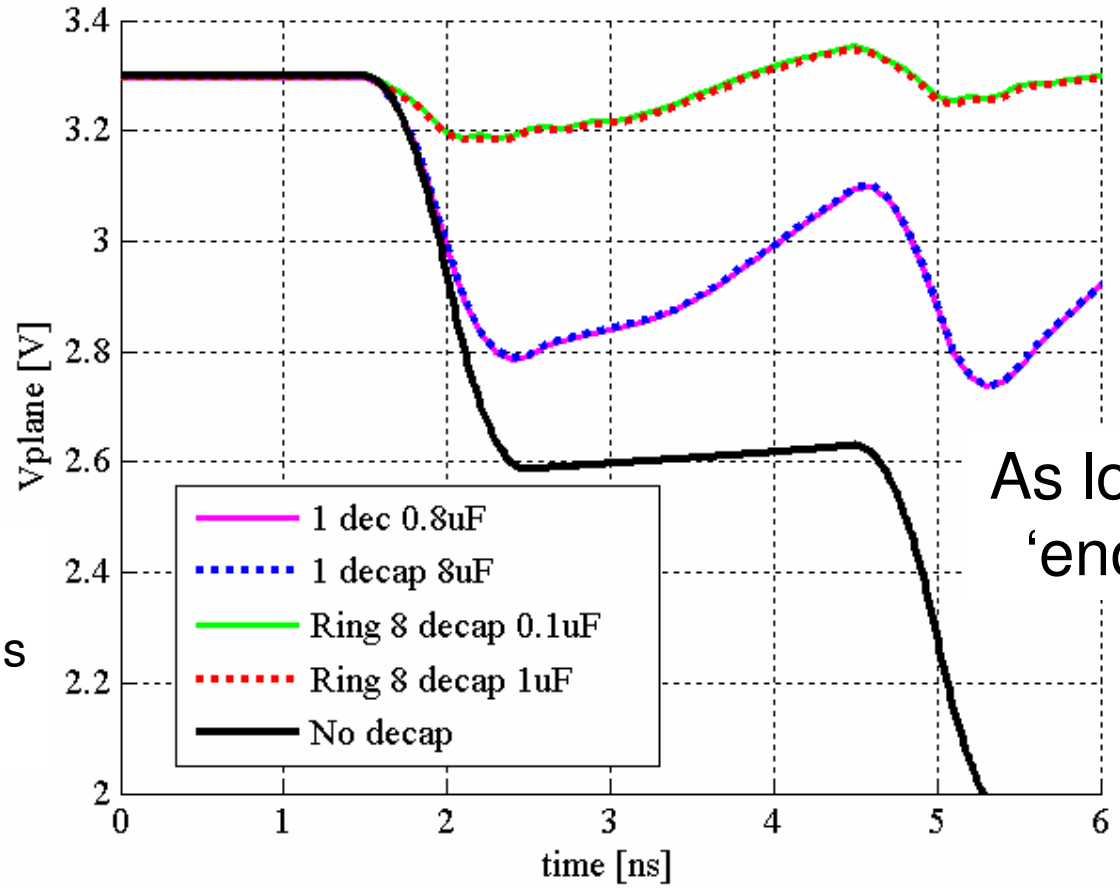
Constant Capacitance 800 mil Distance



Effect of Capacitor Value??

- Need enough charge to supply need
- Depends on connection inductance

Noise Voltage is INDEPENDENT of Amount of Capacitance!



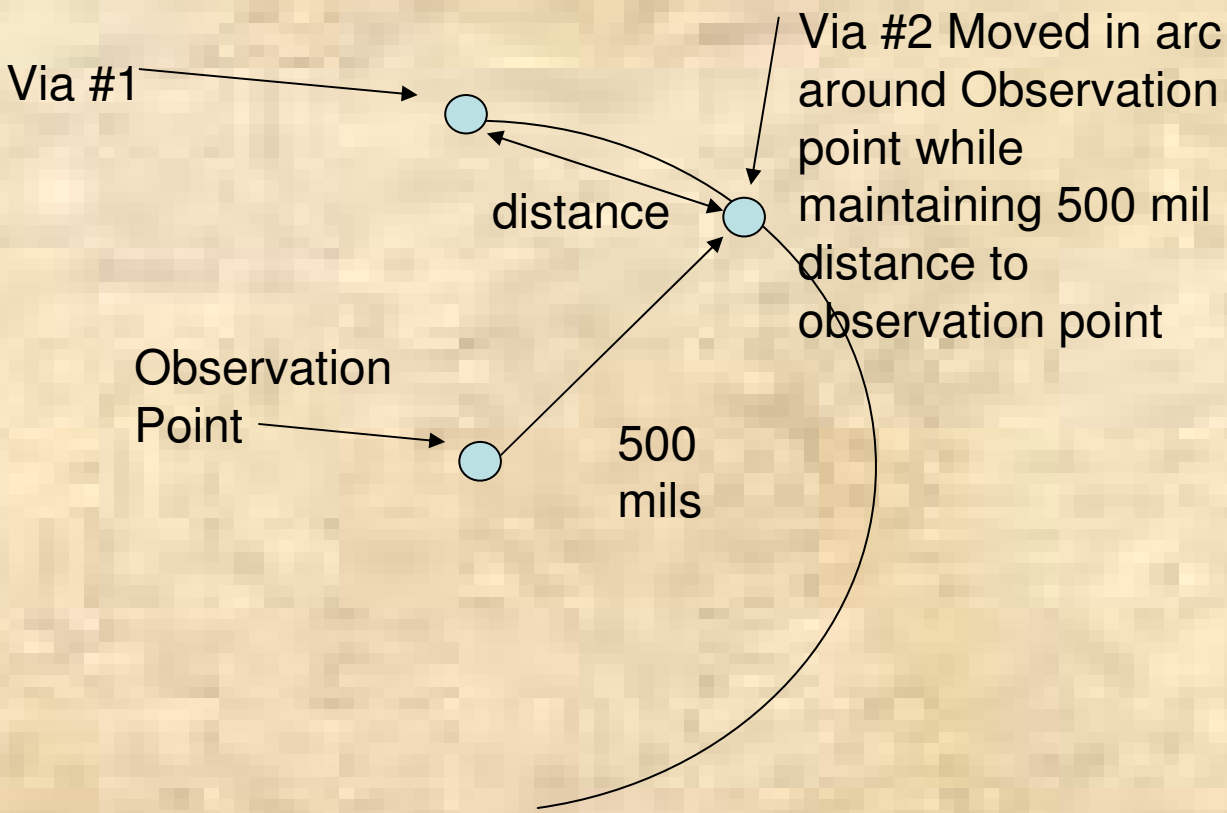
Dist=400 mils

ESR=30mOhms

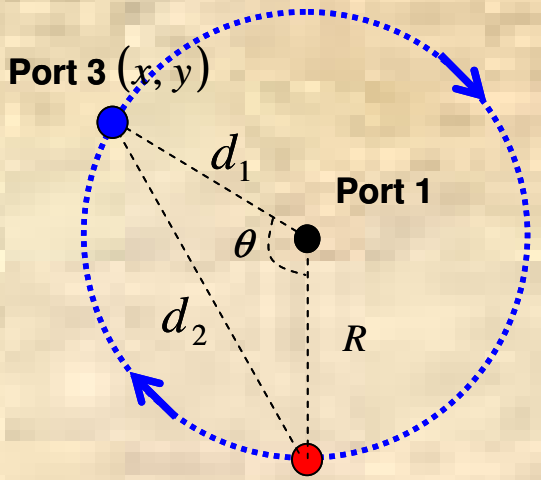
ESL=0.5nH

As long as there is 'enough' charge

What Happens if a 2nd Decoupling Capacitor is placed near the First Capacitor?



Second Via Around a circle



$d_1 = R$

$d_2 = 2R\sin\frac{\theta}{2}$

R: distance between Port 1 and Port 2 in mil

r: radius for all ports in mil

d: thickness of dielectric layer in mil

d1: distance between Port 3 and Port 1 in mil

d2: distance between Port 2 and Port 3 in mil

theta: angle as shown in the figure in degree

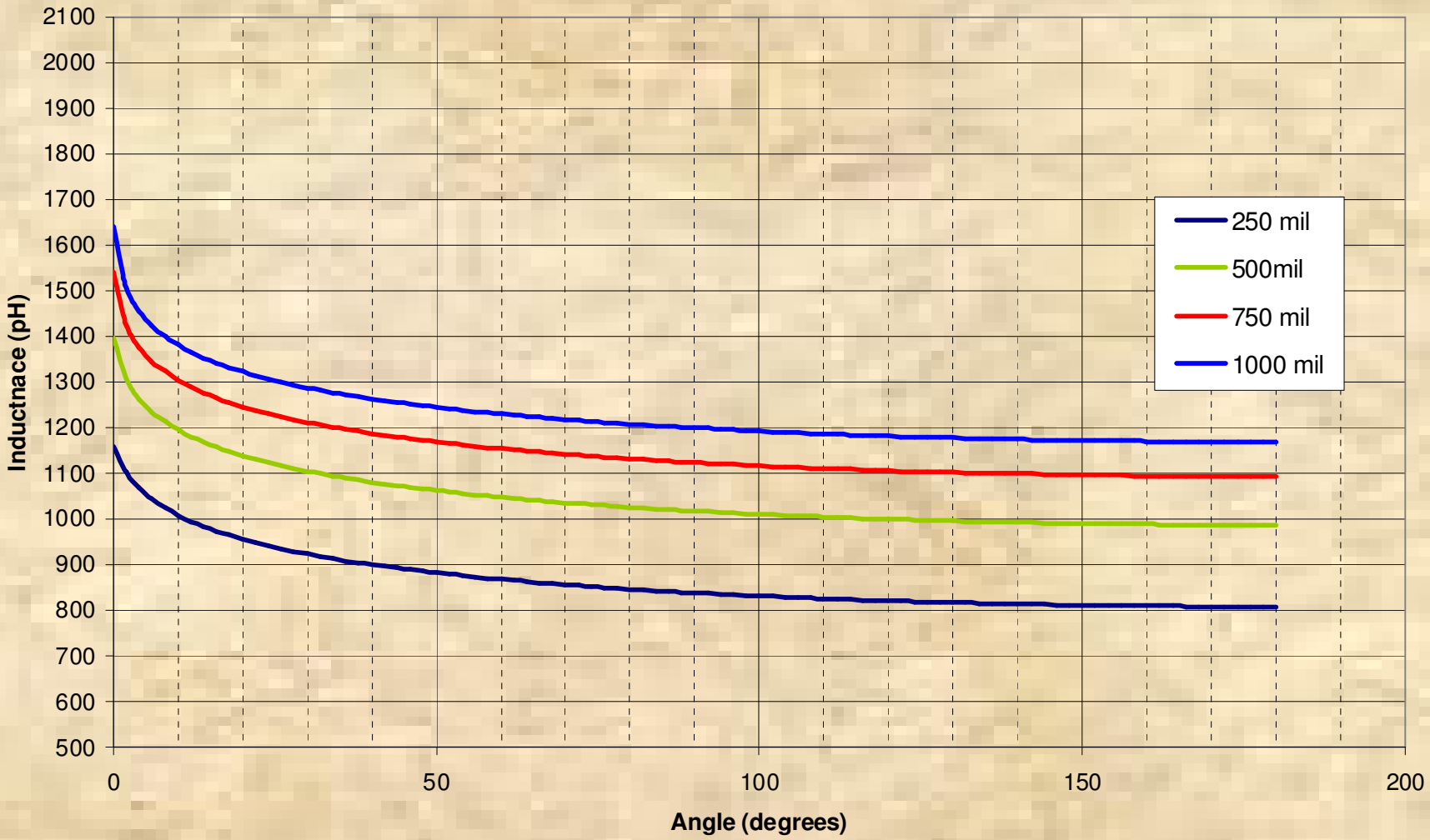
$$\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^2(d_1+r)^2}{r^3(d_2+r)}\right)-\frac{\mu d}{4\pi}\frac{\ln^2\left(\frac{d_1+r}{R+r}\right)}{\ln\left(\frac{d_2+r}{r}\right)}$$

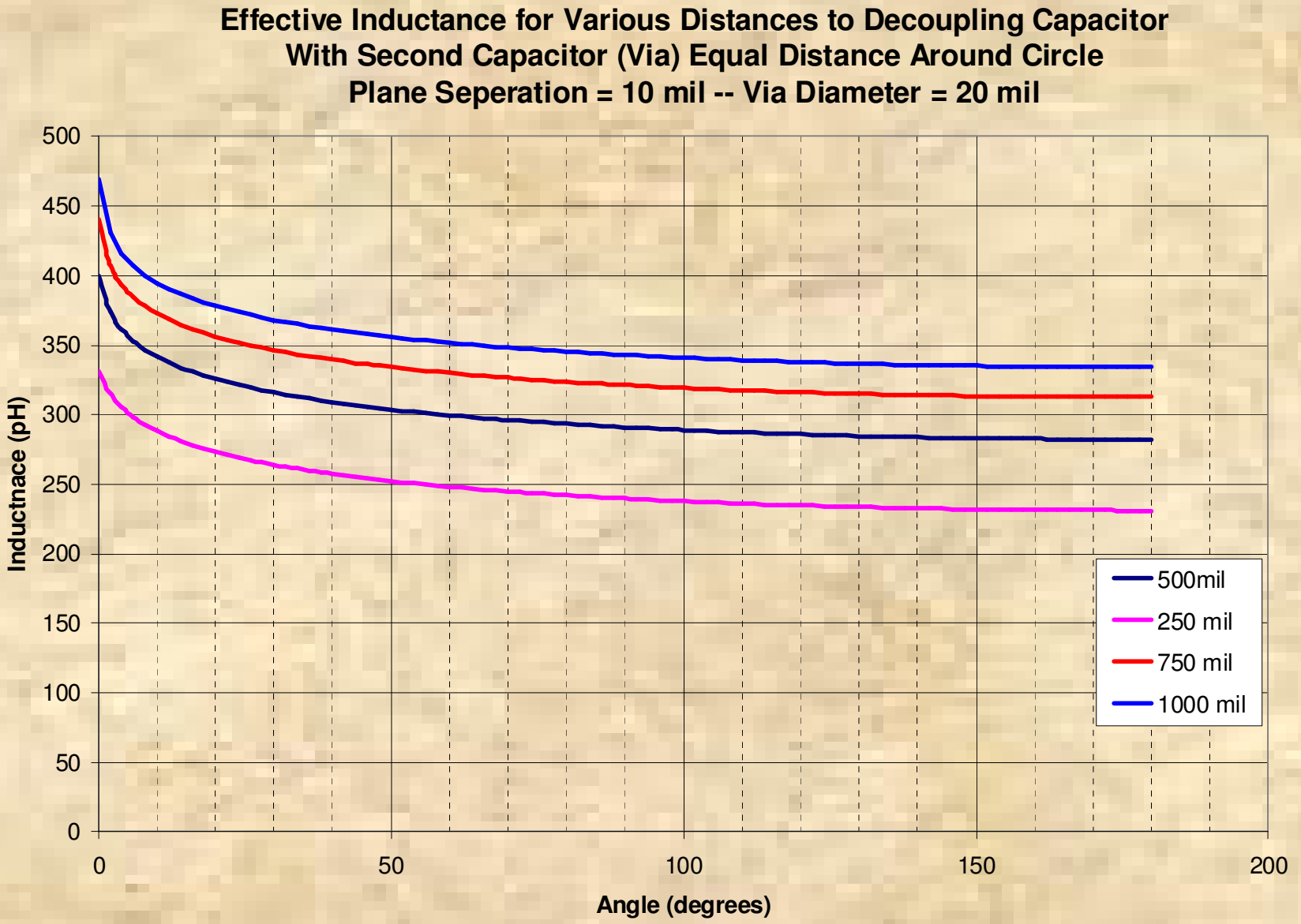
$$=\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^4}{(2R\sin(\theta/2)+r)r^3}\right)$$

Courtesy of Jingook Kim, Jun Fan, Jim Drewniak

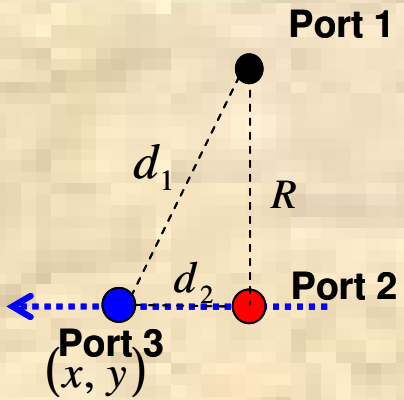
Missouri University of Science and Technology

Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 35 mil -- Via Diameter = 20 mil




Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 10 mil -- Via Diameter = 20 mil
Inductnace (pH)
500
450
400
350
300
250
200
150
100
50
0
0
50
100
150
200
Angle (degrees)
500mil
250 mil
750 mil
1000 mil

Second Via Along Side



$$d_1 = \sqrt{R^2 + {d_2}^2}$$

R: distance between Port 1 and Port 2 in mil

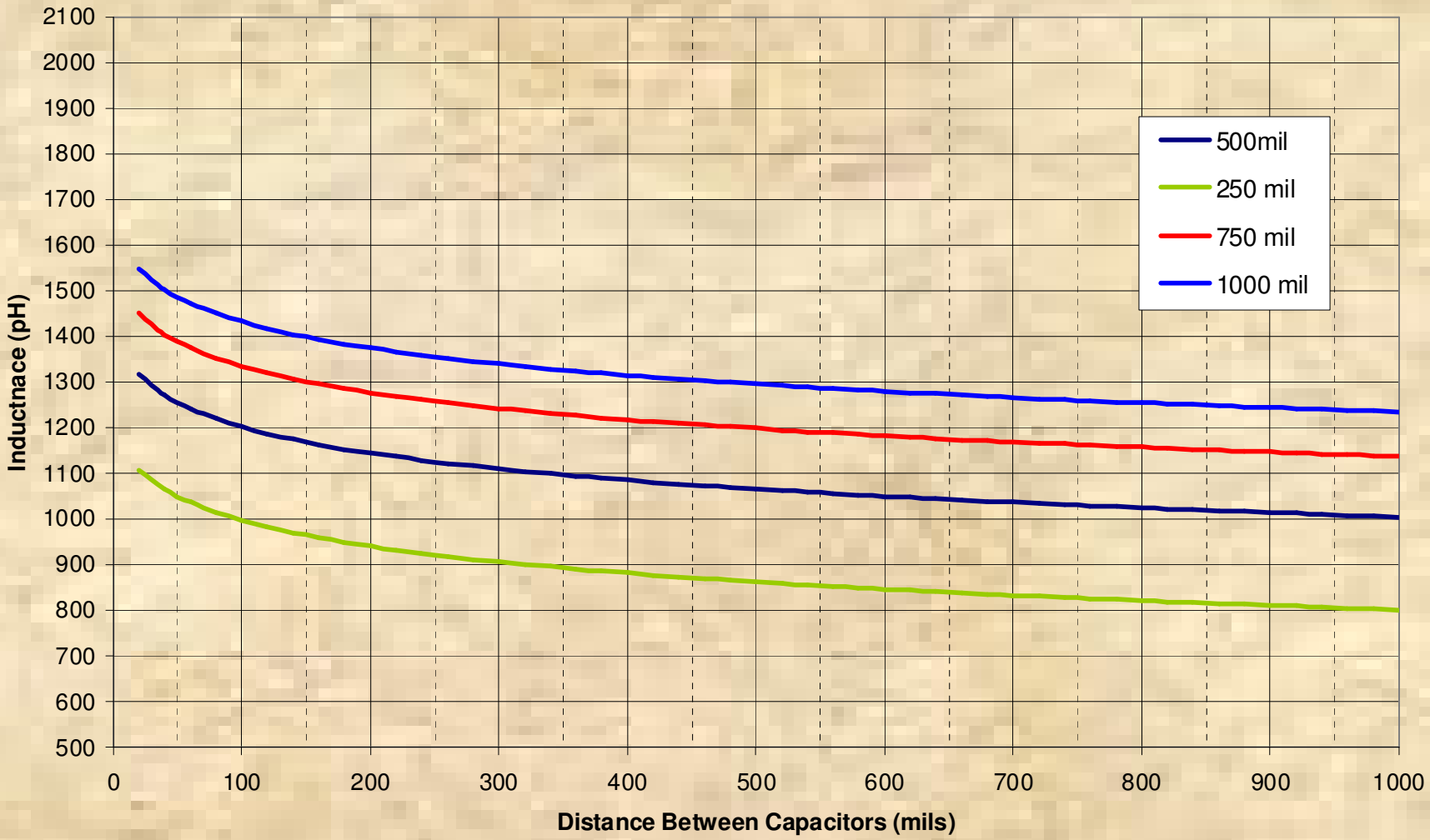
r: radius for all ports in mil

d: thickness of dielectric layer in mil

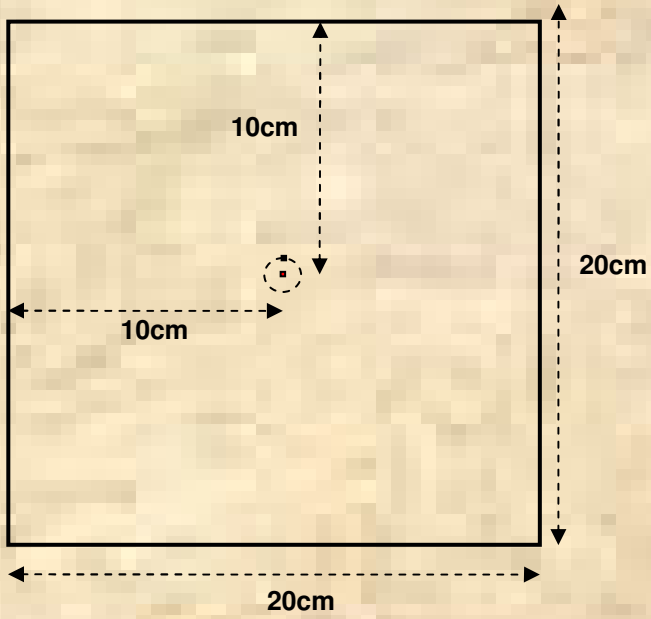
d1: distance between Port 3 and Port 1 in mil

d2: distance between Port 2 and Port 3 in mil

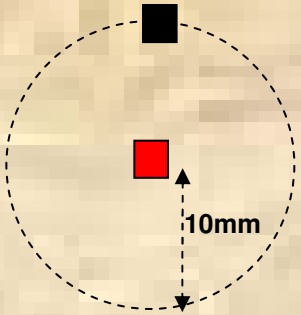
Effective Inductance for Various Distances to Decoupling Capacitor With Second Capacitor (Via) Positioned Adjacent to First Capacitor Plane Seperation = 35 mil -- Via Diameter = 20 mil



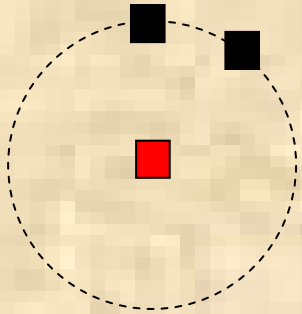
Understanding Inductance Effects and Proximity



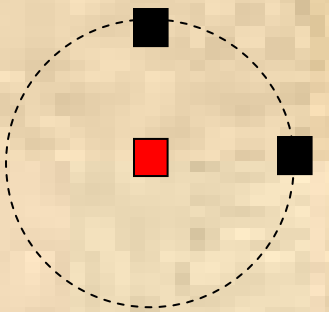
1 via



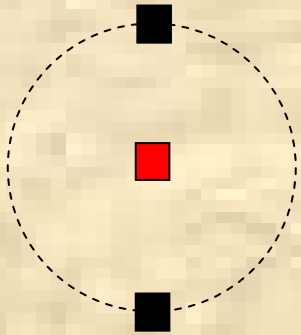
2 via with degree 30°



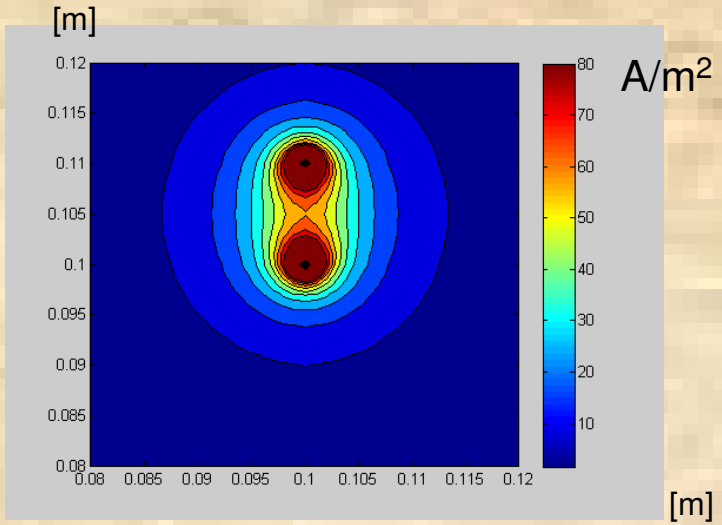
2 via with degree 90°

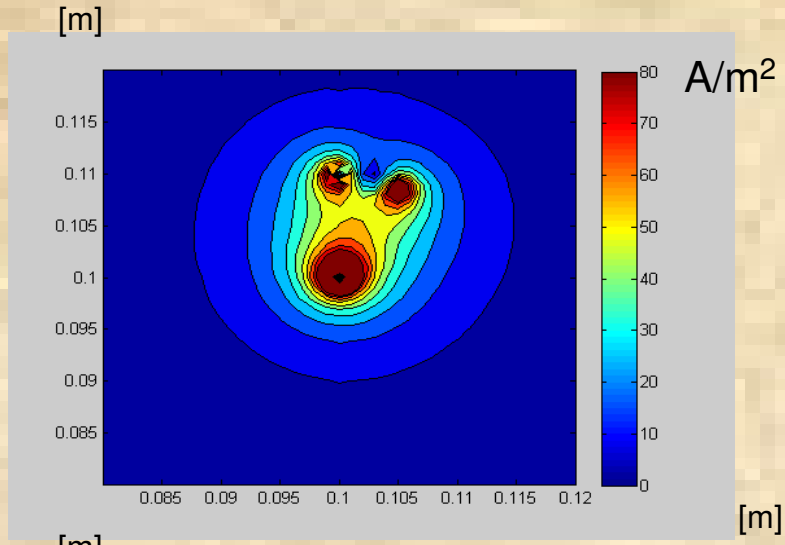


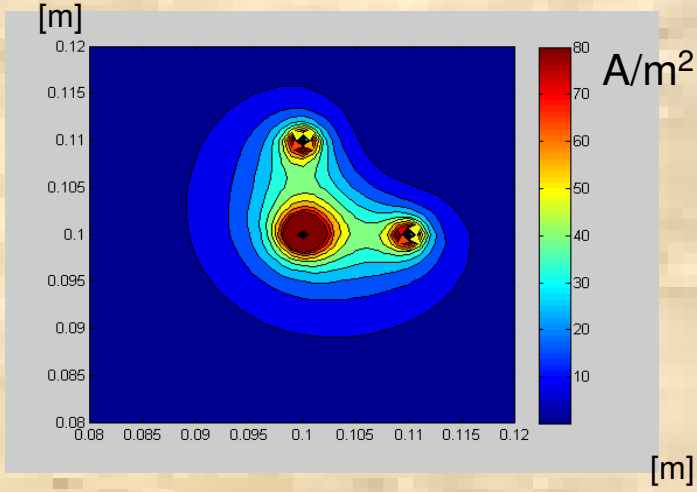
2 via with degree 180°

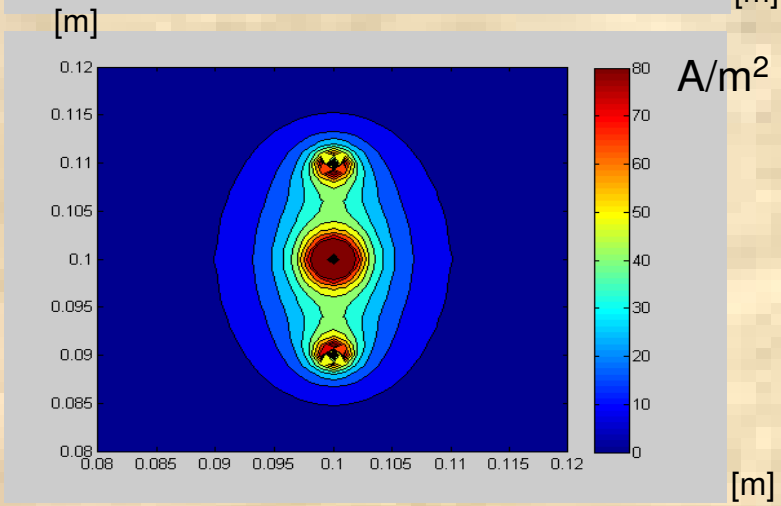


Current Density

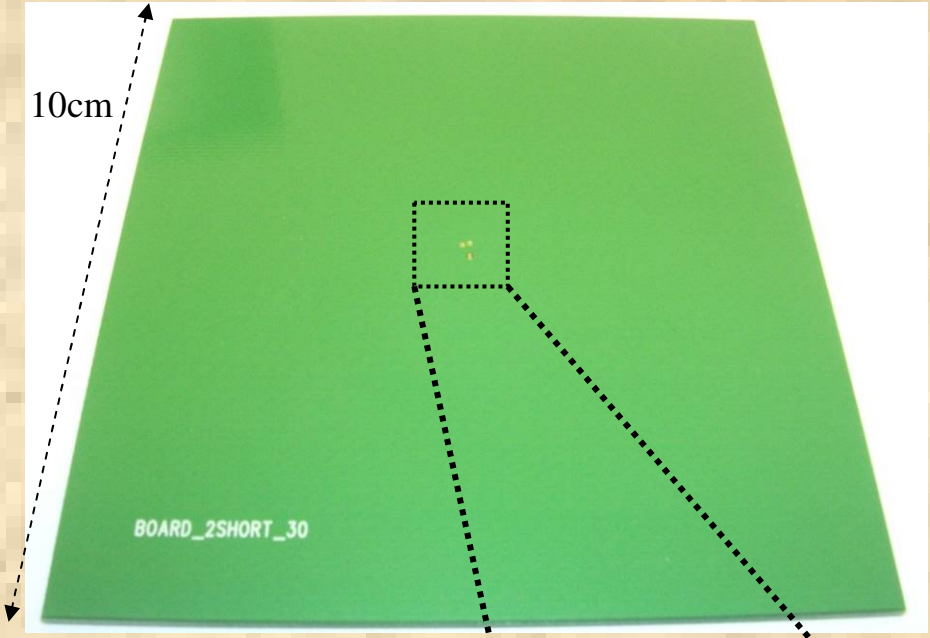


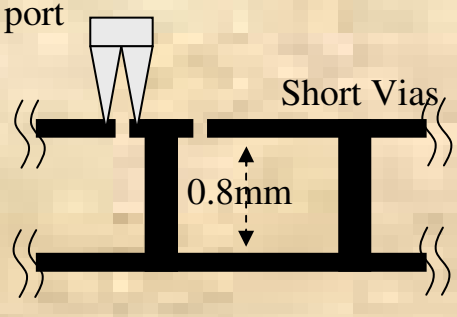


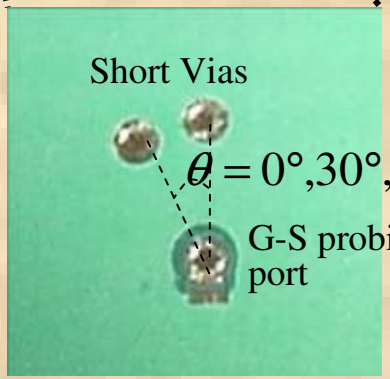


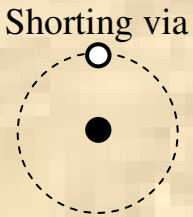


DUT for Experimental Validation (Single Plane pair)



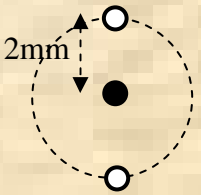






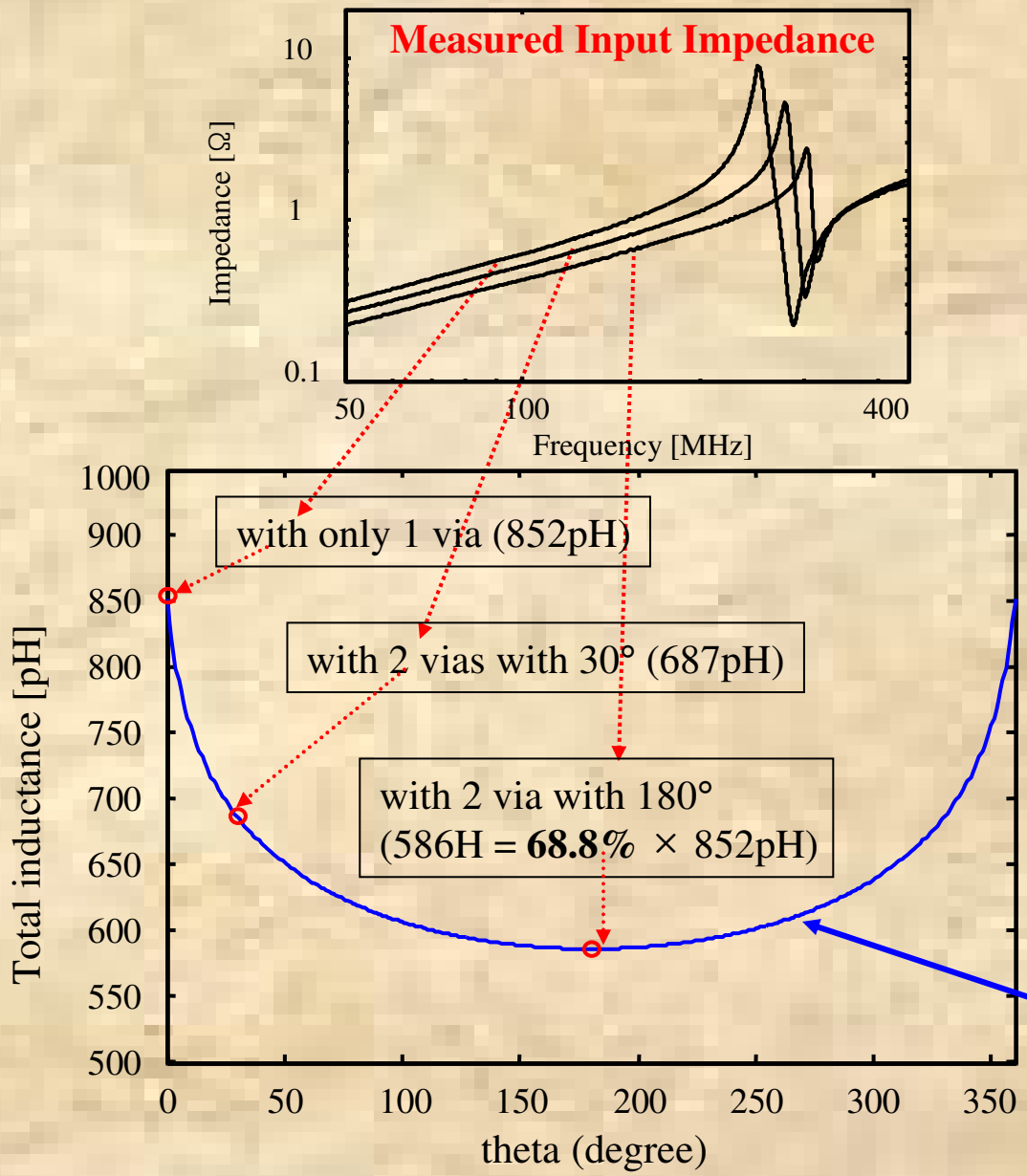
1 shorting

2 shorting with 30°



2 shorting with 180°

Experimental Validation (Single Plane Pair)

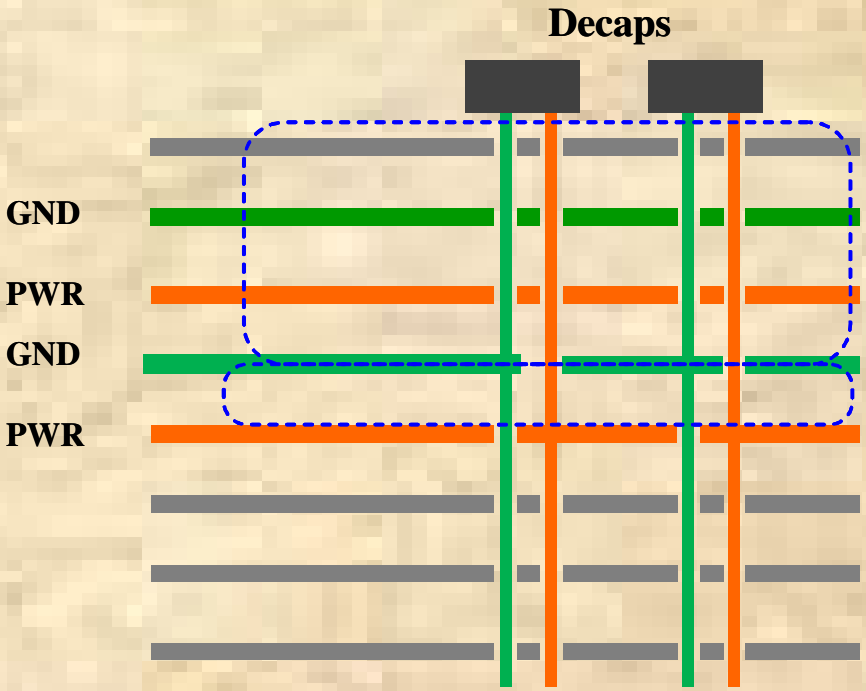


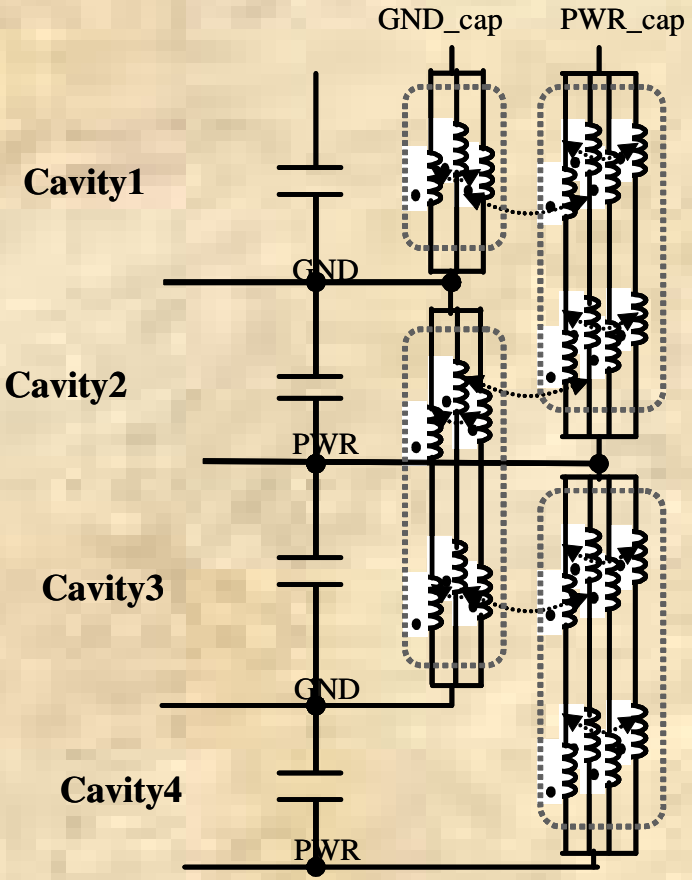
- Even in the case with two shorting vias at opposite sides (θ=180°), the inductance value is 68.8% of that with one shorting via
- As two shorting vias get closer together, mutual inductance between two shorting vias increases.

$$\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^4}{(2R\sin(\theta/2)+r)r^3}\right)$$

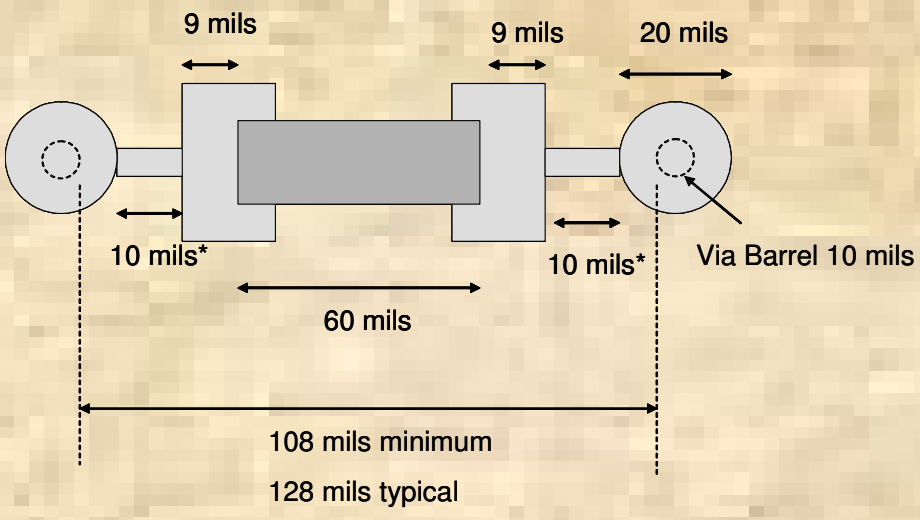
Equation

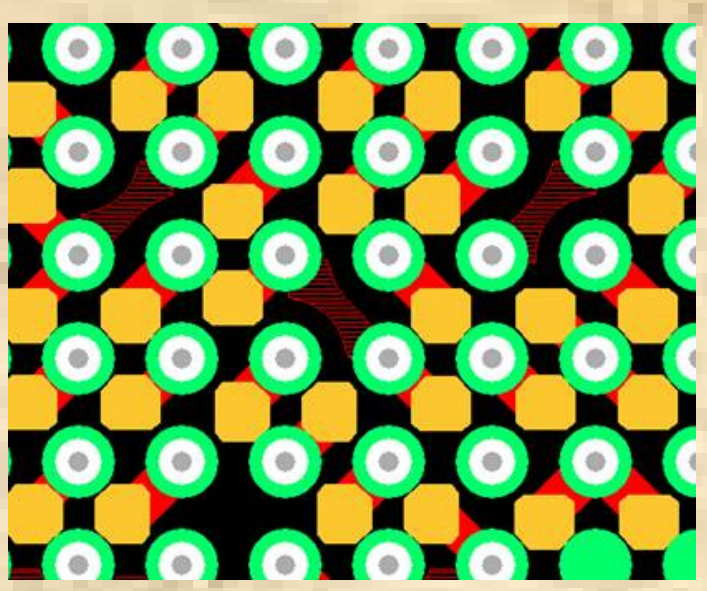
Multiple Capacitors





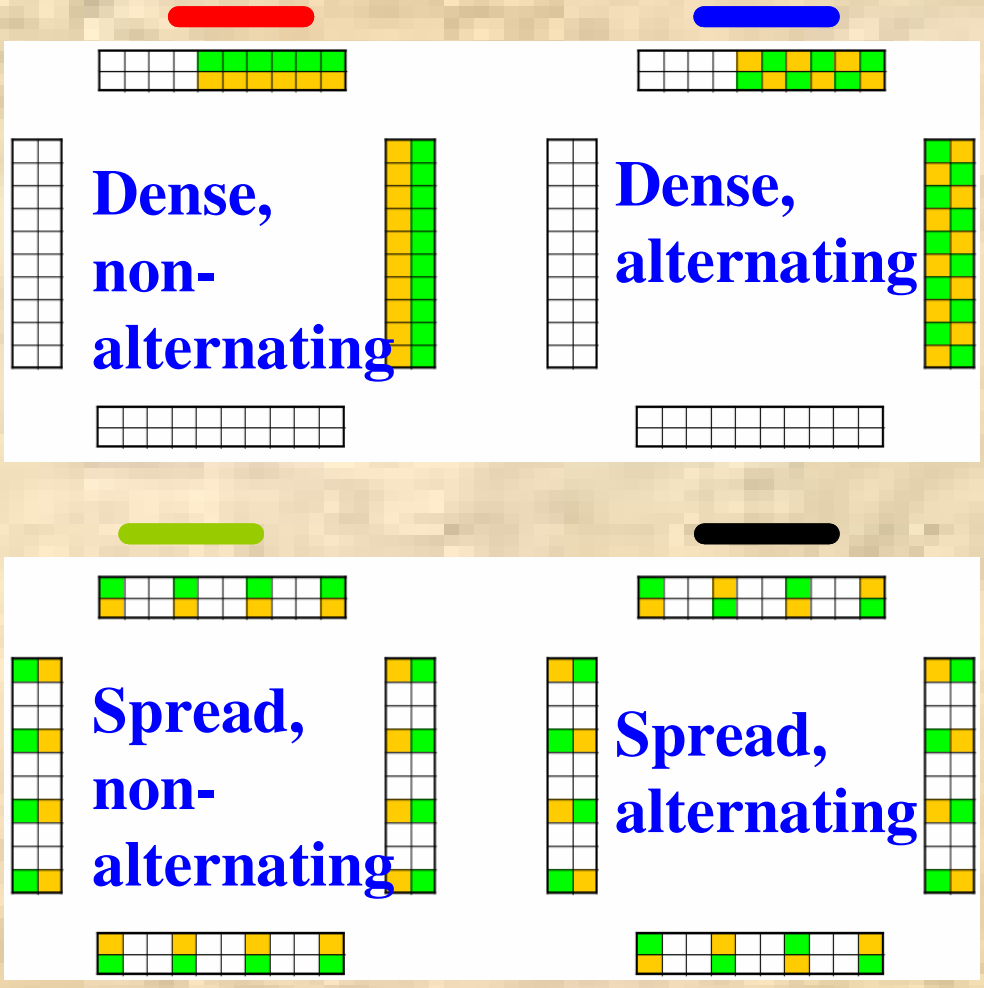
Via Spacing

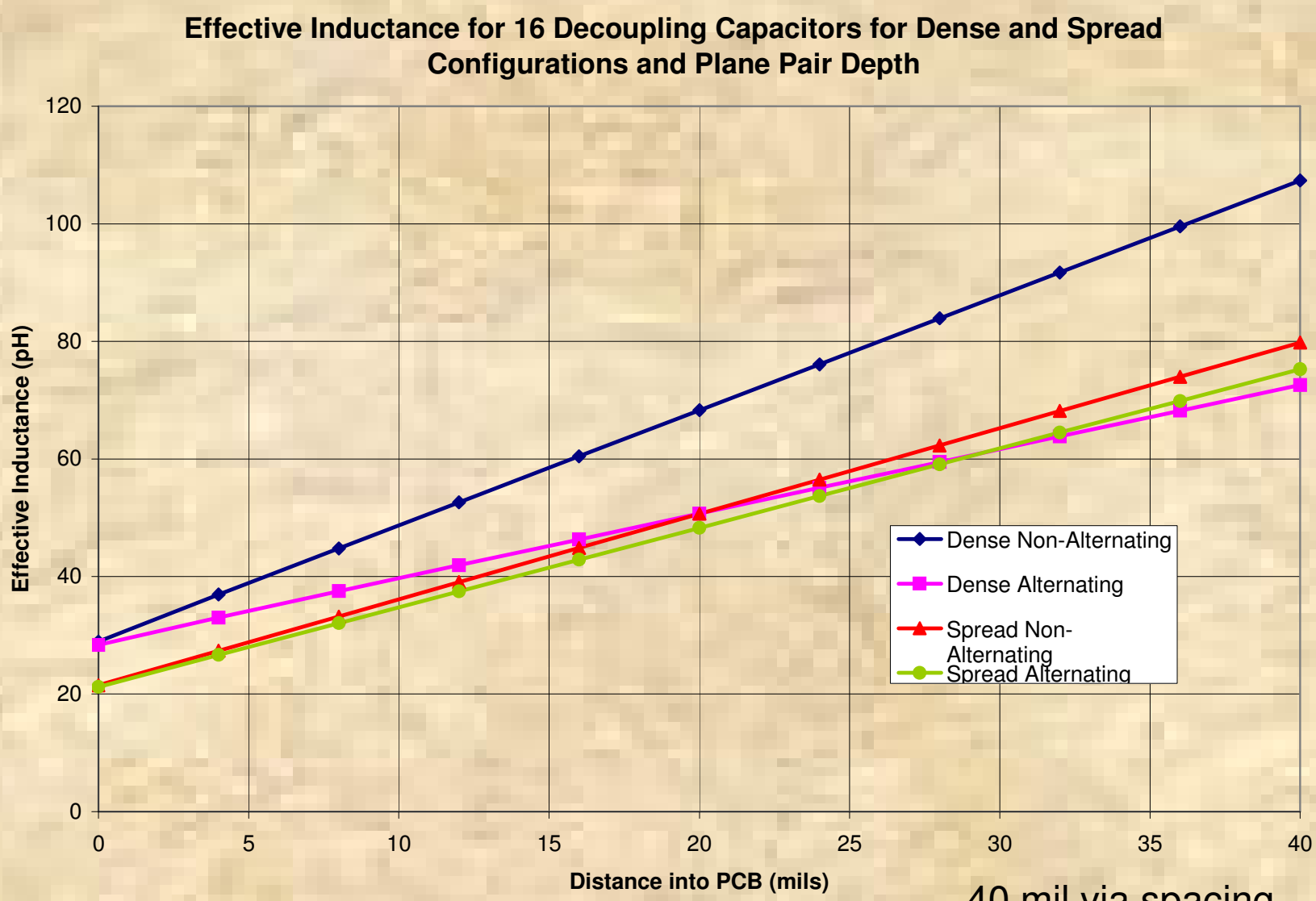




Distance to Planes (mils)	40 mil Spacing (nH)	0402 SMT (nH)	0603 SMT (nH)
10	0.3	0.9	1.1
20	0.5	1.3	1.6
30	0.75	1.6	1.9
40	0.95	1.9	2.2

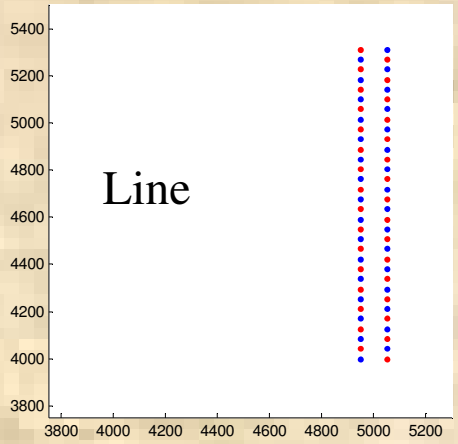
Possible Configurations

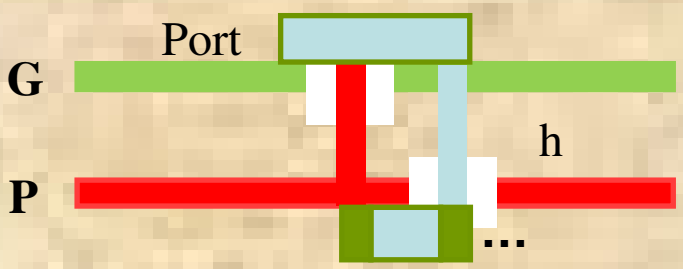




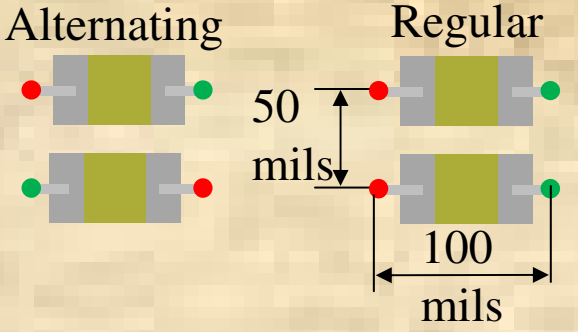
40 mil via spacing

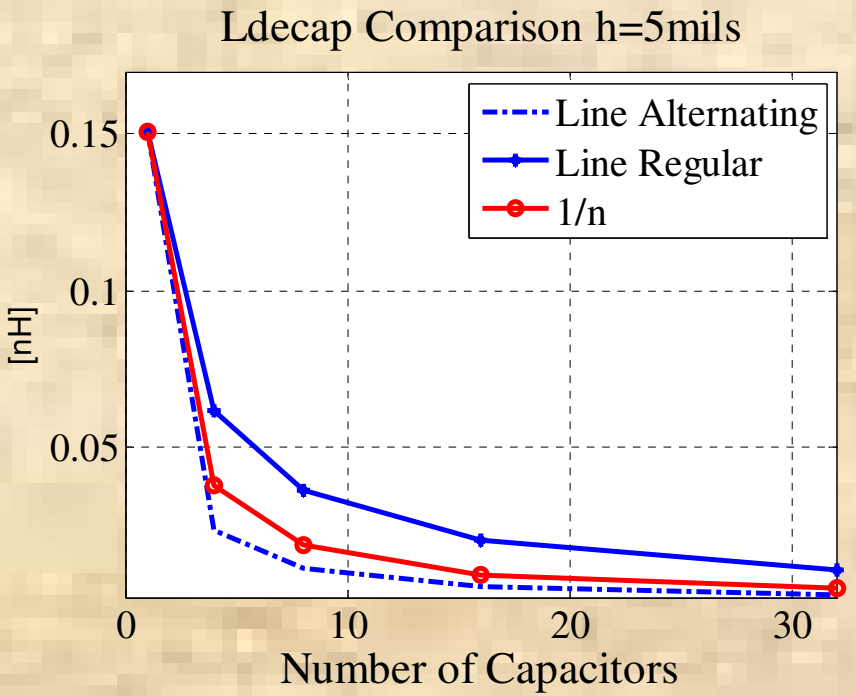
L_{Decap} Convergence

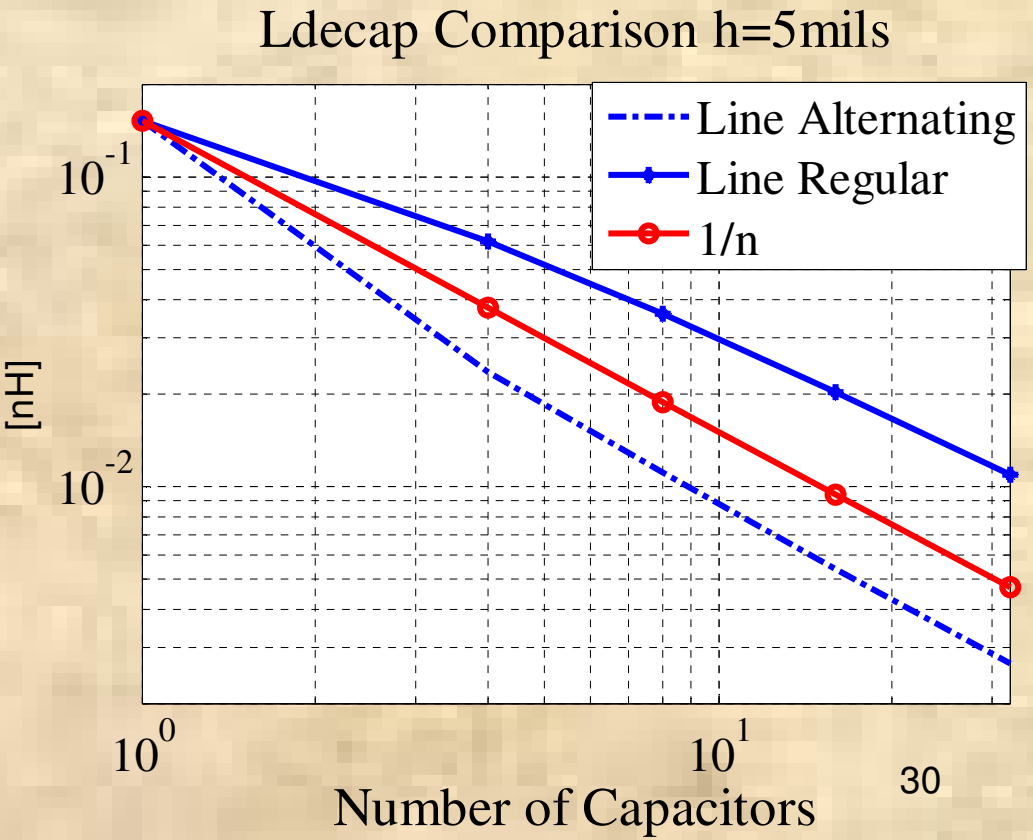




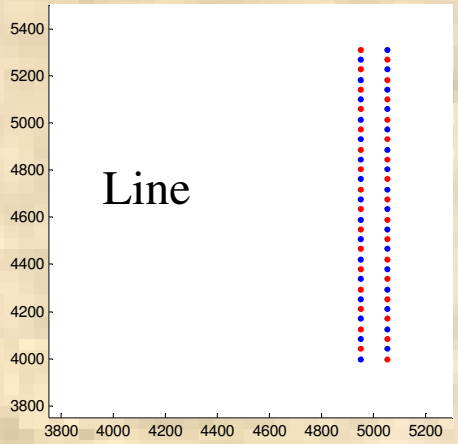
Decaps modeled as a Short

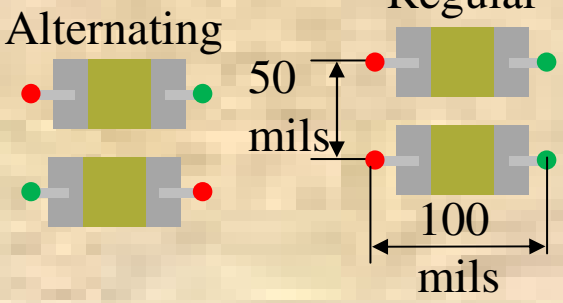


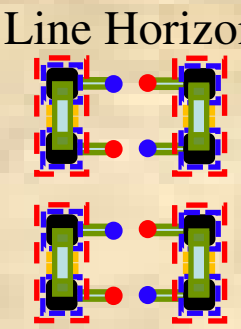


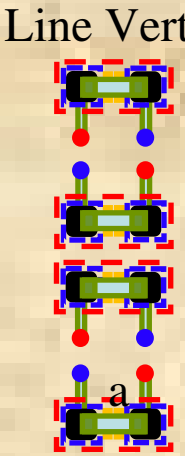


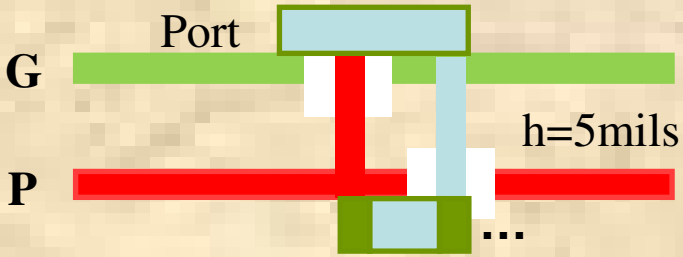
L_{Decap} Convergence 0402 Size



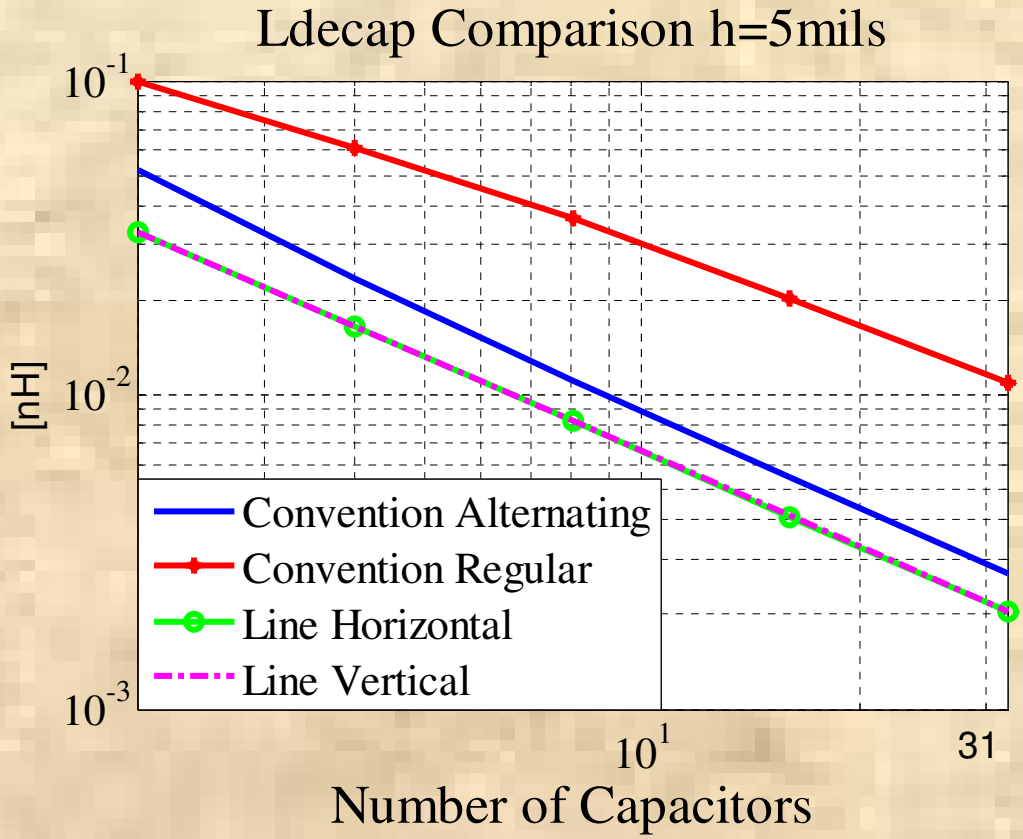




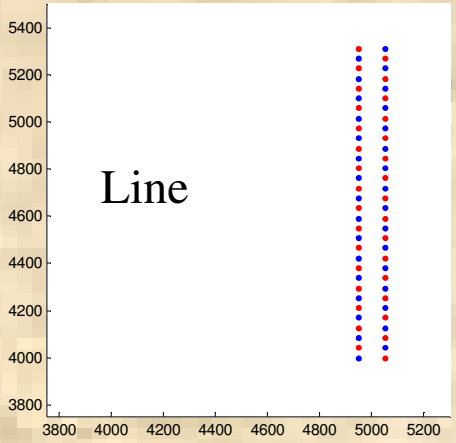


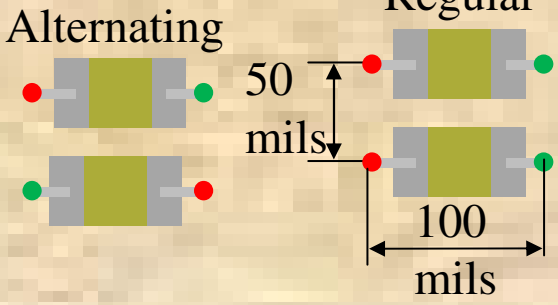


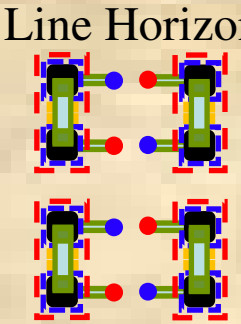
Decaps modeled as a Short

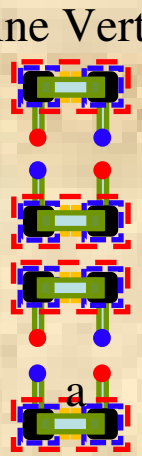


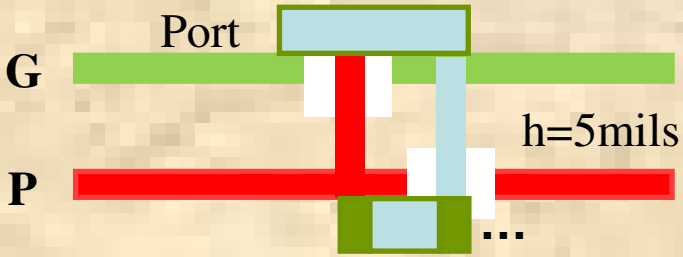
L_{Decap} Convergence 0402 Size



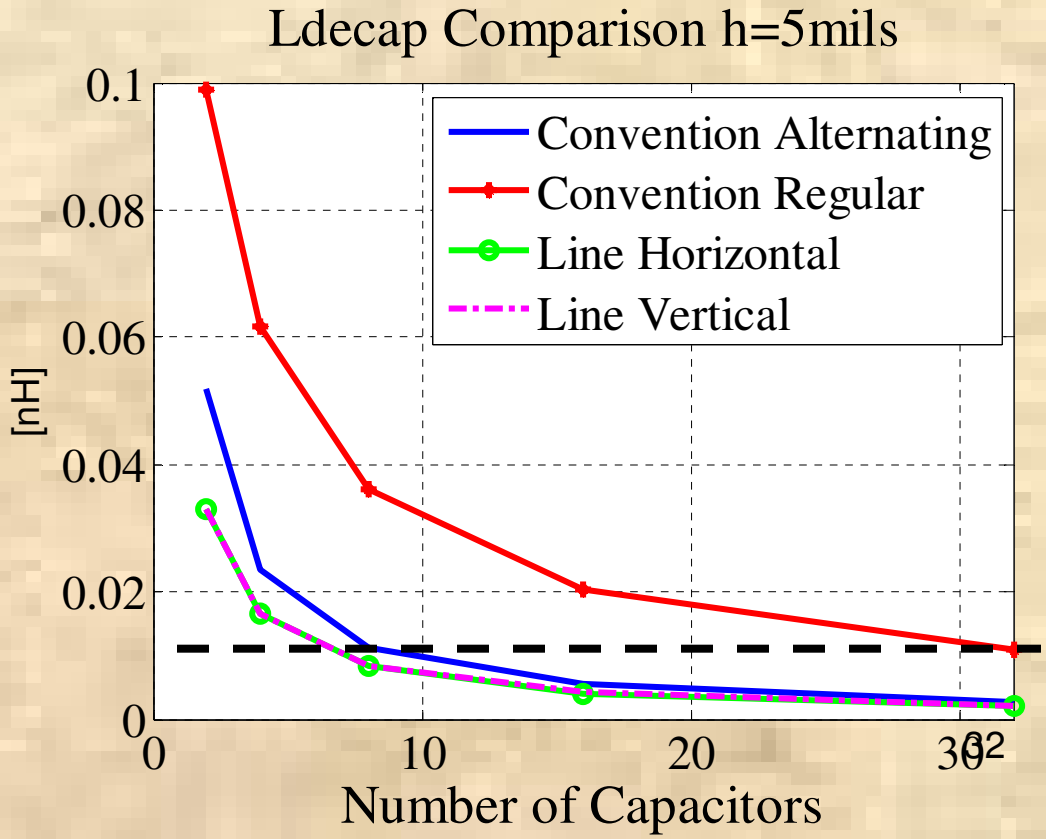








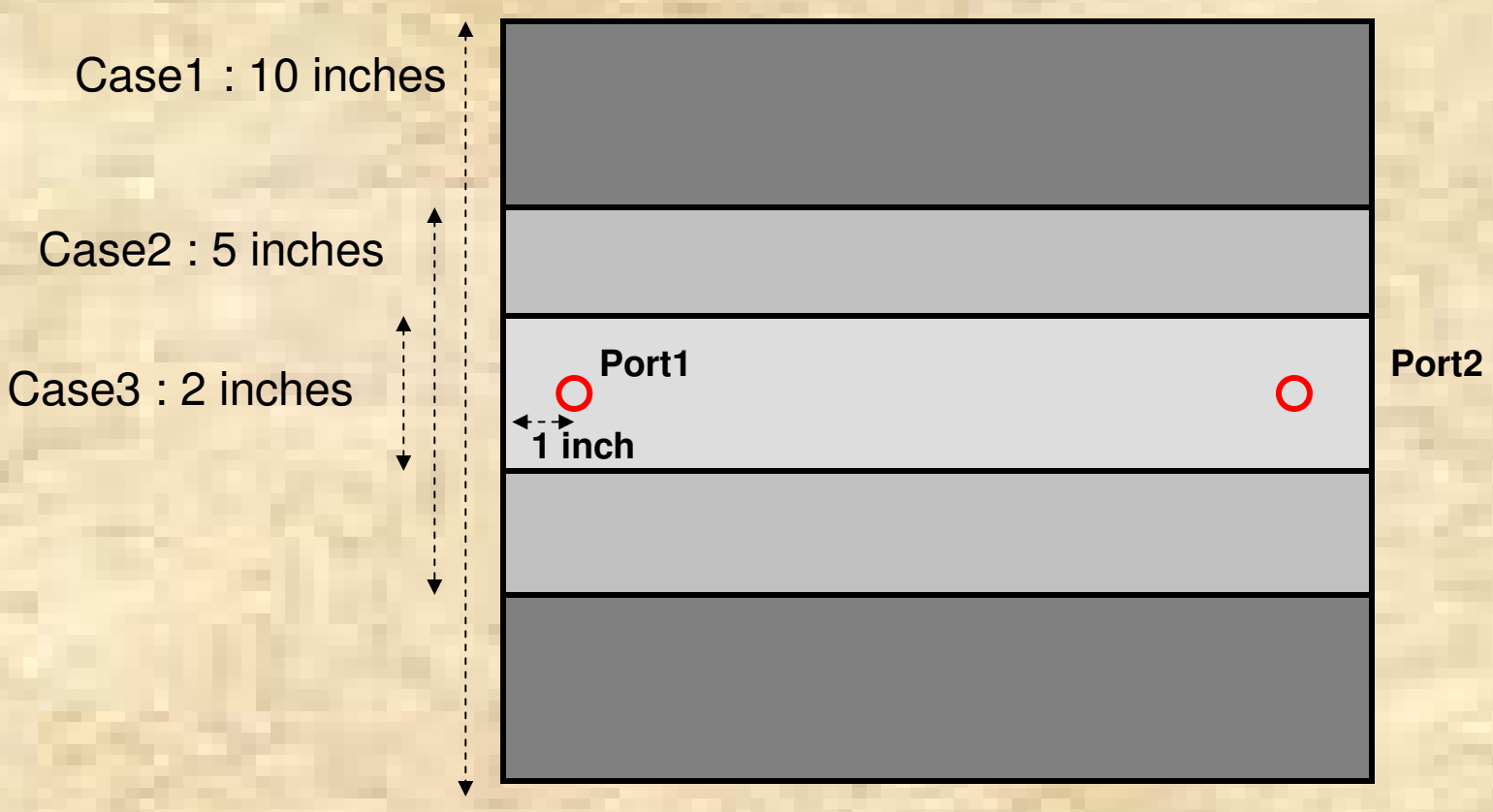
Decaps modeled as a Short



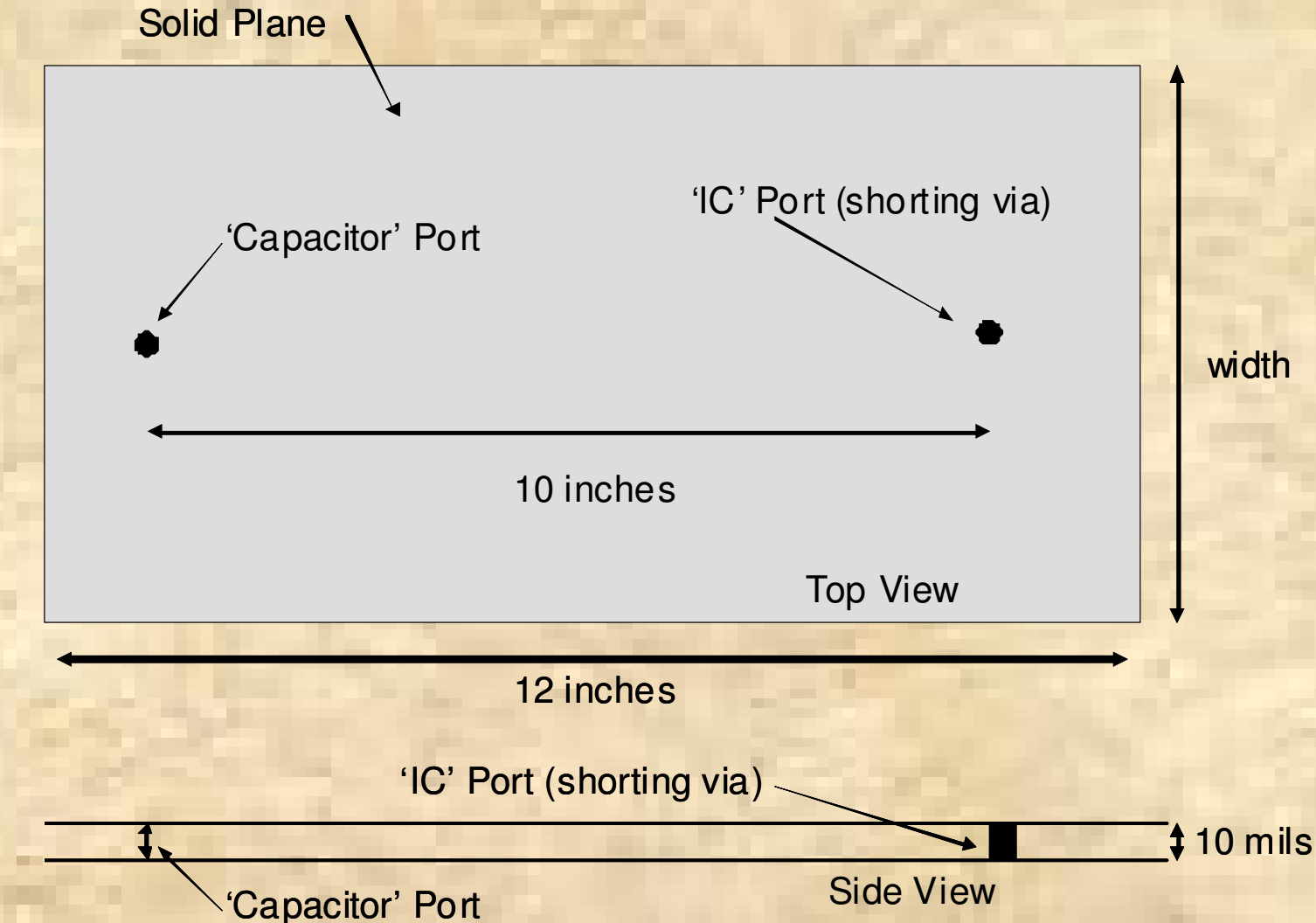
Observations

- Added via (capacitor) does not lower effective inductance to 70-75% of original single via case
- Thicker dielectric results in higher inductance
- Alternating PWR/GND can significantly reduce overall inductance

Effect of Plane width on Inductance



Geometry


Solid Plane
'IC' Port (shorting via)
'Capacitor' Port
width
10 inches
Top View
12 inches
'IC' Port (shorting via)
10 mils
'Capacitor' Port
Side View

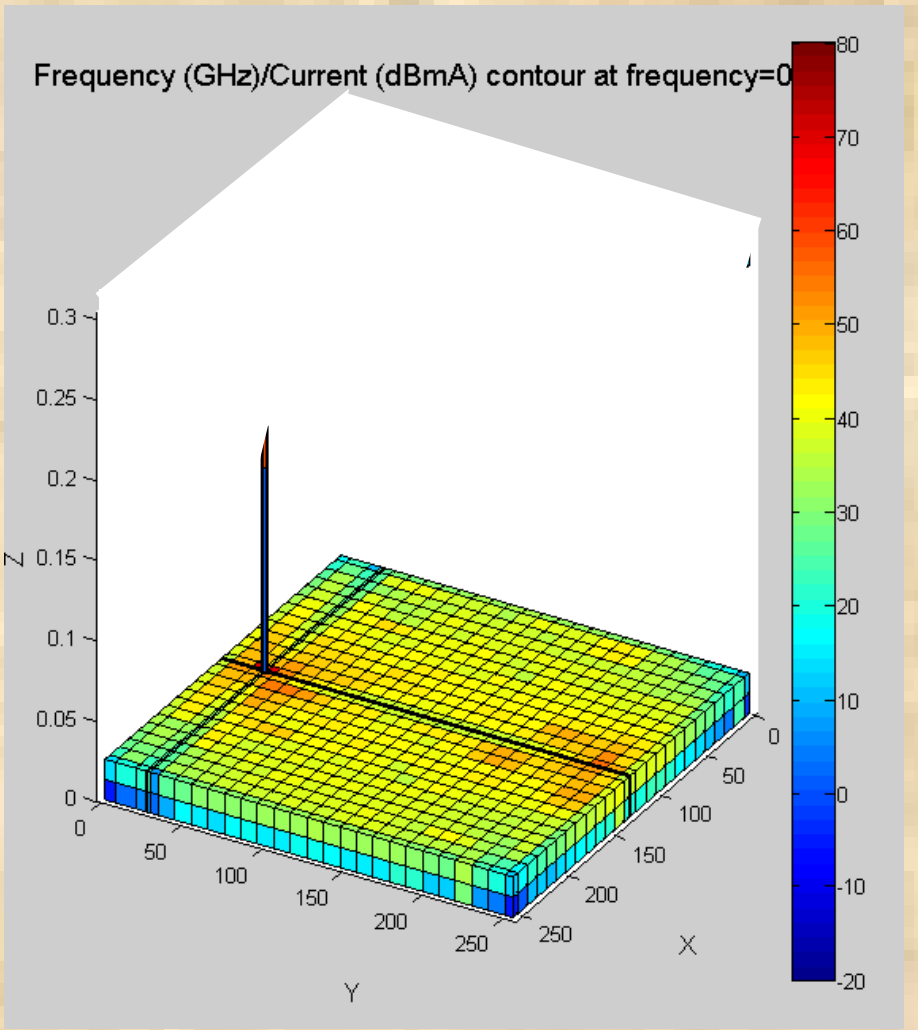
Inductance as a Function of Plane Width

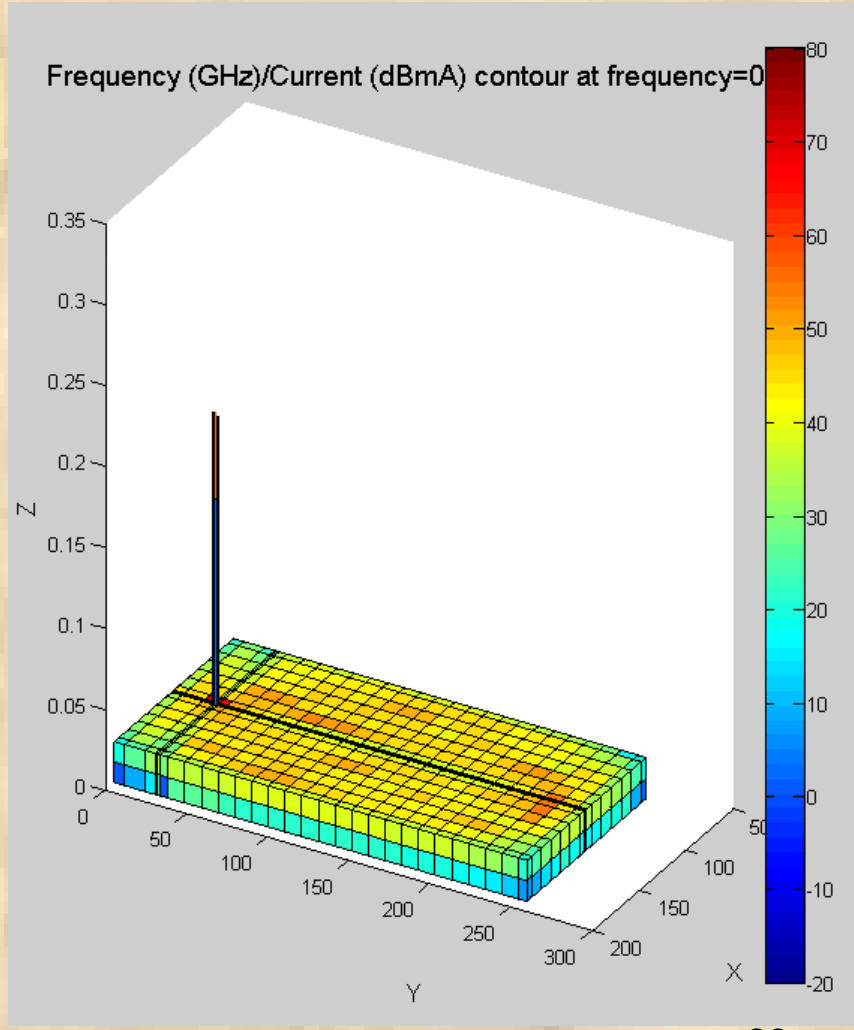
Plane Width (inches)	Inductance (pH)
10	545
5	709
2	1352
1	2574

Inductance as a Function of Plane Width

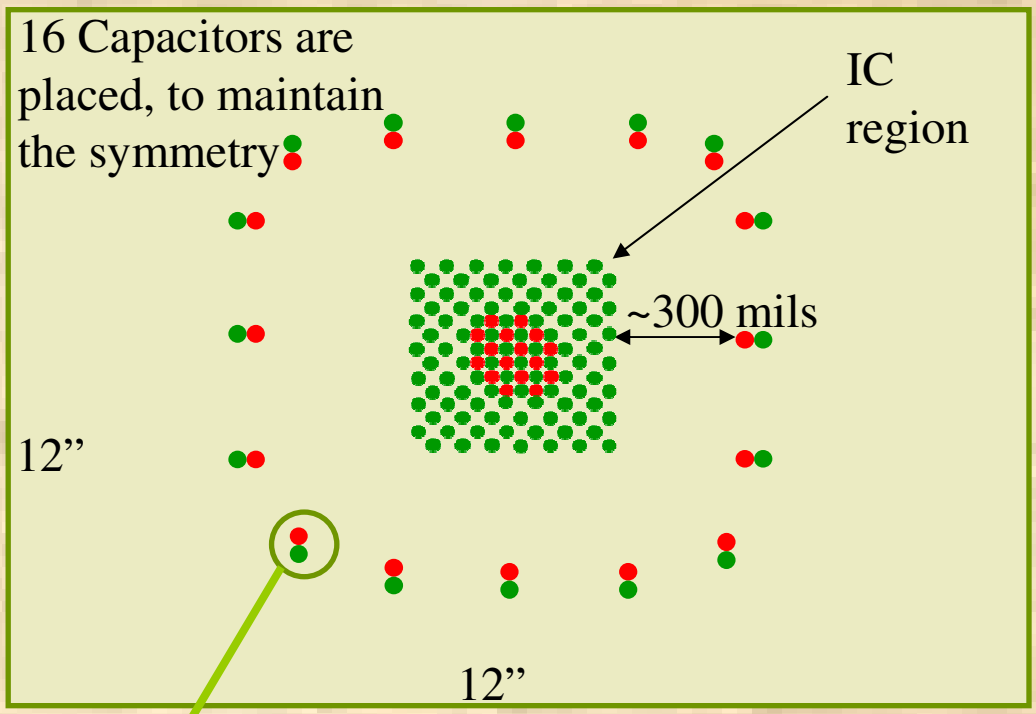
Plane Width (inches)	Inductance (pH) (Distance=10”)	Inductance (pH) (Distance=2”)	Inductance (pH) (Distance=1”)
10	545	173	154
5	709	178	156
2	1352	355	163
1	2574	658	240

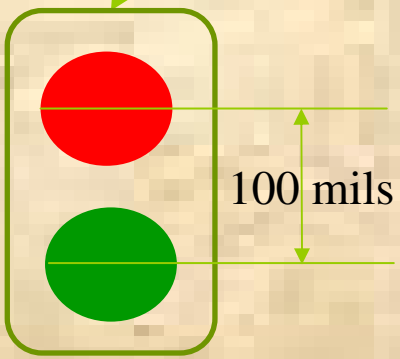
Plane Width & Current Density

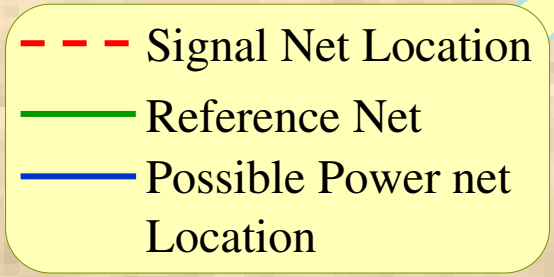


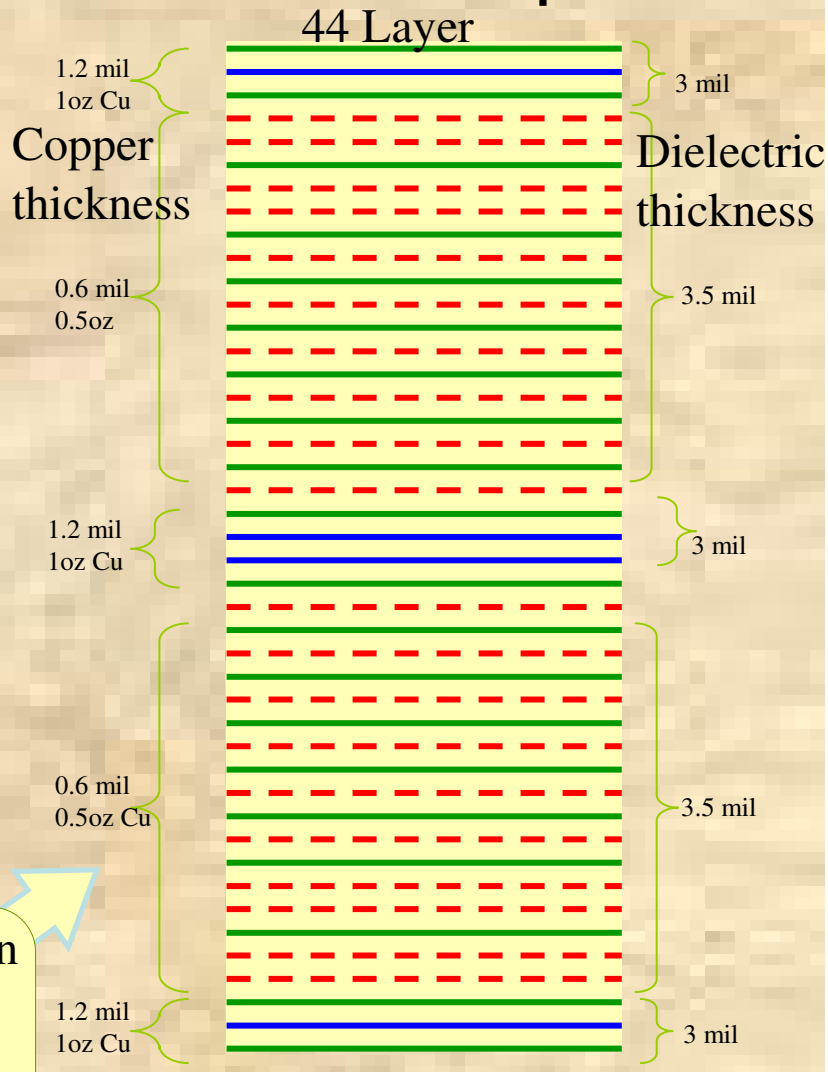


Geometry for Case Studies – Via Map

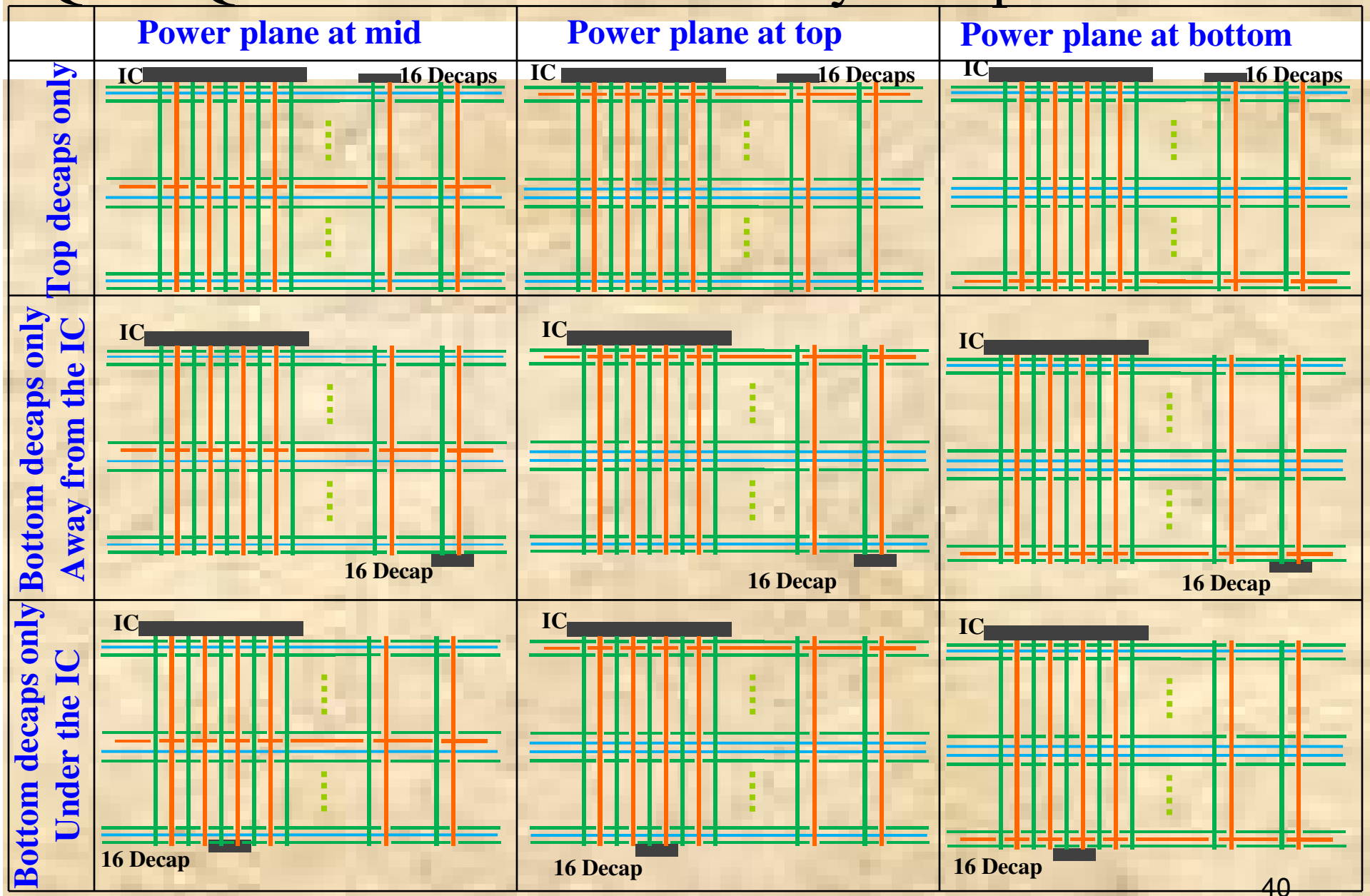




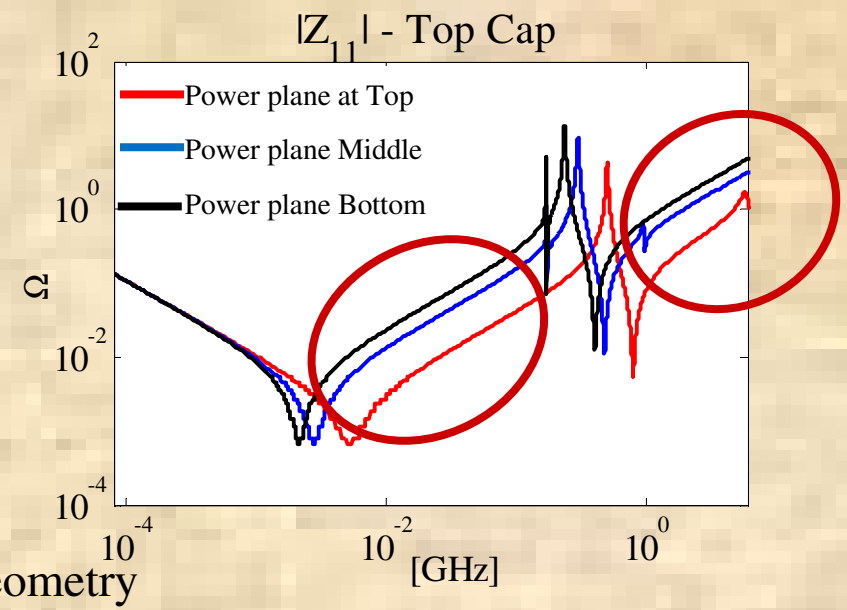


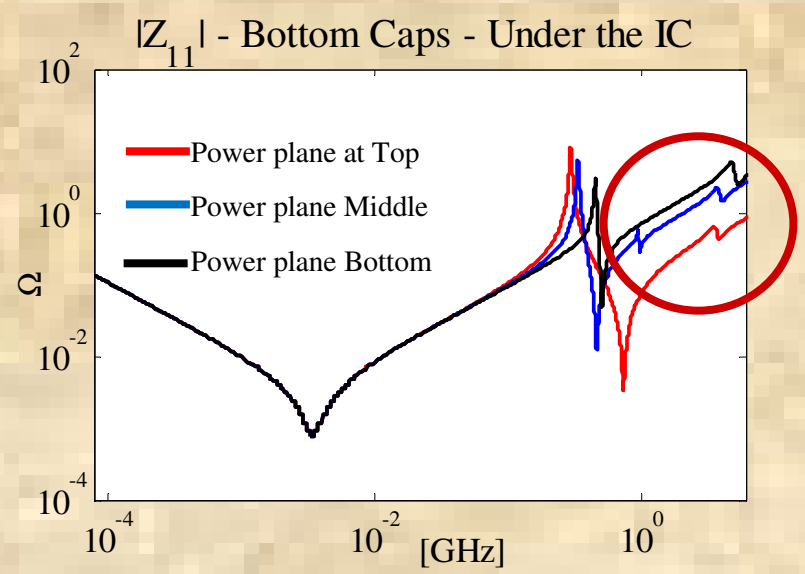


Q1 & Q2. Location of Power Layer/Caps

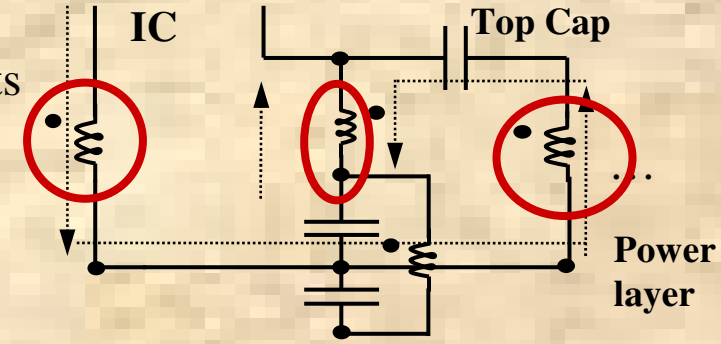


PWR Layer Location – Results

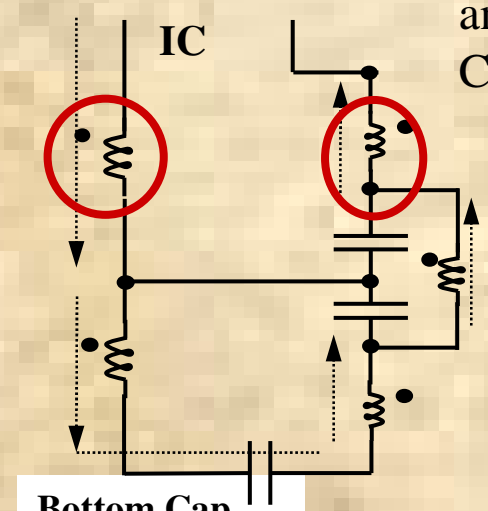




Geometry and Currents

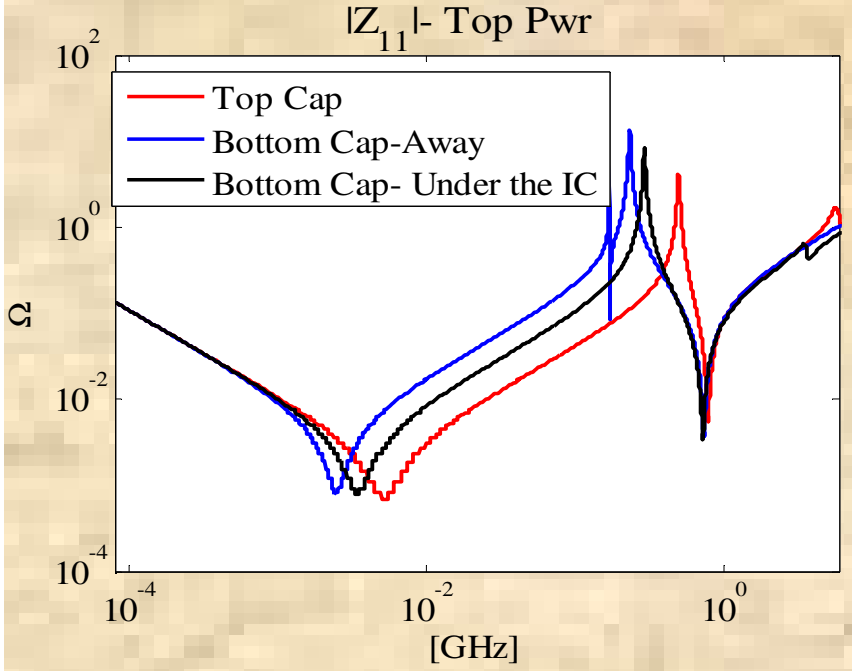


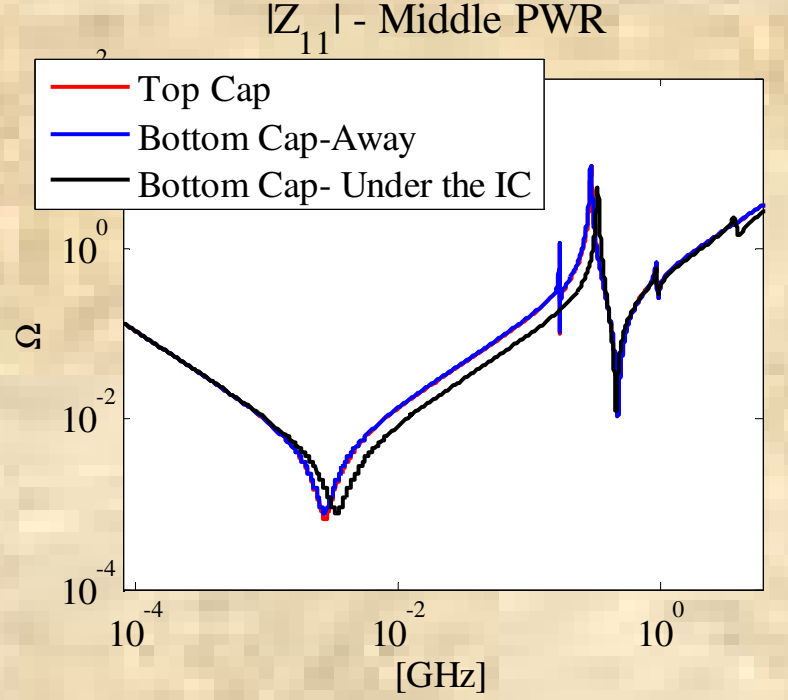
Geometry and Currents

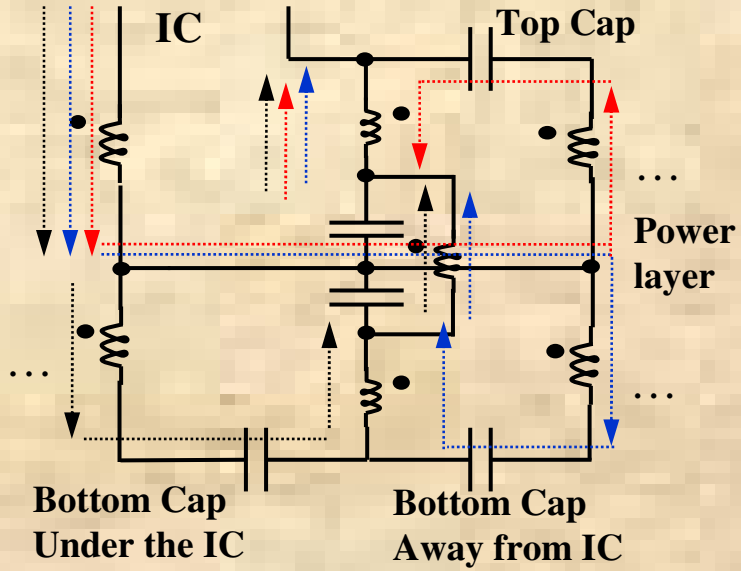


Power layer should be closest to the IC, to minimize IC to power plane inductance.

Cap Location Effect - Results

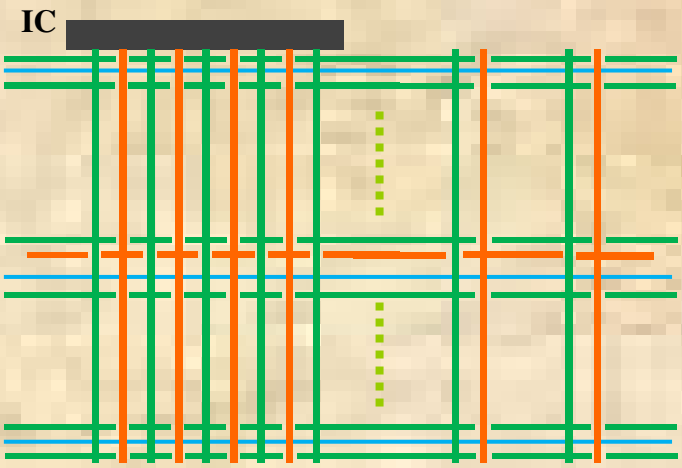




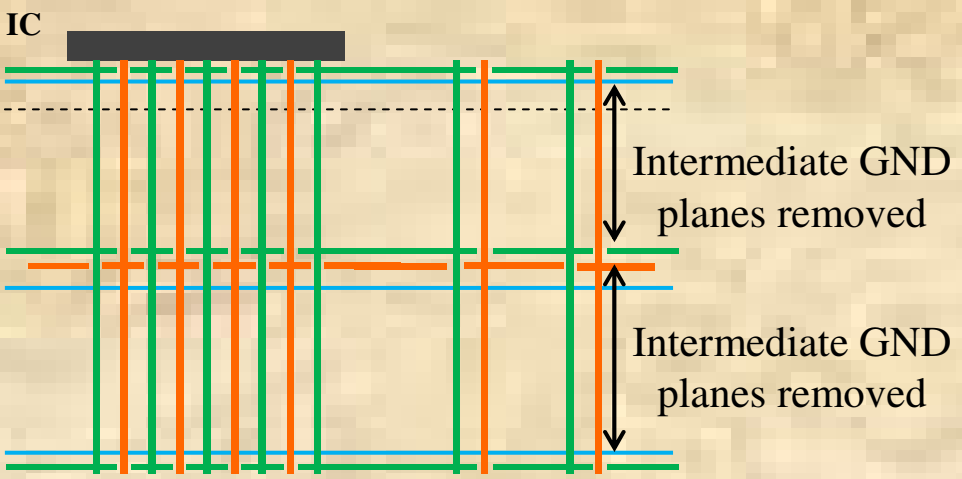


- The capacitors should to be placed on the side closest to the power plane to reduce the inductance from the capacitor to power plane.
- Capacitor location does not affect the high frequency inductance.

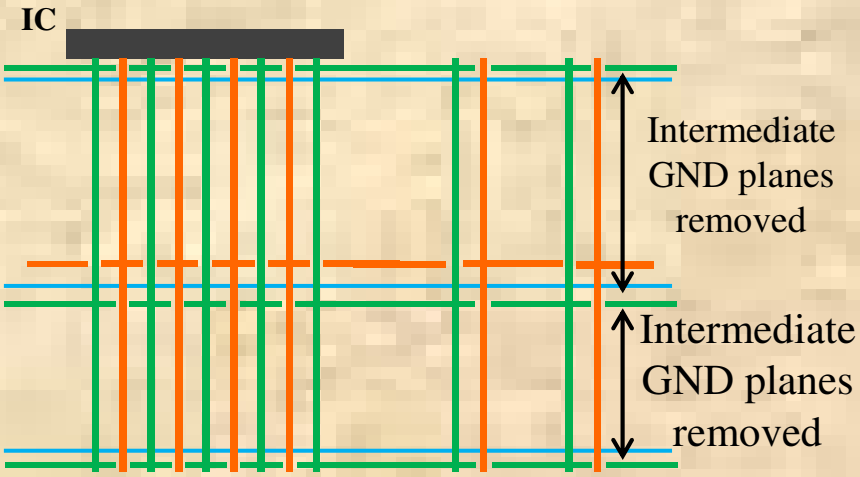
Q3. Effect of Ground Planes – Geometries



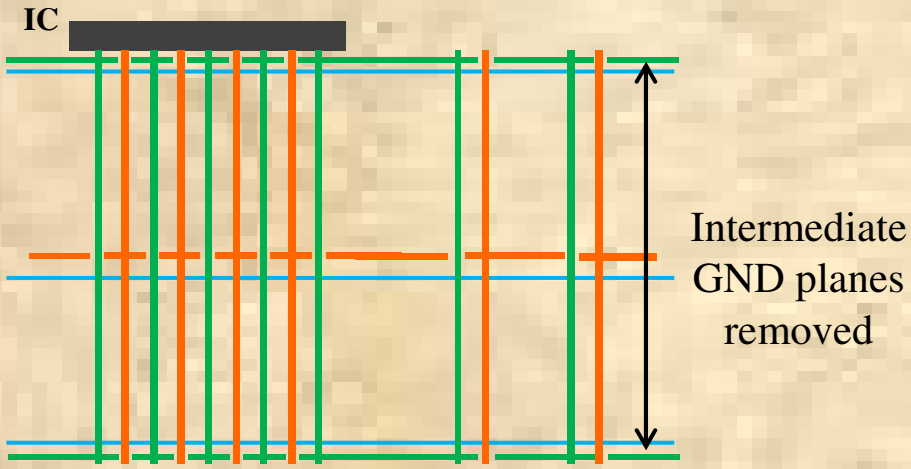
All ground planes



With top nearby ground plane



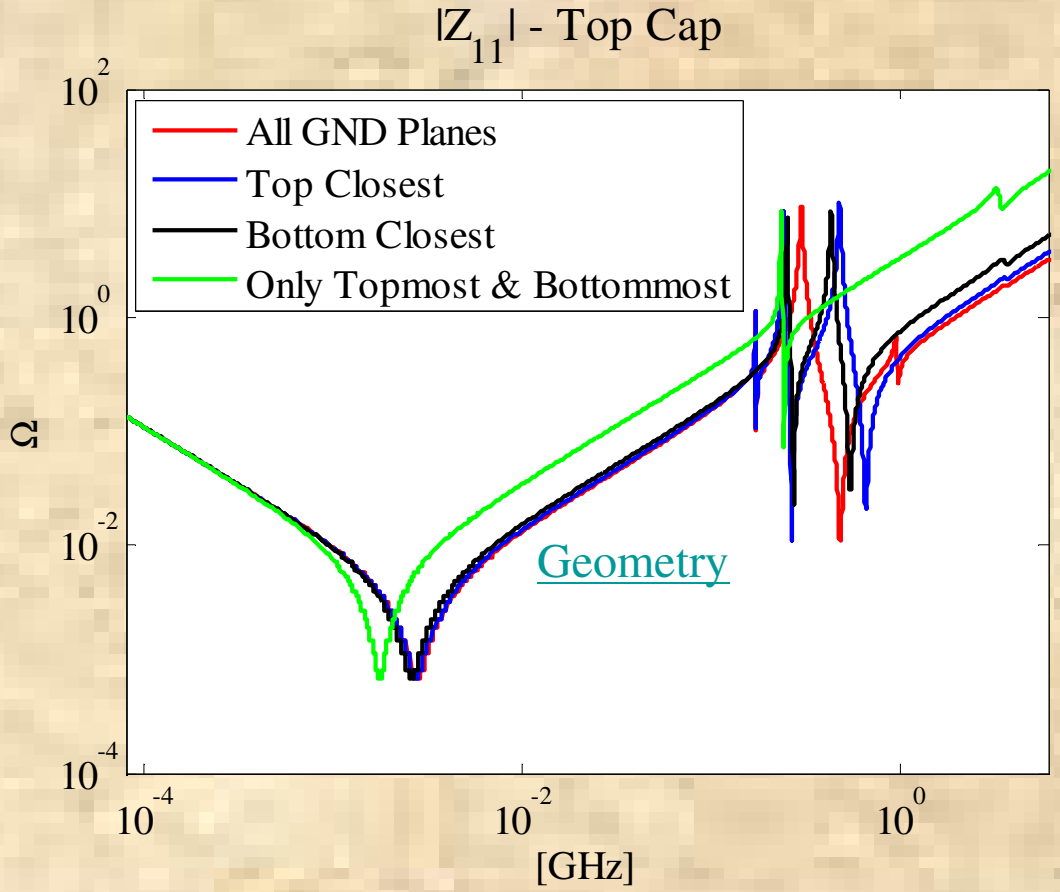
With bottom nearby ground plane

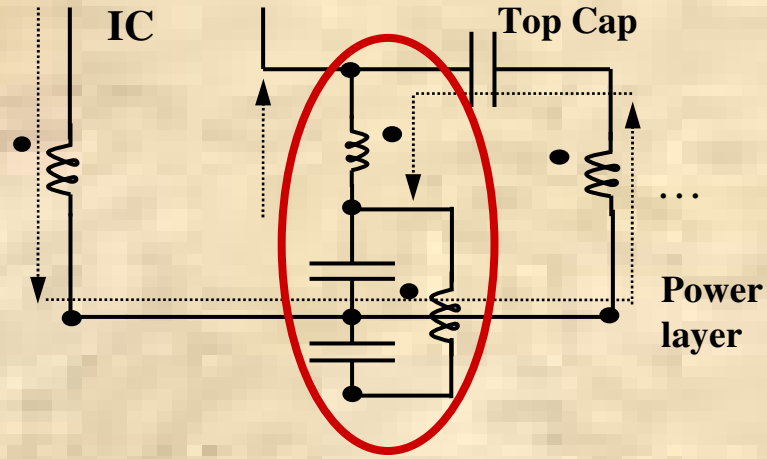


Only topmost and bottommost ground planes

Power Net under test Reference Net Floating Net

Effect of Ground Planes – Results





Geometry and current path for no GND plane case

Geometry and current path for all GND planes case

The closest ground plane from the power plane, is most important. Other Ground planes in the stack up will not affect the L_{low} or L_{high} significantly.

Power Integrity Analysis Summary

- Physical cause of inductance (current path) identified for each portion of overall path
- Value of capacitance not as important as number of capacitors
- Via connection configuration can dramatically influence inductance
- If power/Ground-reference planes deep in PCB stackup, capacitor placement has less impact than might be expected

Design Conclusions

- PWR/GND plane pair close to IC minimizes L_{IC}
- Capacitors close to the power layer minimize the inductance L_{decap} from the capacitor to the power plane.
- PWR/GND plane separation small
- Placing Caps under the IC can benefit the design, if board is thin, or the plane inductance is large.
- Ground plane closest to the power layer affects the response most, all other ground layer have very little influence.
- Ground vias for power return currents placed adjacent to the ground terminal of the capacitors reduces the inductance in the current return path