

Advanced SI Analysis – Layout Driven Assembly



Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

Tom MacDonald

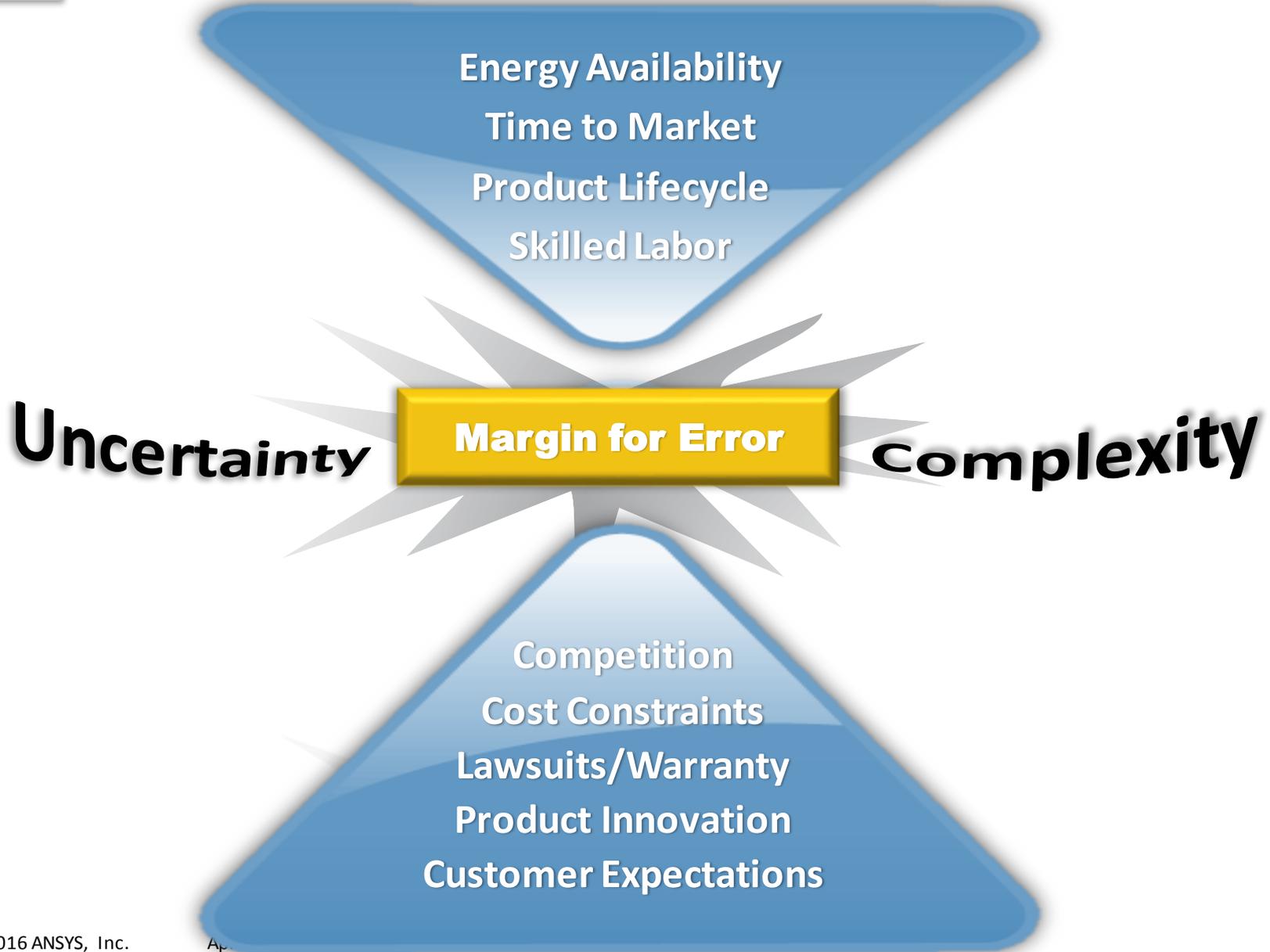
RF/SI Applications Engineer II

As the voracious appetite for technology continually grows, so too does the need for fast turn around times and efficient techniques for characterization. To improve timeliness of turns, ANSYS SI product suite offers new functionality to enhance the user experience with layout driven assembly. By combining HFSS for connectors and HFSS 3D Layout for boards, this methodology allows us to apply current best solving techniques to our problems for optimal turnaround time and accuracy.

Agenda

-  **Design Pressures**
-  **Layout Driven Assembly**
-  **Multiphysics Board Analysis**
-  **Slwave Workflow Enhancements**
-  **Q & A**

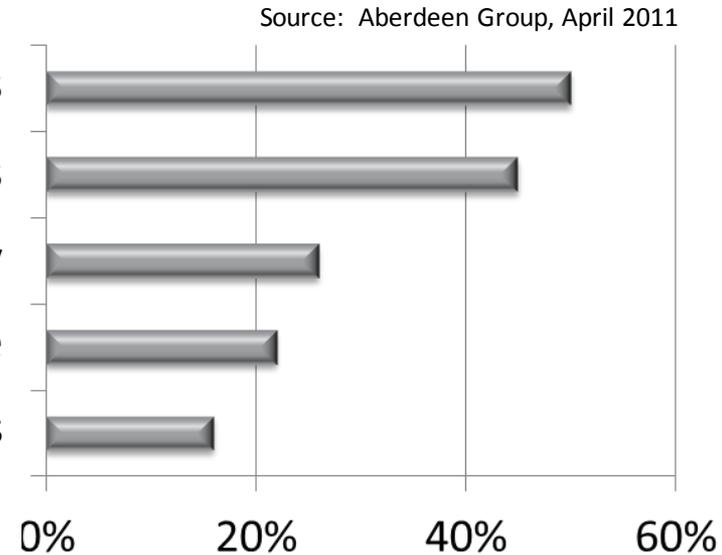
Customer Pressures



Getting Product Designs Right

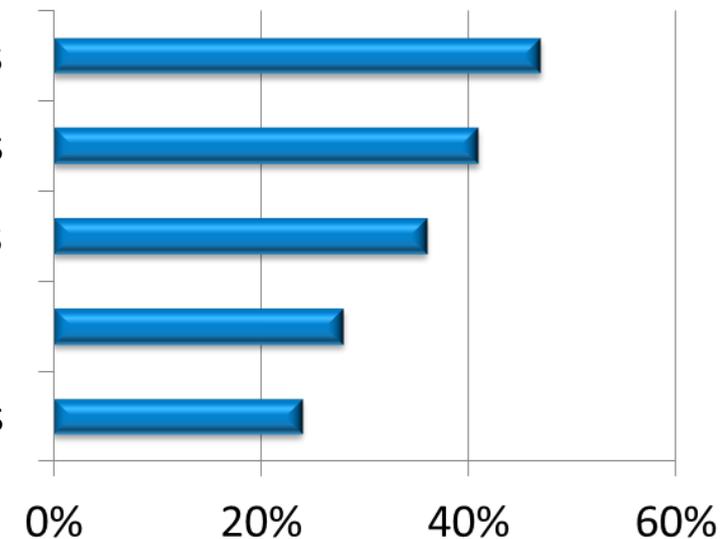
Top Business Pressures Driving Product Design Improvement

Frequent Design Changes
Compressed Schedules
Improving Quality
Need to Innovate
Additional New Features



Biggest Hurdles for Product Design

Late-Design Problems
Making Design Tradeoffs
Frequent Design Changes
Understanding Variation
Skilled Technical Experts



The screenshot displays the ANSYS Electronics Desktop interface with several active windows:

- Top Window:** ANSYS Electronics Desktop - Helical Antenna - HFSS - 3D Modeler - SOLVED. The menu bar includes File, Edit, View, Project, Draw, Modeler, HFSS, Tools, Window, and Help. The toolbar contains various simulation and modeling tools.
- Top-Left Window:** ANSYS Electronics Desktop - Helical Antenna - HFSS - Modeler. Shows a 3D model of a helical antenna with an **E Field [V/m]** plot. The legend ranges from $1.0000E+000$ to $1.0000E+002$. A scale bar indicates 6 inches.
- Top-Middle Window:** Serial_Channel - Equalized - QuickEye Statistical Eye Plot. Displays a plot titled **MEMORY & SERDES VIRTUAL COMPLIANCE**. The y-axis is Amplitude [mV] from -250.00 to 0.00, and the x-axis is UnitInterval from 0.00 to 2.00.
- Top-Right Window:** ANSYS Electronics Desktop - Co-planar Wave Guide GSG - 2D Extractor - Modeler. Shows a 2D cross-section of a waveguide with an **H [A/m]** plot. The legend ranges from $1.0000E+000$ to $1.0000E+004$. A scale bar indicates 0.2 mm.
- Bottom-Left Window:** ANSYS Electronics Desktop - Patch Antennae With Quad Feeds - Layout. Shows a 3D layout of patch antennas with a **Jsurf [A/m]** plot. The legend ranges from $1.0000E-006$ to $5.0000E-003$. A scale bar indicates 6 inches.
- Bottom-Middle Window:** ANSYS Electronics Desktop - EMC Analysis using Push Excitations - Schematic. Displays a schematic titled **ELECTROMAGNETICS WITH CIRCUITS**. It includes IBIS TX 0, IBIS TX 1, IBIS RX 0, and IBIS RX 1 models, along with a 3D model of a brain for EMC analysis.
- Bottom-Right Window:** ANSYS Electronics Desktop - 32 Pin TSSOP - Q3D - Modeler. Shows a 3D model of a 32-pin TSSOP package with a **JAC [A/m]** plot. The legend ranges from $1.0000E-003$ to $1.0000E+003$. A scale bar indicates 3 mm.

HFSS 3D Layout

HFSS interface optimized for layout designs

Stackup editor

Trace, pads, vias bond wires, solder bumps and balls

Same 3D accuracy of HFSS in automated design flow



ANSYS HFSS The Industry's Premier EM Field Simulator

3-D Electrical Layout

3-D Modeler

ANSYS HFSS now includes two interfaces optimized for easy design entry:

- 3-D electrical layout to create parameterized PCB, electronic packages, MMICs and IC layouts
- 3-D modeler to construct arbitrary 3-D geometry, such as antennas, RF/microwave components and biomedical devices

Layout Driven Assembly



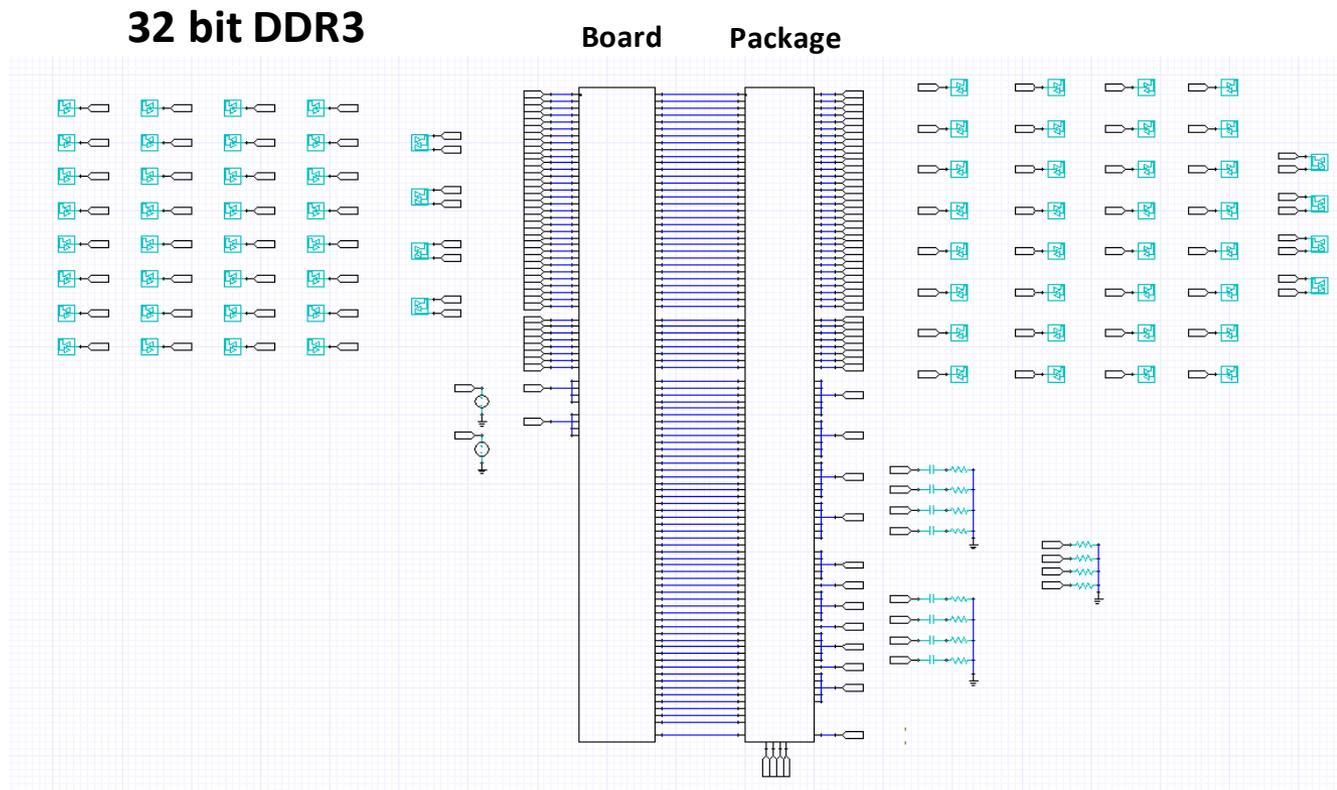
Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

The old way of analyzing a package system plus a board



Package on Board Example

Last year...



Challenge: requires the use of 2-3 software packages

Next step: make a design change

Next step challenges:

- **Keep track of touchstone revs**
- **Making changes to SIwave design (no variables)**

Package on Board Example

Present Day...

Extract board
using SIwave



Extract
package using
HFSS



Assemble full
3D model



Run linear
network
analysis

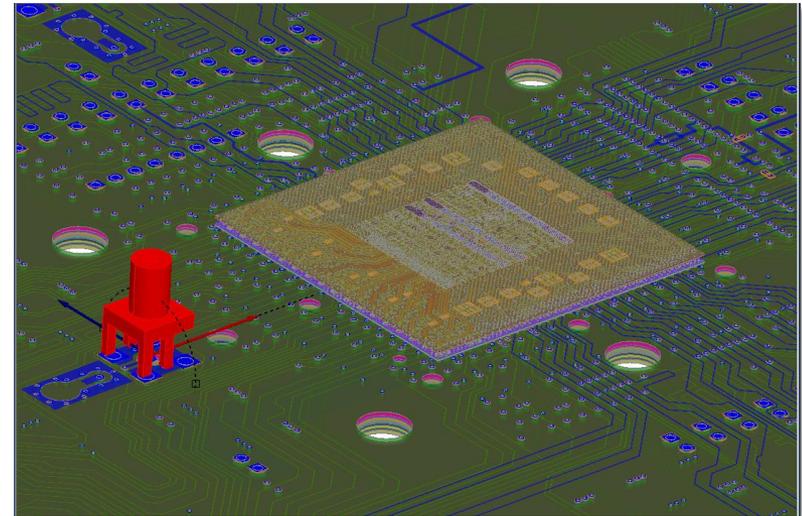
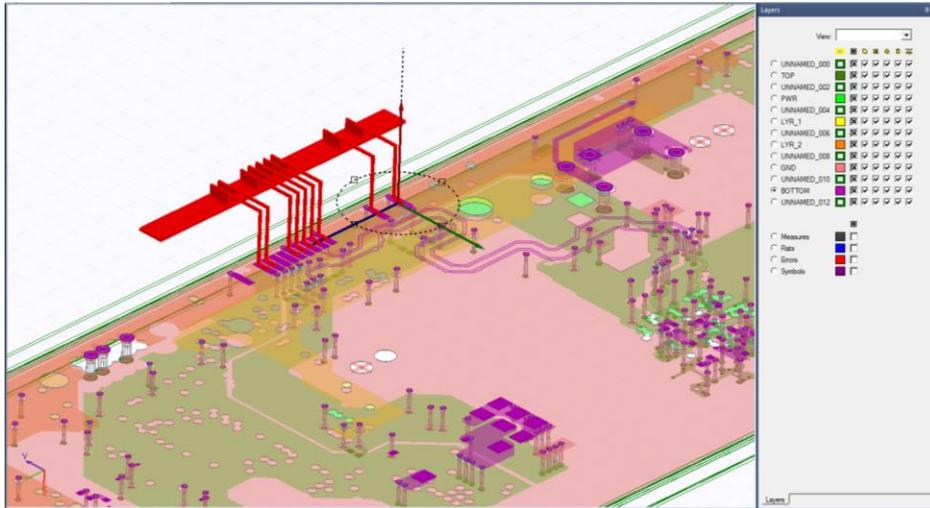
Benefit: requires the use 1 software package (Electronics Desktop)

Next step: make a design change

Benefits:

- **No need to keep track of touchstone revs**
- **Layout interface enables parametric SIwave designs**

Layout-Driven Assembly in ANSYS Electronics Desktop

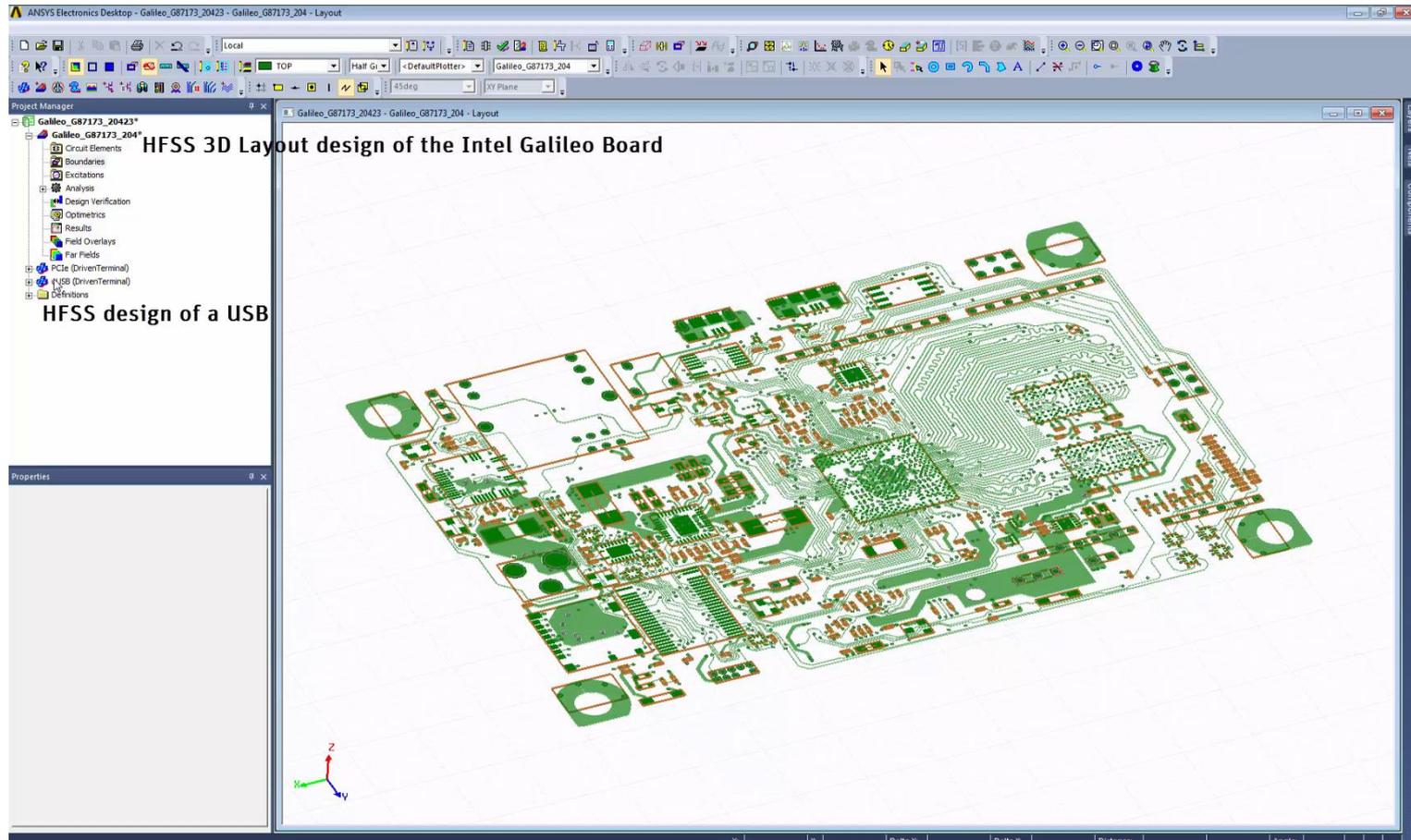


Place and connect components in Layout
Simulate components with 3D accuracy

ECAD and MCAD
HFSS, SIwave, Q3D

Apply automated circuit simulation to capture full system behavior

Ease-of-use drive 3D simulation for design engineers

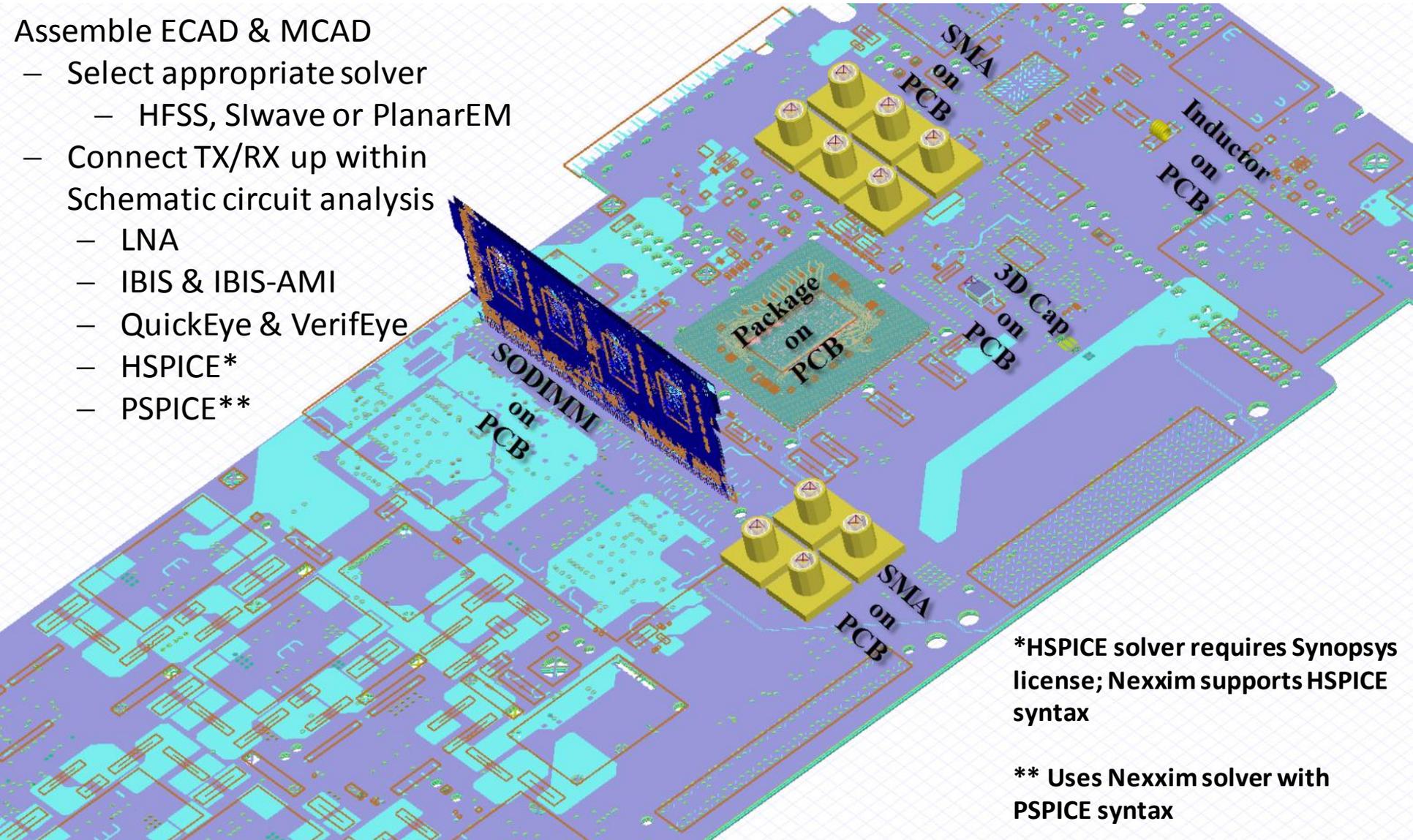


Reducing hands on engineering time

- **Eliminate error prone system wiring**

Assemble ECAD & MCAD

- Select appropriate solver
 - HFSS, Siwave or PlanarEM
- Connect TX/RX up within Schematic circuit analysis
 - LNA
 - IBIS & IBIS-AMI
 - QuickEye & VerifEye
 - HSPICE*
 - PSPICE**

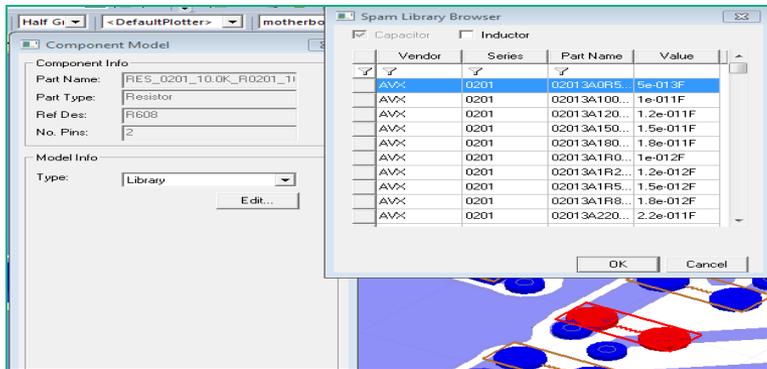
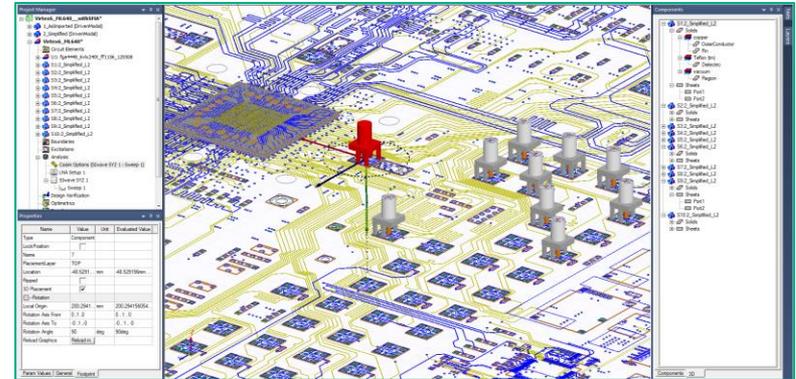


*HSPICE solver requires Synopsys license; Nexxim supports HSPICE syntax

** Uses Nexxim solver with PSPICE syntax

3D Layout: Key Features

- HFSS 3D Dynamic Link in Layout
- 3D Placement and Positioning
- Improved Capacity and Layout Rendering

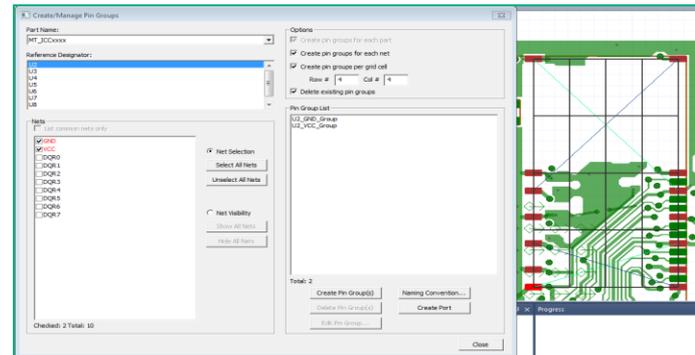


Linear Network Analysis for Co-simulation

- LNA Setup and automated Net listing
- Component Models

Siwave technology for large PCBs and packages

- SYZ Solver
- Geometry Checks



HFSS 3D Workflow Enhancements



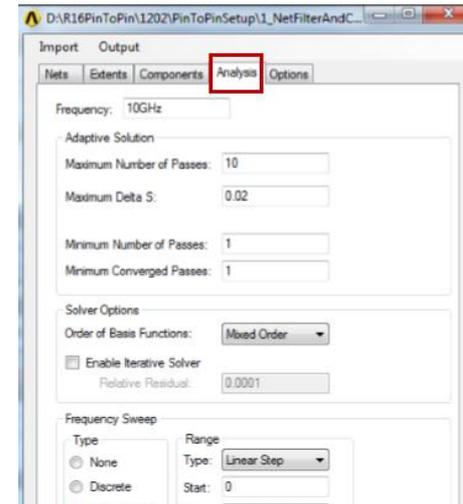
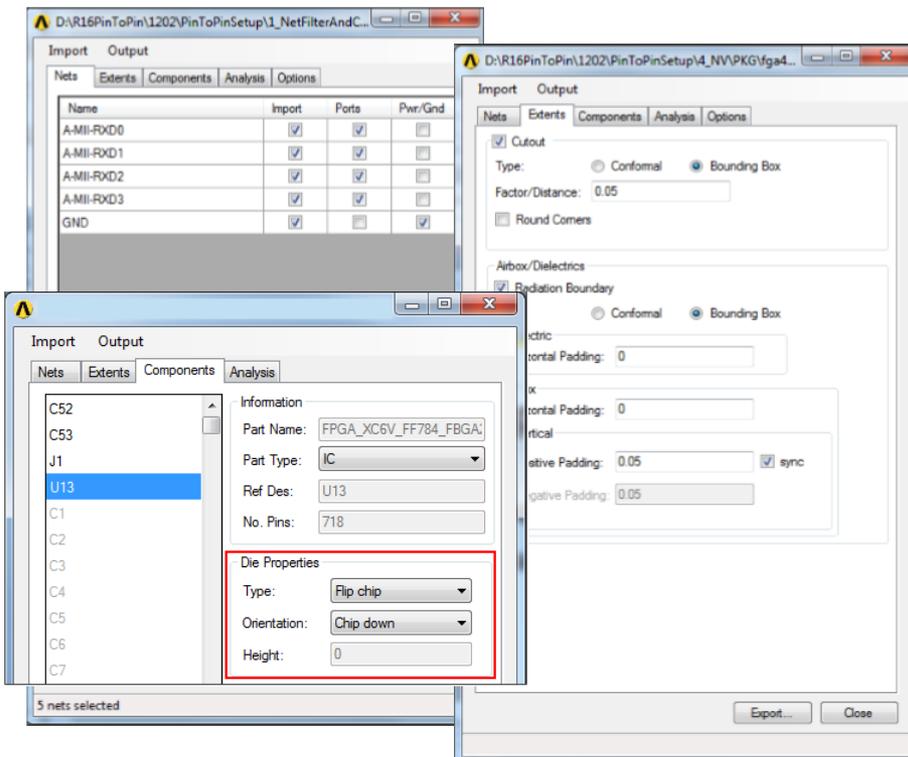
Fluid Dynamics

Structural Mechanics

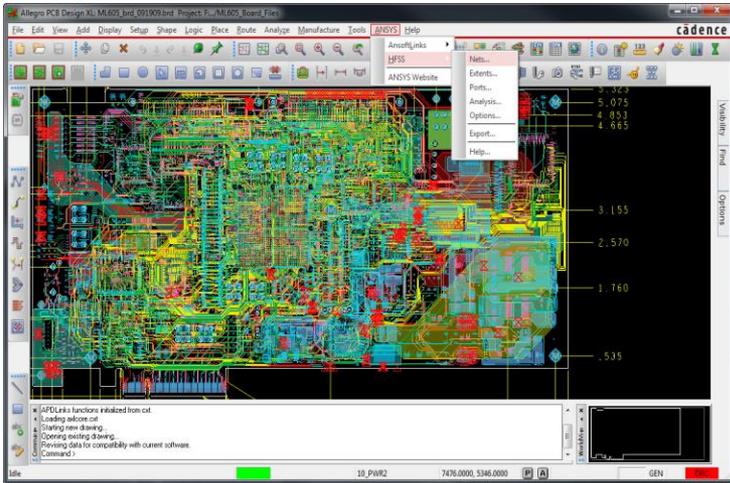
Electromagnetics

Systems and Multiphysics

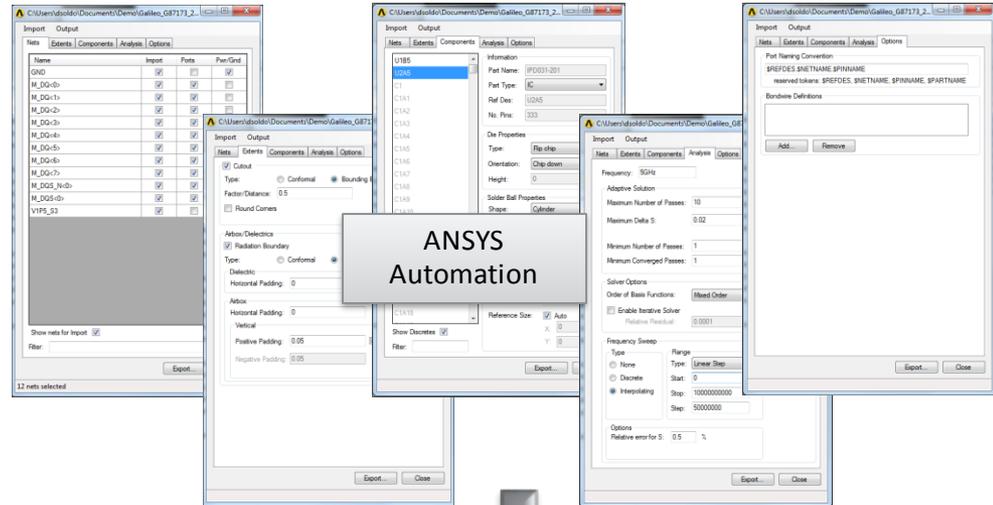
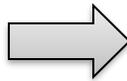
- .Net utility written to highlight layout automation
- Can be run with or without GUI
- Starts from .mcm or .brd



```
<?xml version="1.0" encoding="UTF-8" standalone="no" ?>
<!-- Control plane -->
<!-- Component definitions -->
<!-- Configure these parts with specific modules -->
<!-- All inductors should also be set to Other type, which requires setting to "Discrete" here. This allows for easy ports in HFSS -->
<!-- Any component not matching above filters will get whatever values might be present in the Cadence files, if any -->
</TypeTag>
</Component>
<!-- Import options -->
</ImportOptions>
</Pin2Pin>
```

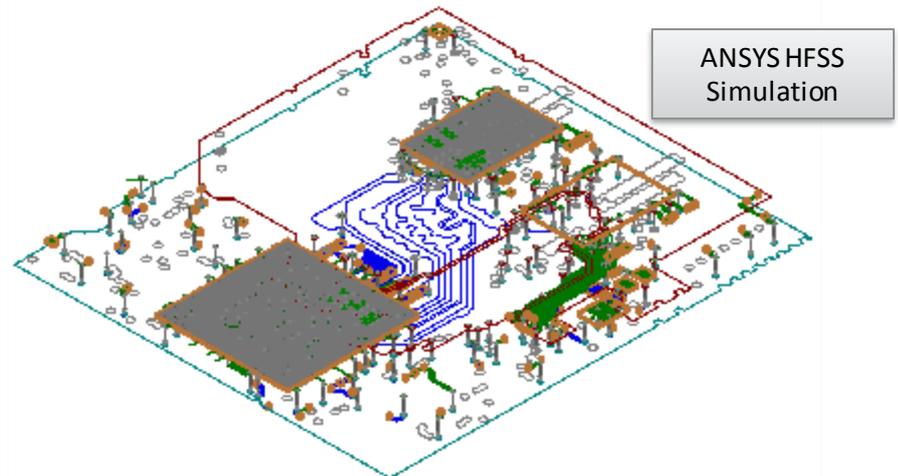


Layout



Simulation Democratization

- Time is best spent in design exploration and results analysis
- Unfortunately, a lot of time is spent preparing the model for simulation
- Automation of pre-processing would free up more of the engineer's time for design innovation



ANSYS HFSS Simulation

Multiphysics Board Analysis



Fluid Dynamics

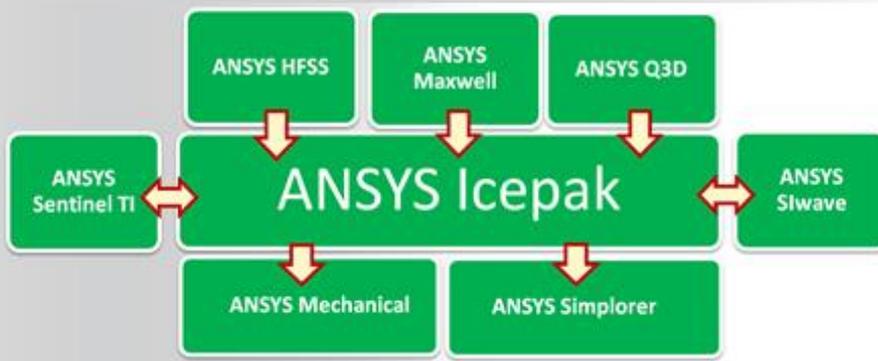
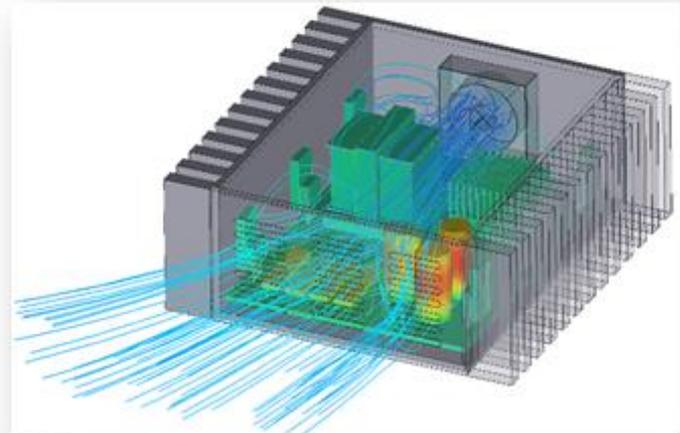
Structural Mechanics

Electromagnetics

Systems and Multiphysics

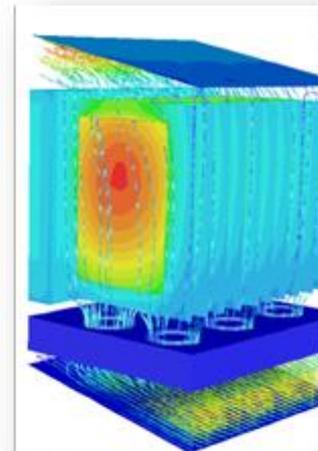
Solver Validated by Experts

ANSYS Icepak uses ANSYS Fluent as the solver engine, which is recognized as the market leader for both speed and accuracy of CFD



Customized for Thermal Management

ANSYS Icepak contains a streamlined user interface with "smart objects" to rapidly create models of electronics assemblies



Coupling Electromagnetics, Mechanical & Thermal Simulations

ANSYS Icepak can be connected to ANSYS mechanical or electromagnetic simulation solutions inside the Workbench environments to simulate the complete performance of a product

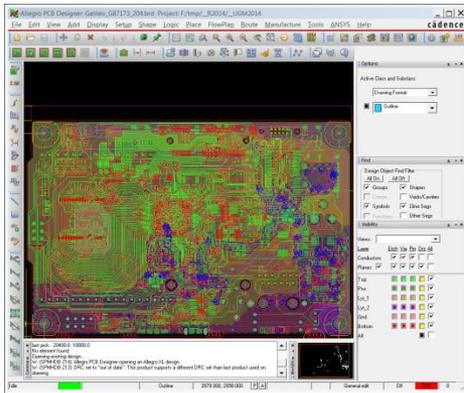
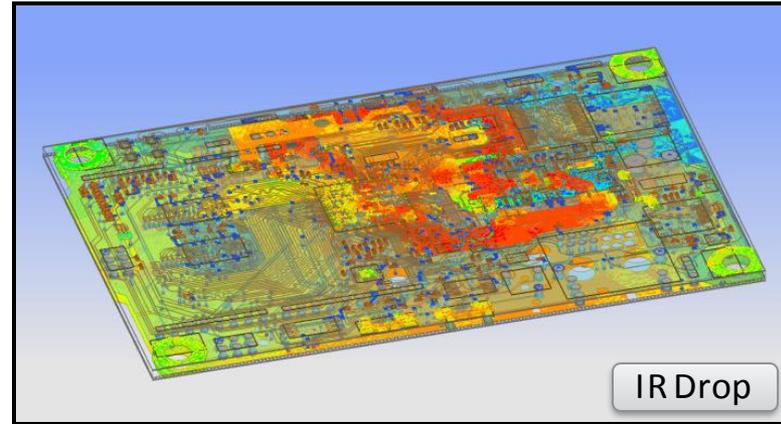
DC Heating

SIwave for DC

ECAD Translators

User Interface

I²R DC Analysis



Cadence Allegro
BRD file

SIwave
User Interface

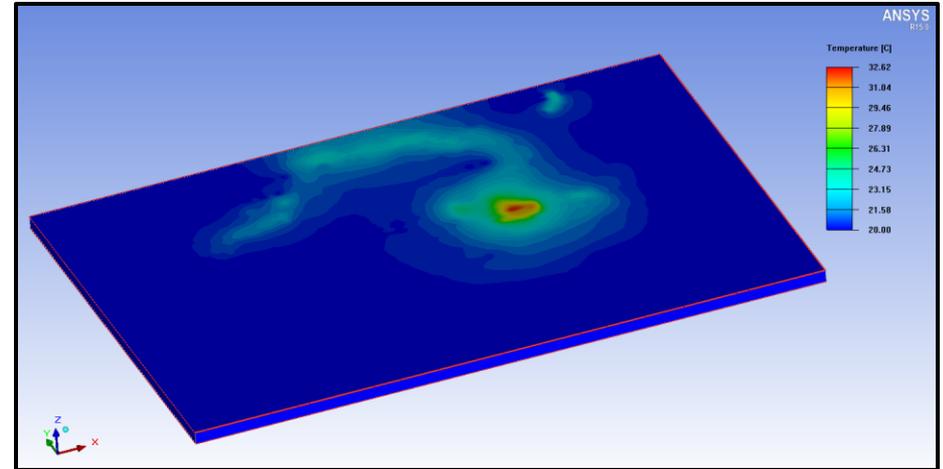
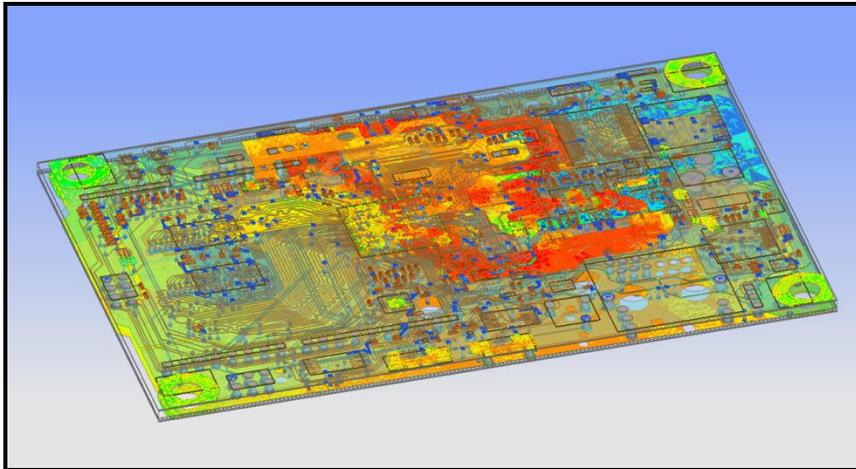
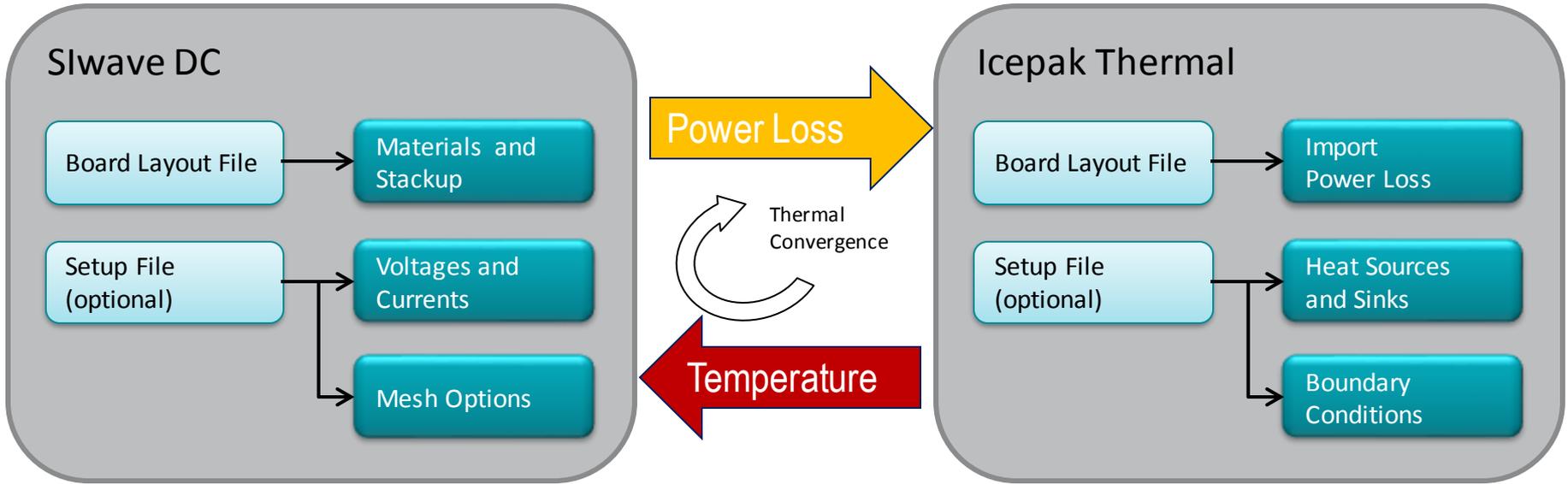
DC Setup
Voltage/Current
Sources

Components

- Voltage Probes
- Current Sources
 - I_U4A1_1P5
 - I_U1A1_1P5
 - I_U1B5_1P5
 - I_U2A2_1P5
 - I_U2A3_3P3
 - I_U2A4_1P5
 - I_U2A5_1P0
 - I_U2A5_1P5
 - I_U2A5_3P3
 - I_U2L1_3P3
 - I_U2M1_3P3
- Voltage Sources
 - V_1P0_U3A1
 - V_1P5_U2A4
 - V_1P5_U3A1
 - V_3P3_U3A1
- Integrated Circuits
- Input/Output

Simulate

Two-way coupled Thermal Heating



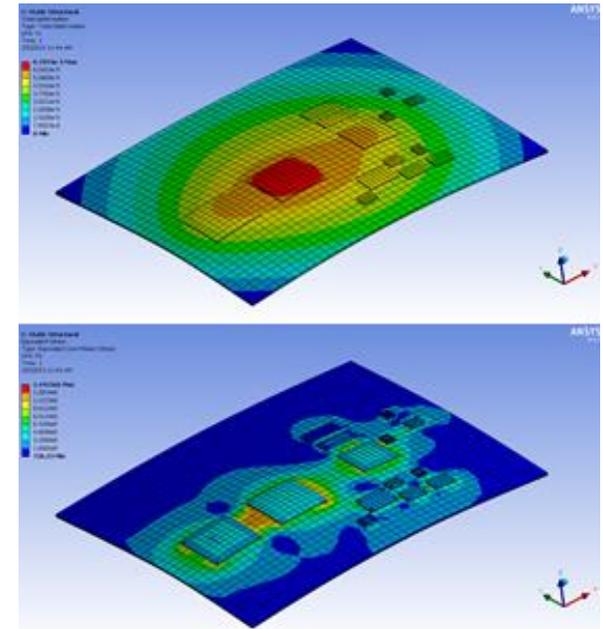
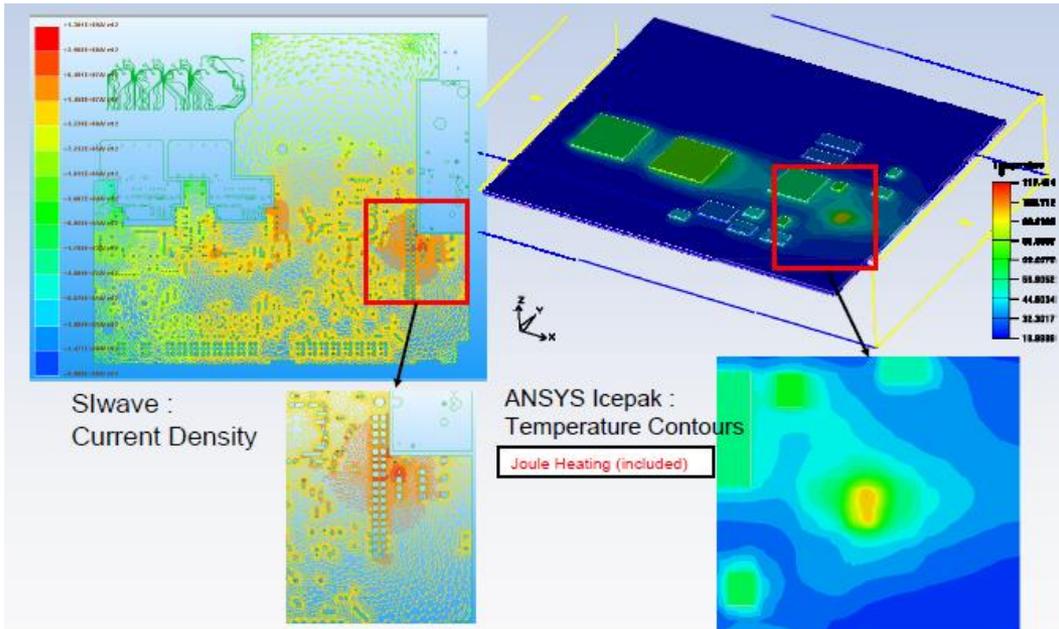
ANSYS Solutions for Pkg/PCB

Thermal Management Design Challenges

- Thermal impact to IC
- Electric / Thermal Co-Analysis for PKG/PCB
- Automation of pre-processing would free up more of the engineer's time for design innovation
- Thermal impact for mechanical stress
- Optimization of power, weight, and thermal design requirements

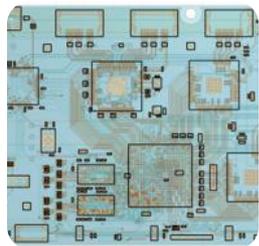
Electrical / Thermal Co-Simulation

Thermal / Mechanical Co-Simulation

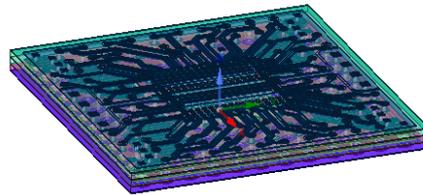


ANSYS Mechanical can be used to predict stresses and deformation in the package during

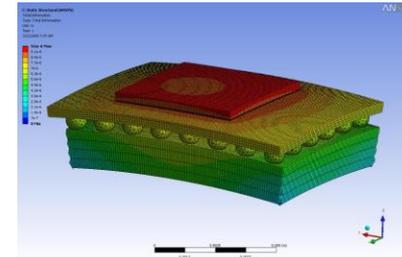
- Flip Chip Attachment
 - Crack Initiation and Crack Growth
- Thermal Cycling
 - Solder Joint Reliability
- Shock Analysis



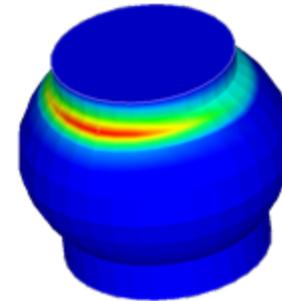
Layout Tool*



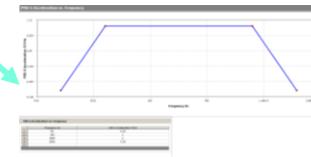
ANSYS
Mechanical



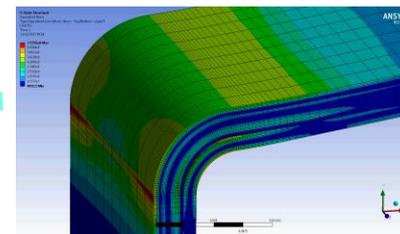
Flip chip
Attachment



Solder Joint
Reliability

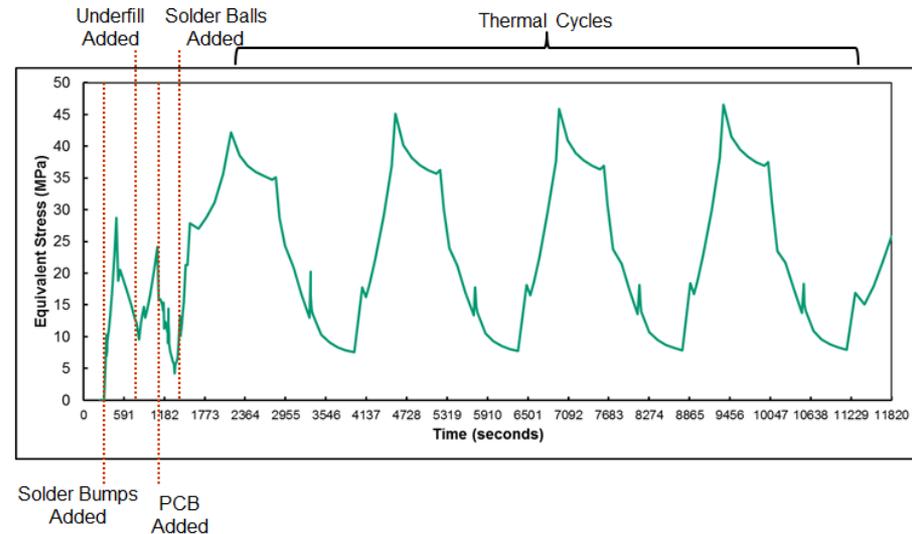
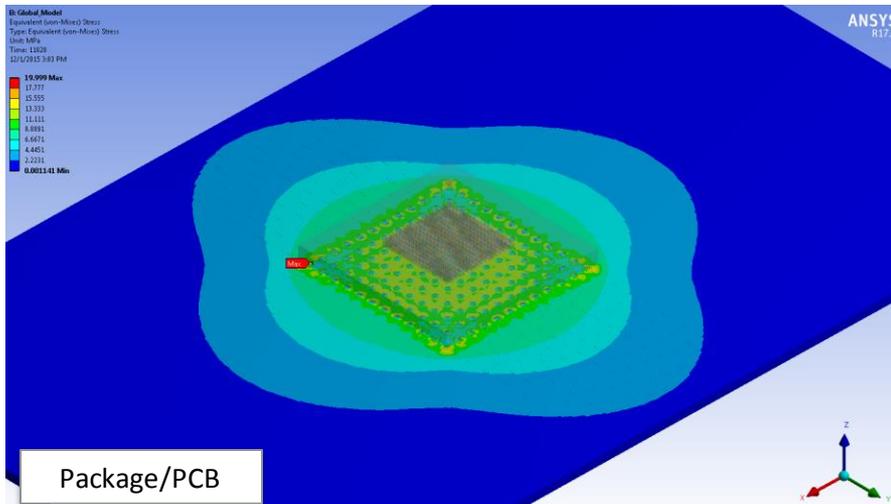
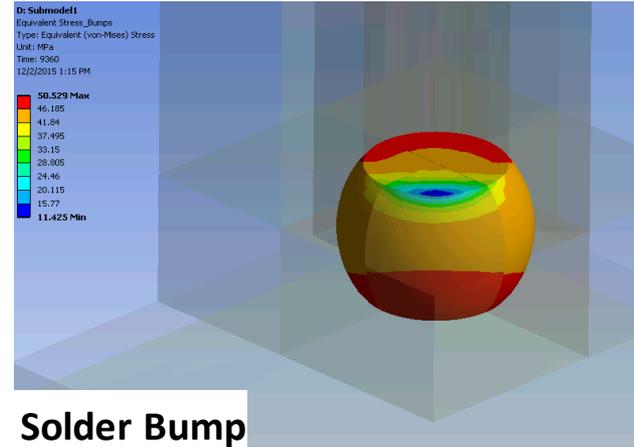
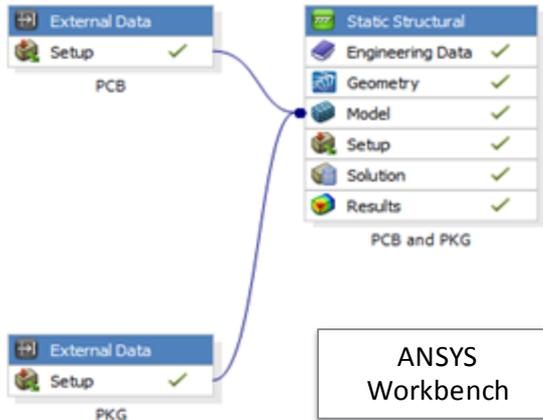


Shock
Analysis



Crack

Mechanical: Electronics Assembly



Siwave Workflow Enhancements

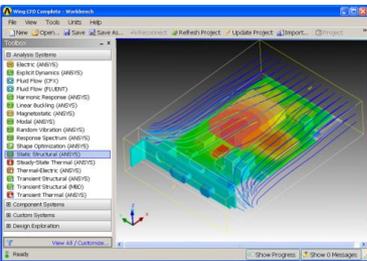


Fluid Dynamics

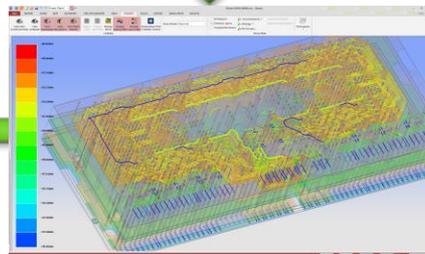
Structural Mechanics

Electromagnetics

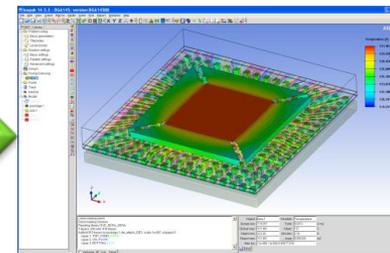
Systems and Multiphysics



Workbench

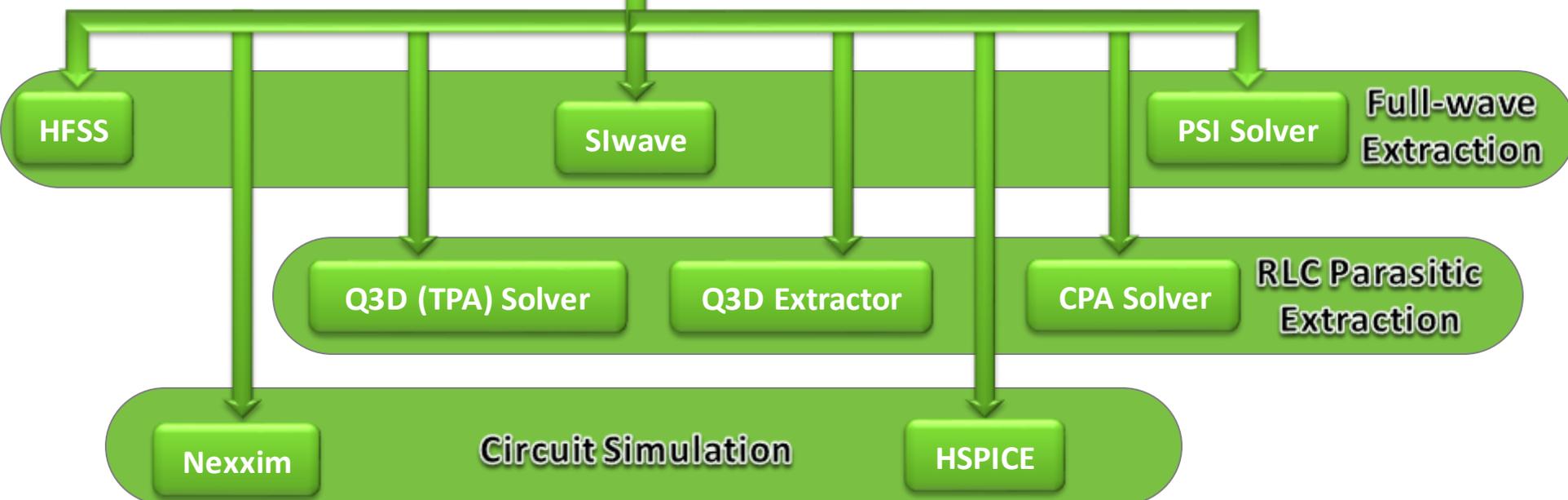


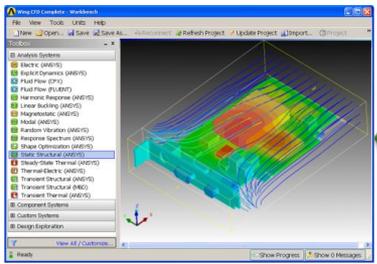
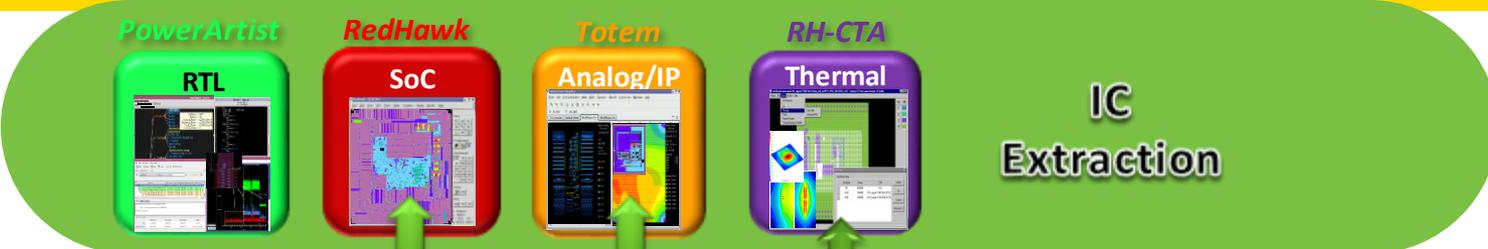
SIwave



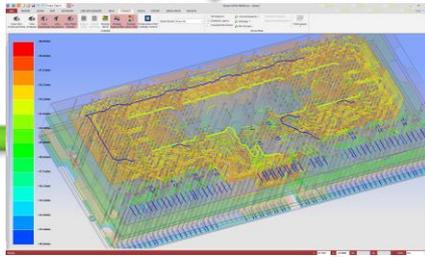
Icepak

Multi-physics

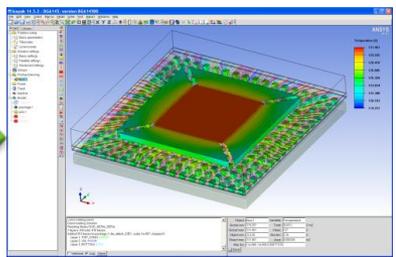




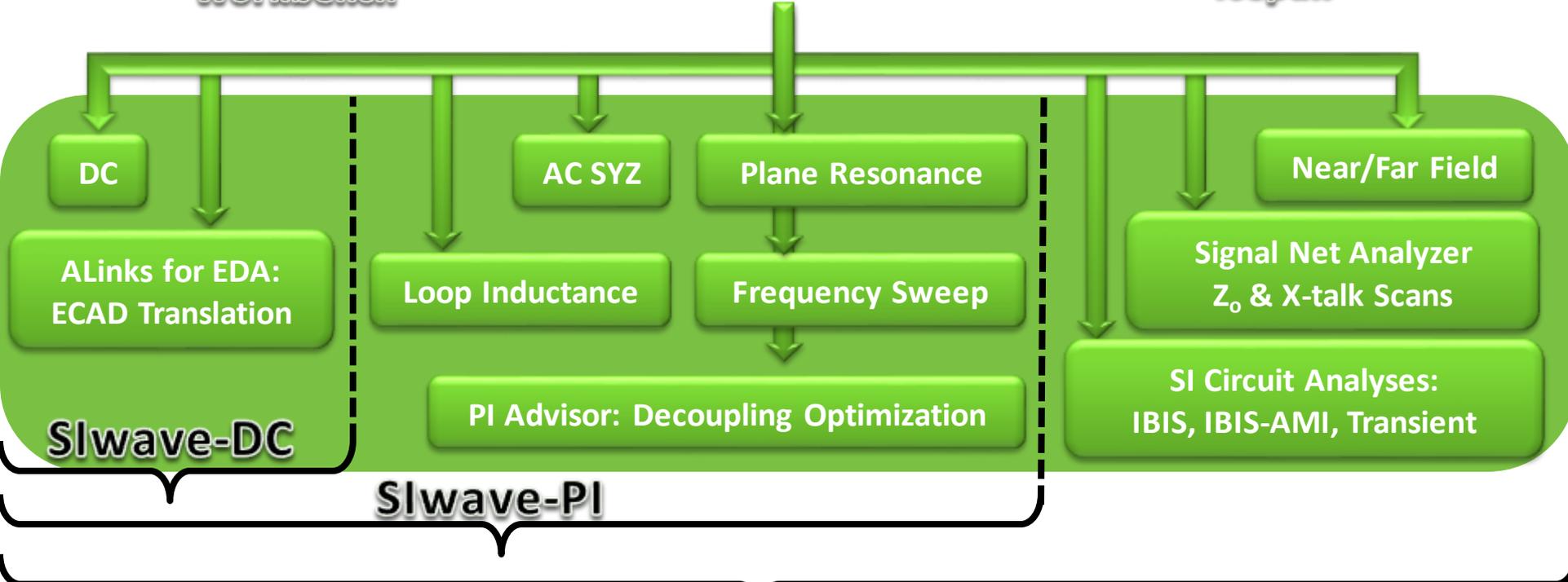
Workbench



Siwave Core Solvers



Icepak



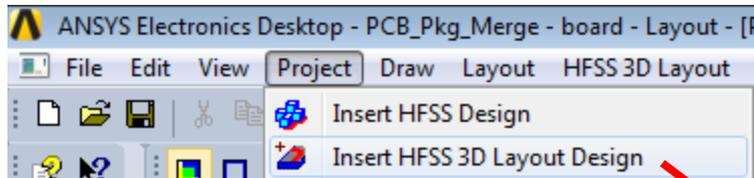
Siwave SYZ Solver Integration into AEDT 3D Layout

Siwave Solution Setups are now part of ANSYS Electronics Desktop 3D Layout

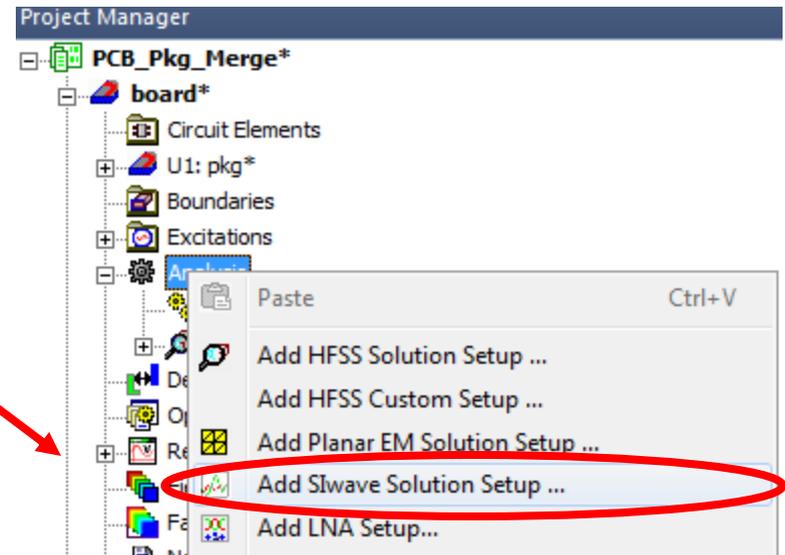
Enables parametric solves

Enables usage of Electromagnetics RSM

Insert HFSS 3D Layout Design



Add Siwave AC SYZ Solution

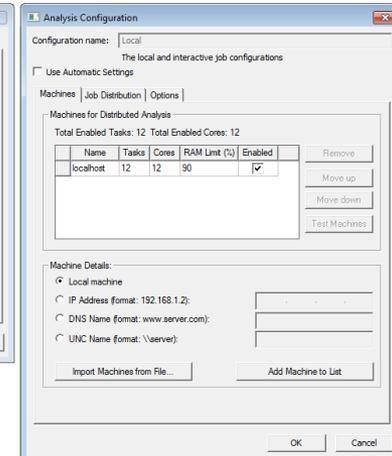
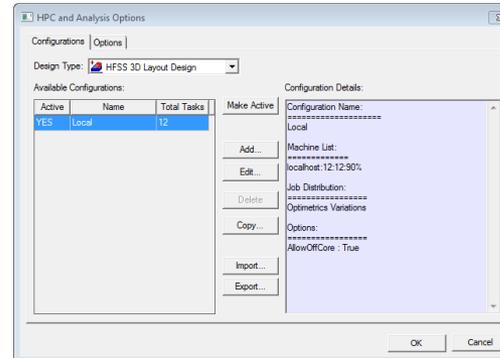
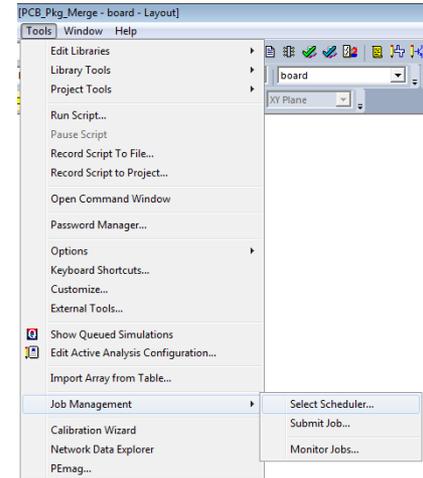
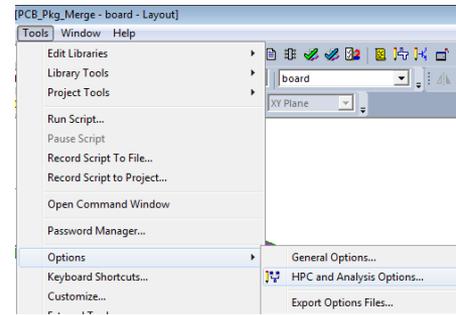
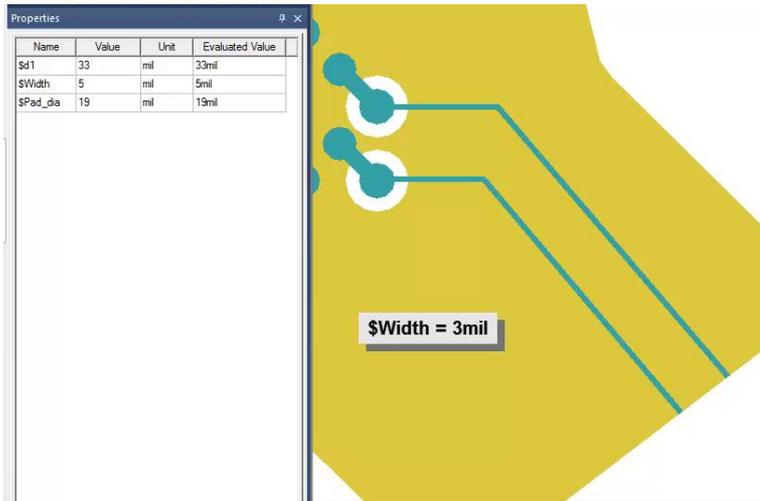


Slwave SYZ Solver Integration into AEDT 3D Layout

Slwave Solution Setups are now part of ANSYS Electronics Desktop 3D Layout

Enables parametric solves

Enables usage of Electromagnetics RSM so that jobs can be submitted to a cluster



SIwave Parametric Design within AEDT 3D Layout

Project Manager

- SIwave_3D_Layout_PKG_PCB*
- SIwave_3D_Layout_PKG_PCB*
 - Circuit Elements
 - Boundaries
 - Excitations
 - Analysis
 - Cosim Options (HFSS)
 - SIwave SVZ 1
 - Sweep 1
 - Design Verification
 - Optimetrics
 - ParametricSetup1
 - Results
 - Field Overlays
 - Far Fields
 - Definitions

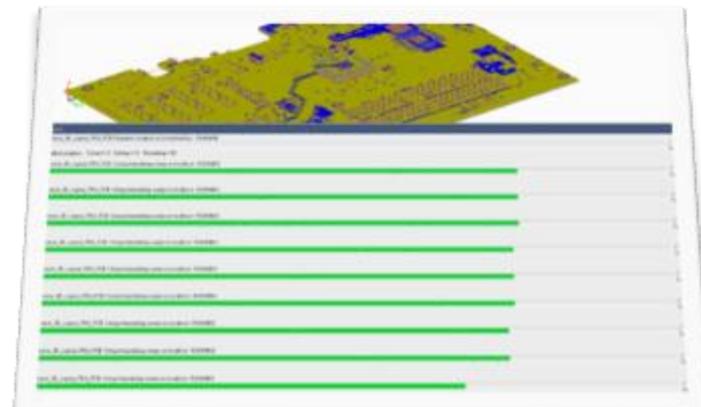
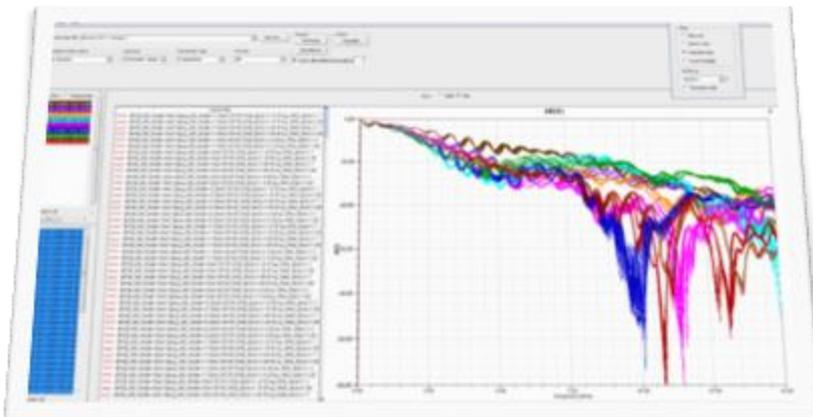
Properties

Name	Value	Unit	Evaluated Value
Name	ParametricSetup1		
Enabled	<input checked="" type="checkbox"/>		

Setup Sweep Analysis

Sweep Definitions | Table | General | Calculations | Options

Sync #	Variable	Description
	\$pkg_MS_Width	Linear Step from 1.75mil to 2.25mil, step=0.25mil
	\$Top_PKG_Etch	Single Value at 1.1
		Single Value at 1.25
	\$PCB_MS_Width	Linear Step from 4mil to 6mil, step=1mil
	\$TOP_PCB_Etch	Single Value at 1.15
		Single Value at 1.25
		Single Value at 1.4



- Automated .html reporting for partial and loop resistance/inductance
- The CPA solver is capable of producing per bump/ball resolution RLC extracted parasitics
- Visual Bar graph plotting is available for solderball/bump and Pin Groups

Flip-Chip PDN System

Solver	Net	R (mΩ)	L (nH)	C (pF)	Solve Time (minutes)	Speed Up	RAM (MB)	RAM Reduction
Q3D (TPA)	PDN A	12.3	310.6	24.8	4.51	-	748	-
CPA	PDN A	12.9	312.4	25.8	0.4	11x	210	4x
Q3D (TPA)	PDN B	9.1	224.8	24.8	4.51	-	748	-
CPA	PDN B	9.2	230.7	25.9	0.4	11x	210	4x

Solver	Net	R (mΩ)	L (pH)	C (pF)	Solve Time (Hours)	Speed Up	RAM (GB)	RAM Reduction
Q3D (TPA)	PDN C	1.58	79.2	128.4	48	-	71	-
CPA	PDN C	1.61	79.9	129.3	0.1	480x	13	5x
Q3D (TPA)	PDN D	0.16	12.6	973.4	48	-	71	-
CPA	PDN D	0.16	12.9	979.3	0.1	480x	13	5x

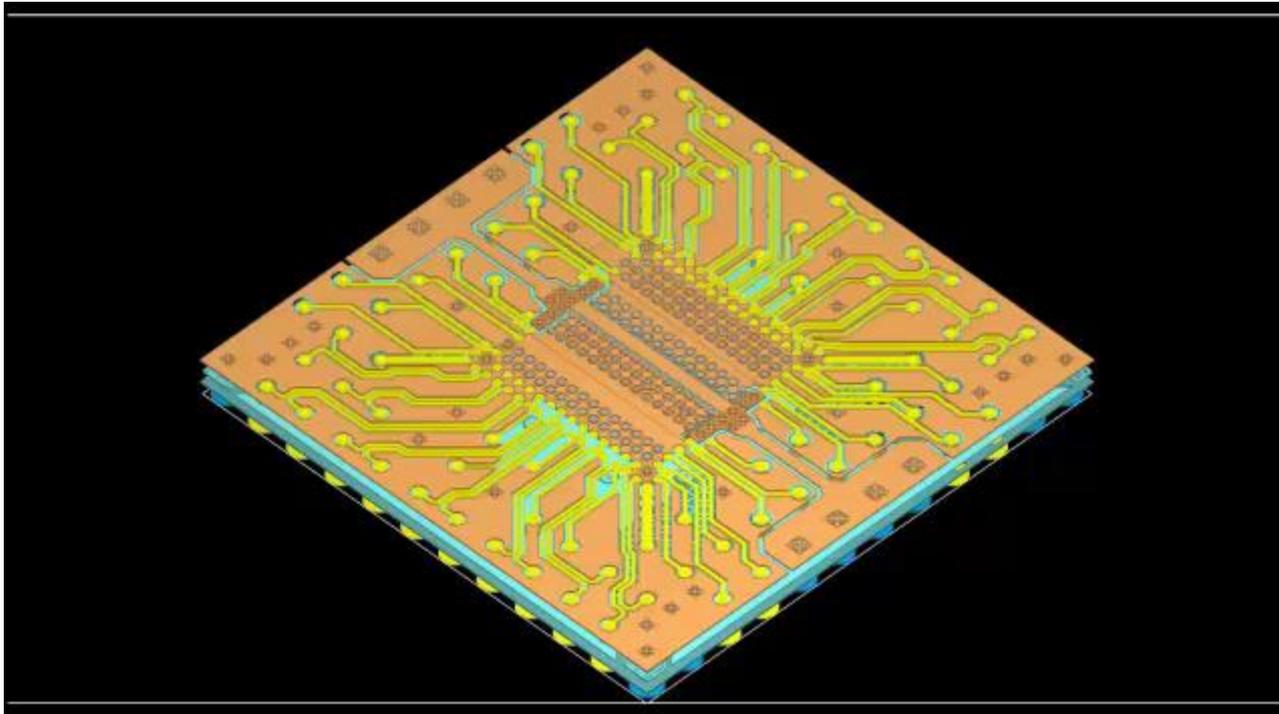
Coupled Microstrip Lines

Solver	Net	R (mΩ)	L (nH)	C (pF)	Solve Time (Minutes)	Speed Up	RAM (MB)	RAM Reduction
NPE	Trace A	386	3.42	1.17	3.0	-	450	-
CPA	Trace A	386	3.22	1.17	1.0	3x	300	3x
NPE	Trace B	386	3.44	1.19	3.0	-	450	-
CPA	Trace B	386	3.30	1.17	1.0	3x	300	3x

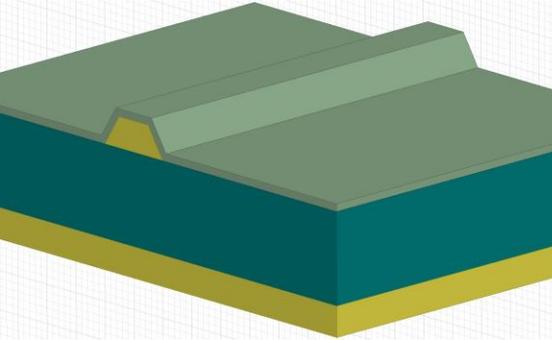
SIwave-Q3D (TPA) Improvements

Added DC Adaptive Meshing

Added the ability to use Pin Groups with Q3D (TPA) solver



Slwave Conformal Soldermasks



Layer Stackup Editor

Color	Name	Type	Thickness (mils)	Material	Conductivity (S/m)	Dielectric Fill	Dielectric constant	Loss tangent	Translucency	Elevation (mils)	Roughness (mils)
	Top_Conformal_SM	CONFORMAL COAT	1	SolderMask	0		3.1	0.035		64.5	
	top	METAL	1.1	EDB_copper	5.8E+07	SolderMask	3.1	0.035	0	63.4	HJ: 0, HJ: 0
	Dielectric_1	DIELECTRIC	4	EDB_FR4_epoxy	0		4.4	0.02		59.4	
	plane1	METAL	0.65	EDB_copper	5.8E+07	EDB_FR4_epoxy	4.4	0.02	0	58.75	HJ: 0, HJ: 0
	Dielectric_2	DIELECTRIC	52	EDB_FR4_epoxy	0		4.4	0.02		6.75	
	plane2	METAL	0.65	EDB_copper	5.8E+07	EDB_FR4_epoxy	4.4	0.02	0	6.1	HJ: 0, HJ: 0
	Dielectric_3	DIELECTRIC	4	EDB_FR4_epoxy	0		4.4	0.02		2.1	
	bottom	METAL	1.1	EDB_copper	5.8E+07	SolderMask	3.1	0.035	0	1	HJ: 0, HJ: 0
	Bottom_Conformal_SM	CONFORMAL COAT	1	SolderMask	0		3.1	0.035		0	

Add / Delete / Move Layer(s)
 Add Above Selected Layer
 Add Below Selected Layer
 Delete Selected Layers
 Move Selected Layers Up
 Move Selected Layers Down

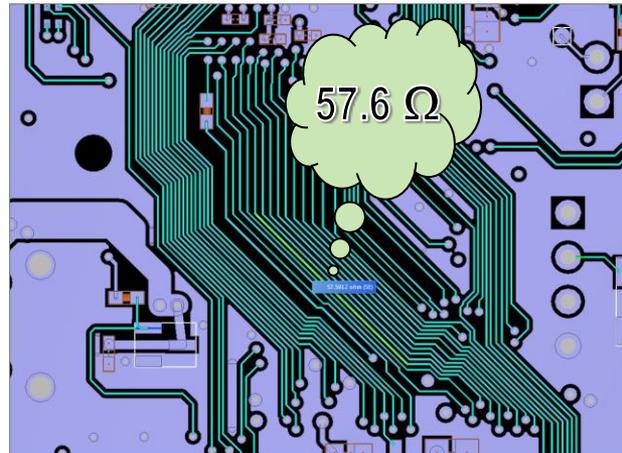
Edit Selected Layer(s)
 Color: #fb464 Update
 Name: top Update
 Type: METAL Update
 Material: EDB_copper Update
 Dielectric Fill: SolderMask Update
 Translucency: 0% Update
 Thickness: 1.1 mils Update
 Roughness: HJ: 0, HJ: 0 mils Update

Select all DIELECTRIC layers Apply Edit Material Properties Invert Stackup Conformal Coat Units mils

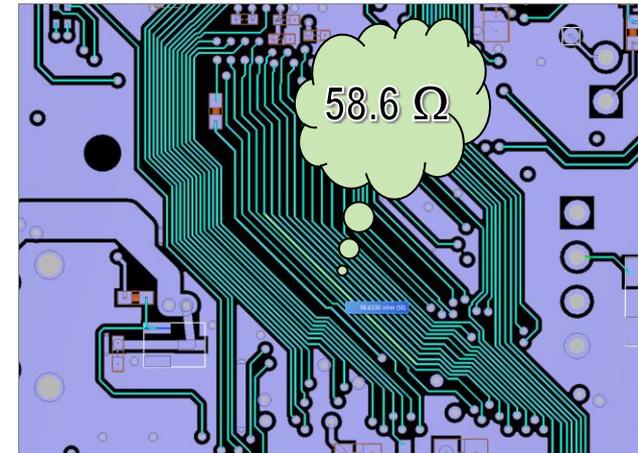
Single Ended Zo
Without Trace-Trace Coupling
Without Conformal Soldermask



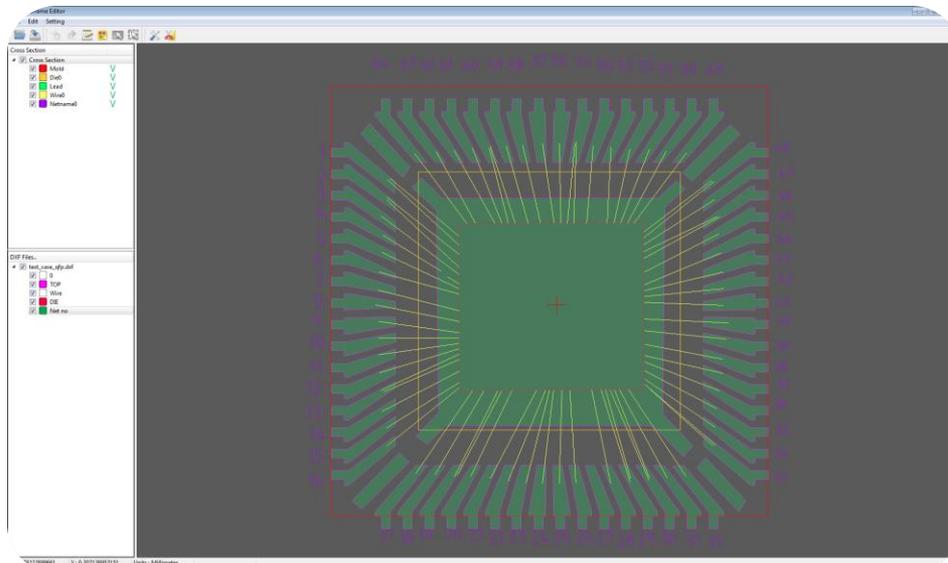
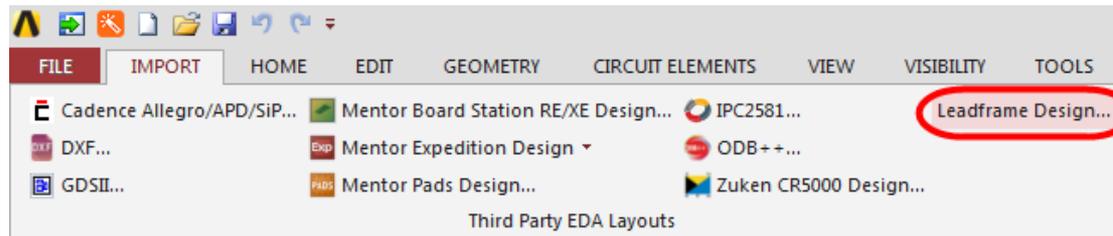
Single Ended Zo
With Trace-Trace Coupling
Without Conformal Soldermask



Single Ended Zo
With Trace-Trace Coupling
With Conformal Soldermask

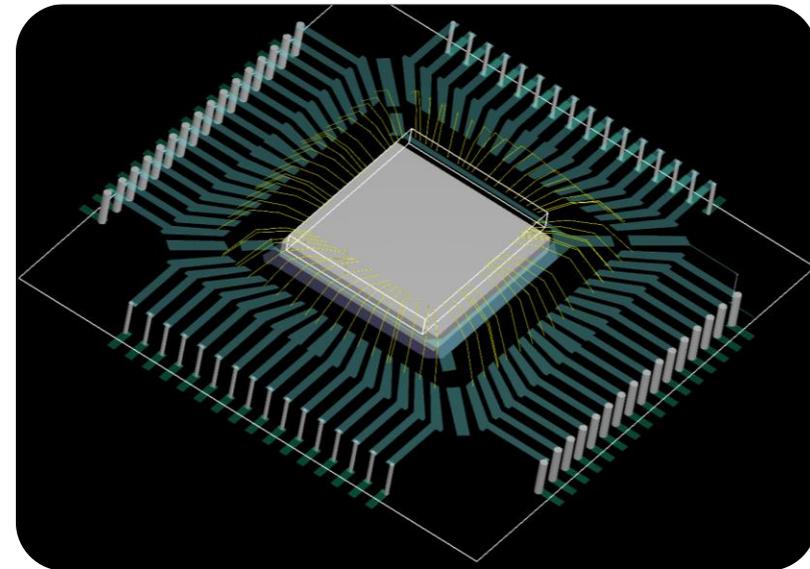


Leadframe Editor



Lead Frame Editor

- Creates Slwave & 3D Layout .anf Geometries
- Creates HFSS & Q3D .sat Geometries



Lead Frame Editor

- Slwave QFP Package from Lead Frame Editor



Thank You