

The logo for EDICON 2018, featuring the text "EDI" in black and "CON" in white on a blue background, with "2018" in red below it.

EDI  
CON

2018

Electronic Design Innovation  
Conference & Exhibition

The event date and location information, including the dates "October 17-19 2018" and the location "Santa Clara Convention Center, Santa Clara, CA".

October 17-19 2018  
Santa Clara Convention Center  
Santa Clara, CA

# Increasing Broadband Interconnect Characterization

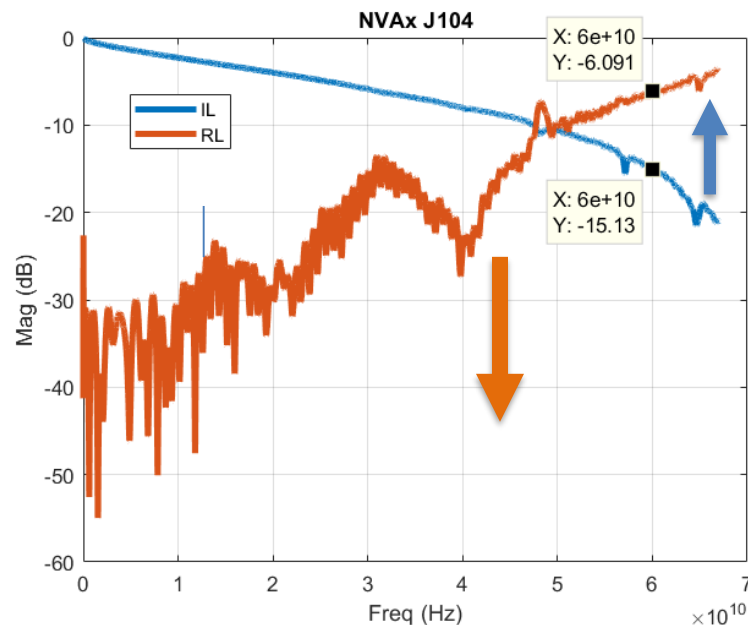
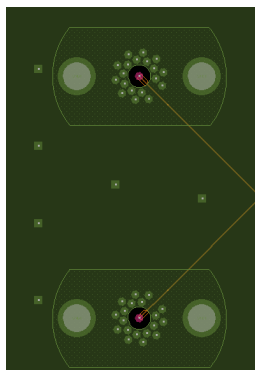
Gustavo Blando

Ted Ballou, Scott McMorro

## Calibrations

### Anatomy of the DUT

- Calibration traces consists of:
  - 2.4mm or 1.85mm connector and mating interface
  - PCB launch structure
  - Small section of single ended traces
  - Differential trace
- Higher BW calibration means:
  - Decreasing insertion loss (push up)
  - Decreasing return loss (push down)



# Topology Components

Measurements done in the time  
(TDR) and frequency (VNA) domain

**Important to establish  
equivalence between time and  
frequency domain measurements!!**

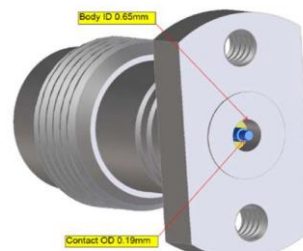
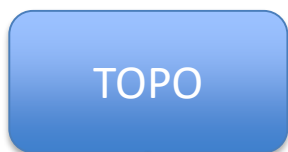
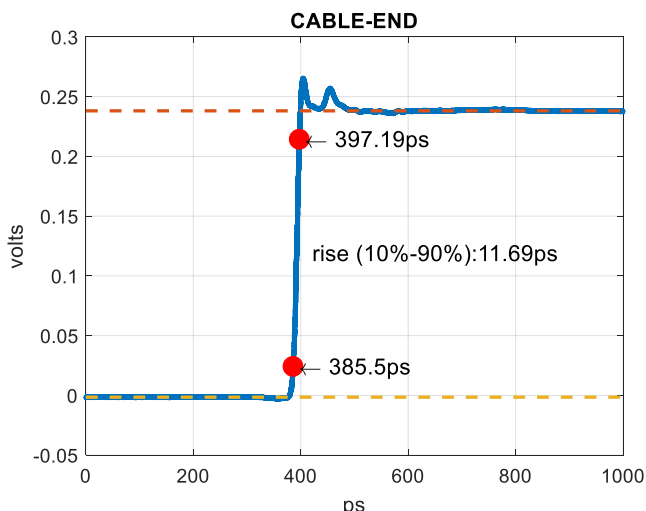
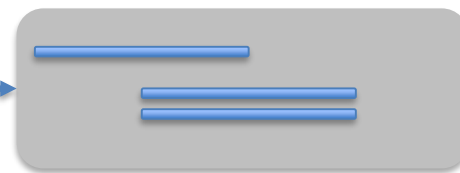
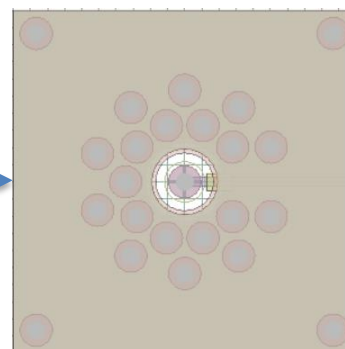


Fig. 3.4: Optimized rear dimension



We'll first study the  
coaxial connector in  
isolation

We'll then  
study  
the PCB launch  
and traces

# Coaxial Connector Preparation

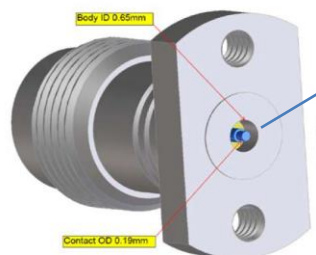
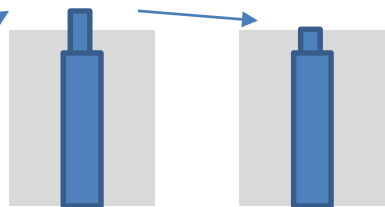


Fig. 3.4: Optimized rear dimension



DUT

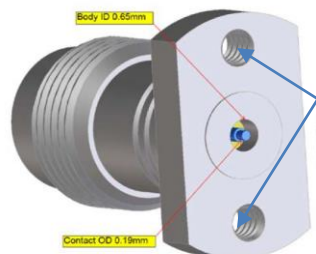
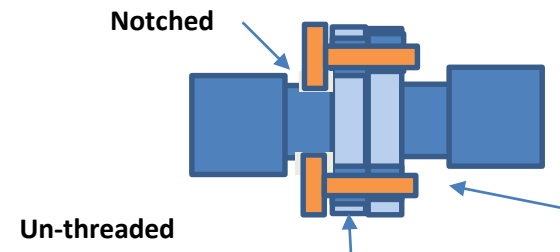
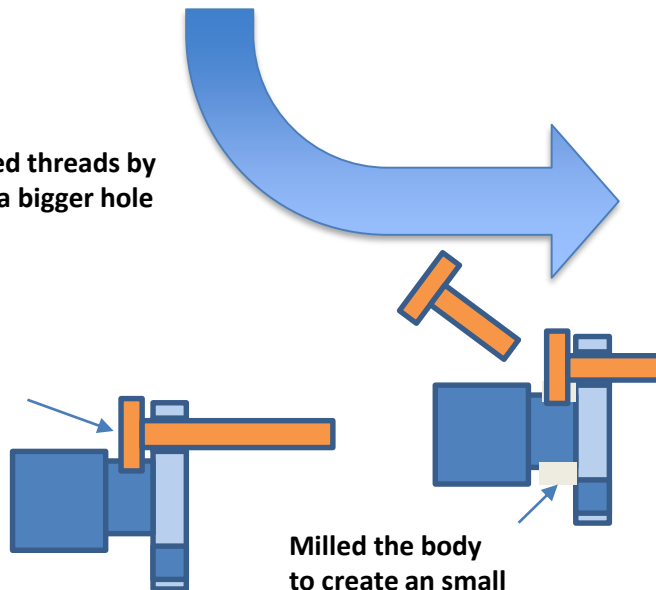


Fig. 3.4: Optimized rear dimension

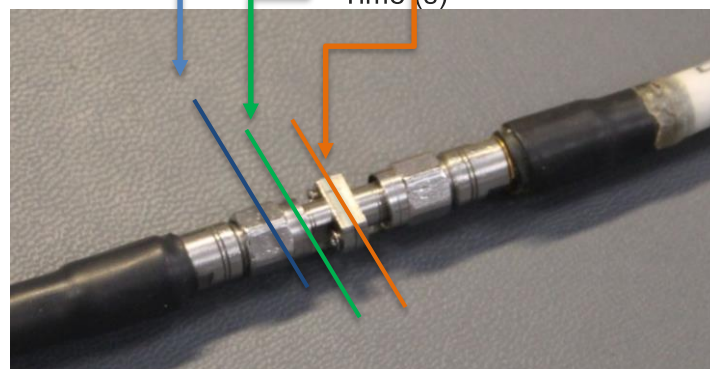
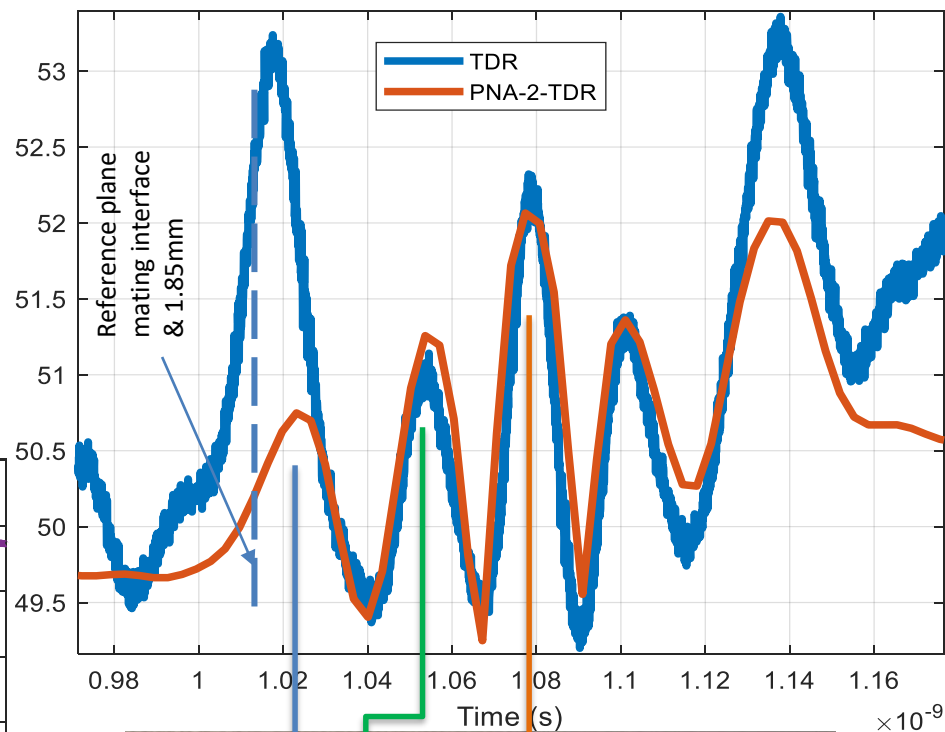
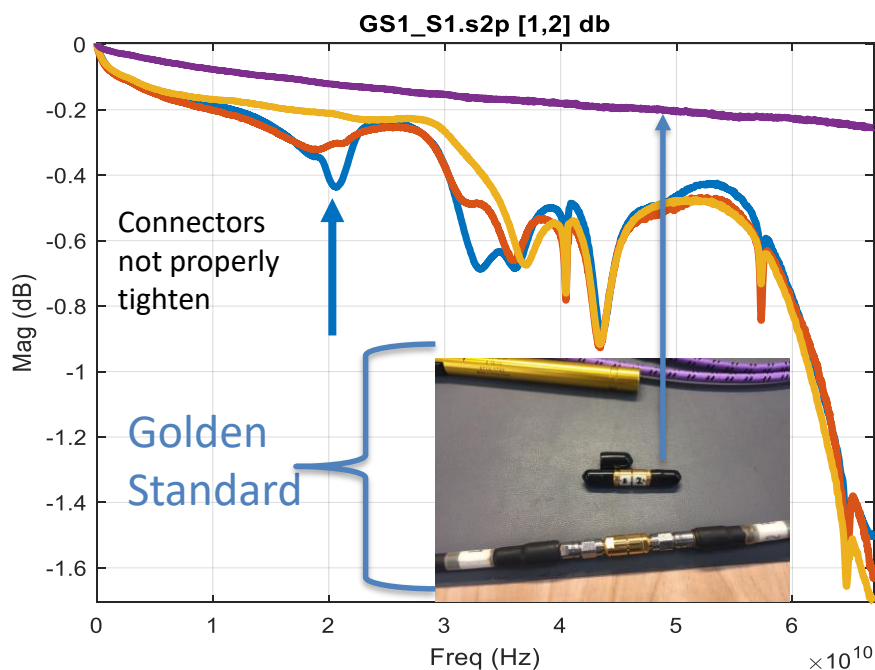
Removed threads by drilling a bigger hole





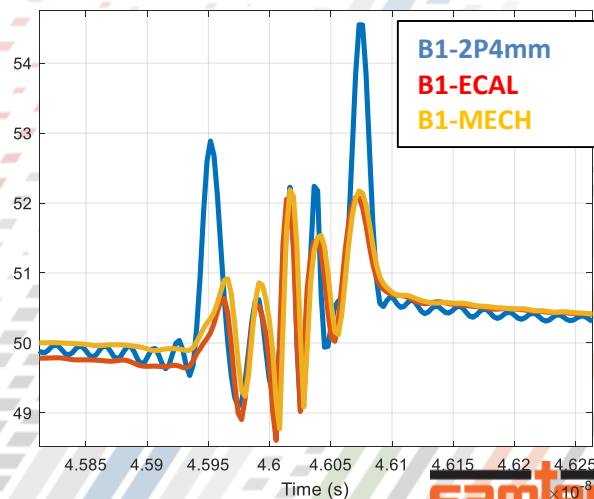
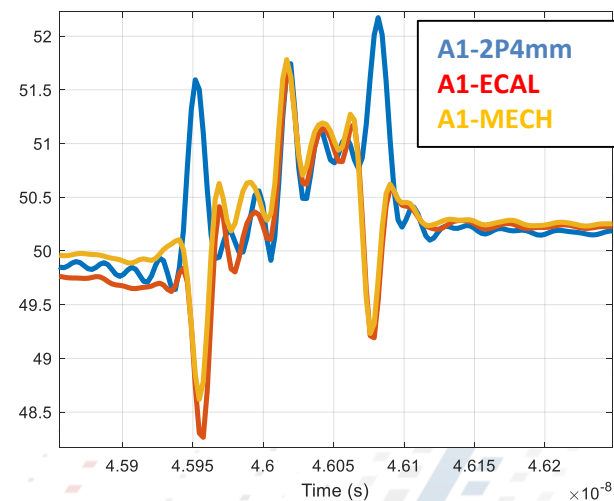
## 2.4mm Connectors back-2 back

- B2B connectors have low losses, but reflective IL as compared to the golden standard (cal piece)
- Very good correlation between measurement on TDR and VNA (**equivalence**)
- Whole mating interface present in TDR
- Partial mating interface present in VNA



## Back-2-Back 2.4mm on different mating interfaces (2 vendors)

- Measurements of 2.4mm back to back pair connected to either 1.85mm or 2.4mm terminated cables
- **Blue** case: DUT connects to a 2.4mm cable.
- **Red** and **Yellow** case: DUT connects to a 1.85mm cable
- Vendor-A1
  - Small inductive peak when connected to 2.4mm mate
  - Small capacitive dip when connected to 1.85mm mate
- Vendor-B1
  - Bigger inductive peak when connected to 2.4mm mate
  - Smaller inductive peak when connected to 1.85mm mate

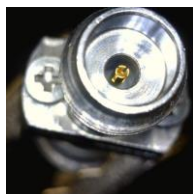


## 1.85mm vs 2.4mm

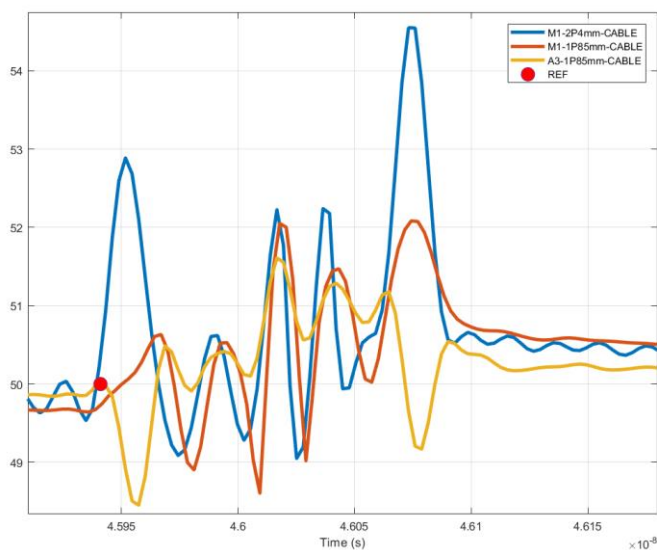
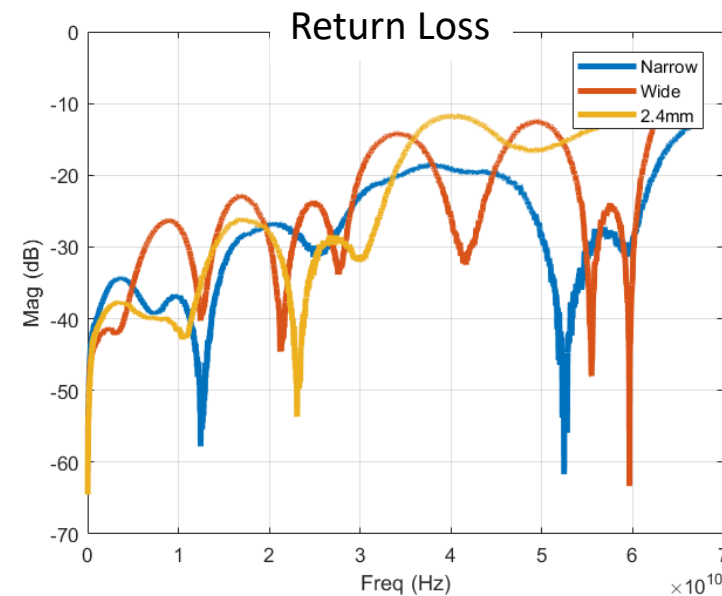
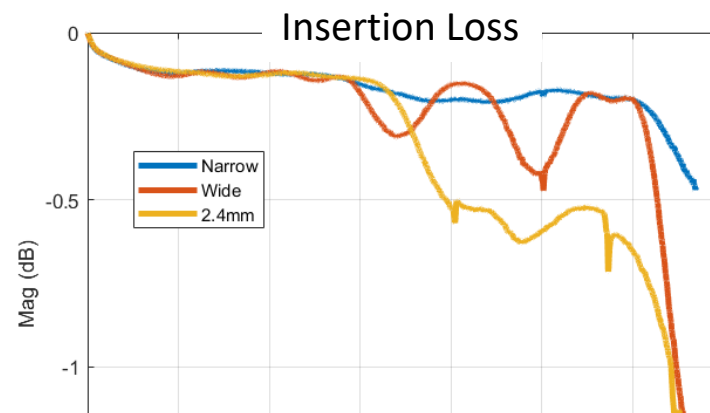
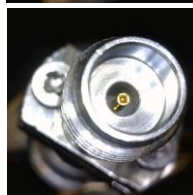
Two version of 1.85mm found in my lab: (Narrow and Wide pin)

Both 1.85mm vendors looks similar and with higher BW than 2.4mm as expected

Wide



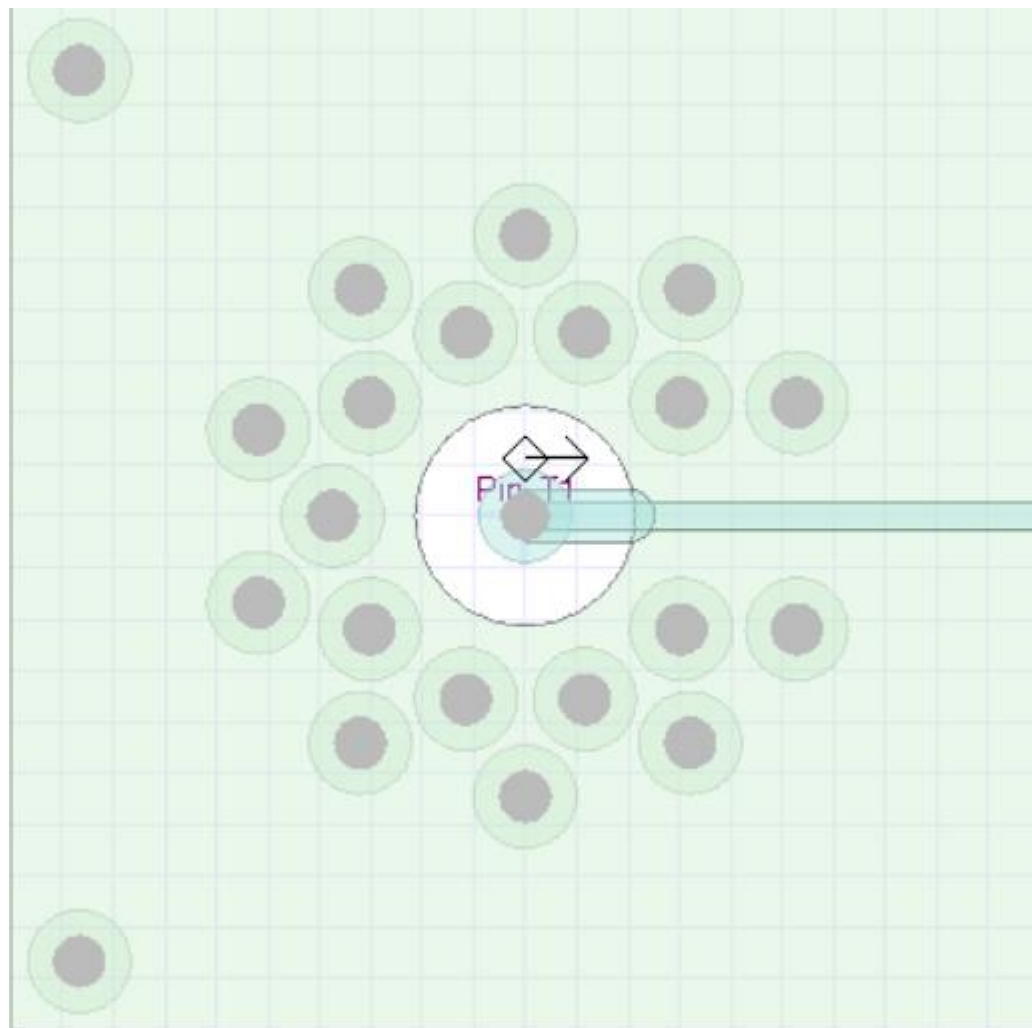
Narrow





## PCB Launch

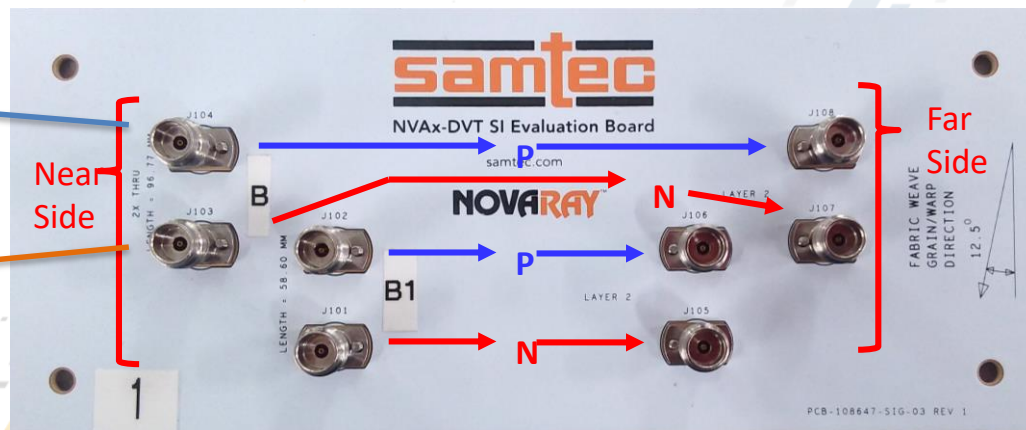
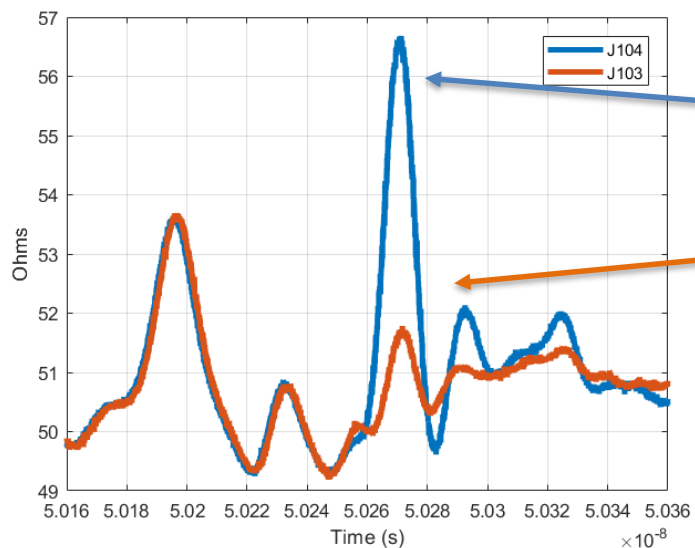
- Architected to mimic as much as possible a coax structure
  - Two concentric rings of GND vias to contain and direct the fields
  - Drill size adjustments
  - Pad and anti-pad sizes adjustments per layer
  - Exit trace width dimension adjustments
  - Design dependent on stack-up construction and exit layer





## PCB Launch Test Case

- Launch From TOP to SIG02
- *Asymmetrical Impedance Profile – ~59 ohms SE max.*
  - *P* side launch vias have a higher impedance than the *N* side



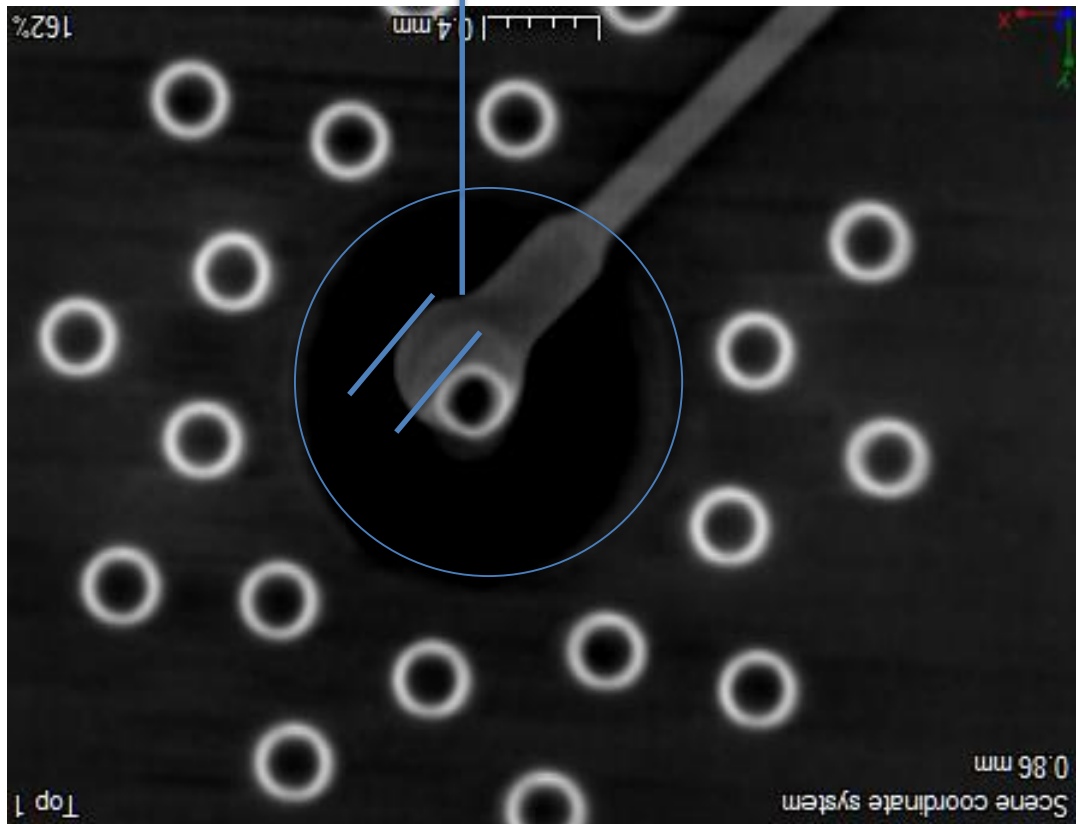
## Layer Registration

CT Scan of boards show quite a bit of TOP to SIG2 registration

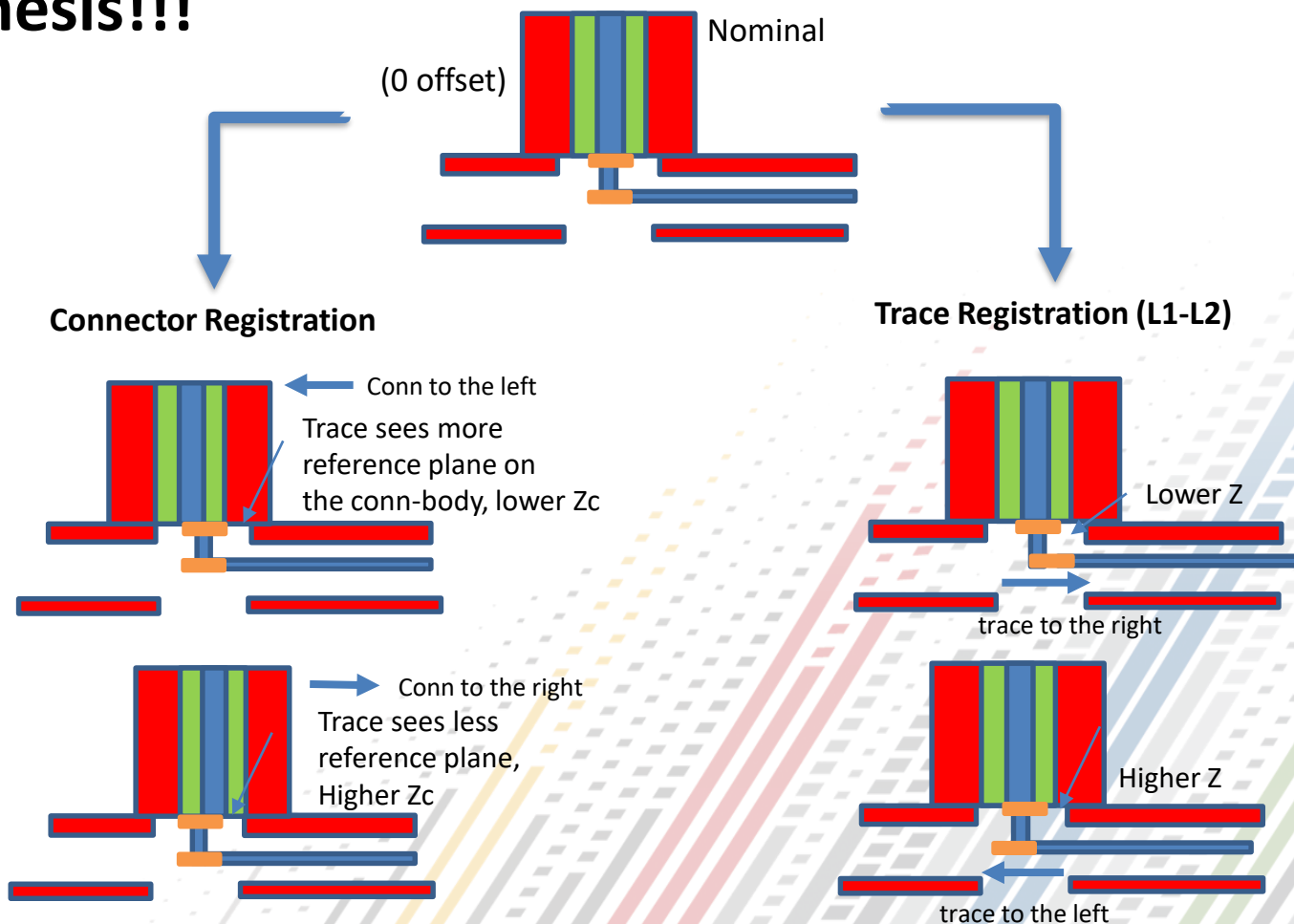


Registration  
direction

- 3.5mils ← (more than expected)



## Hypothesis!!!

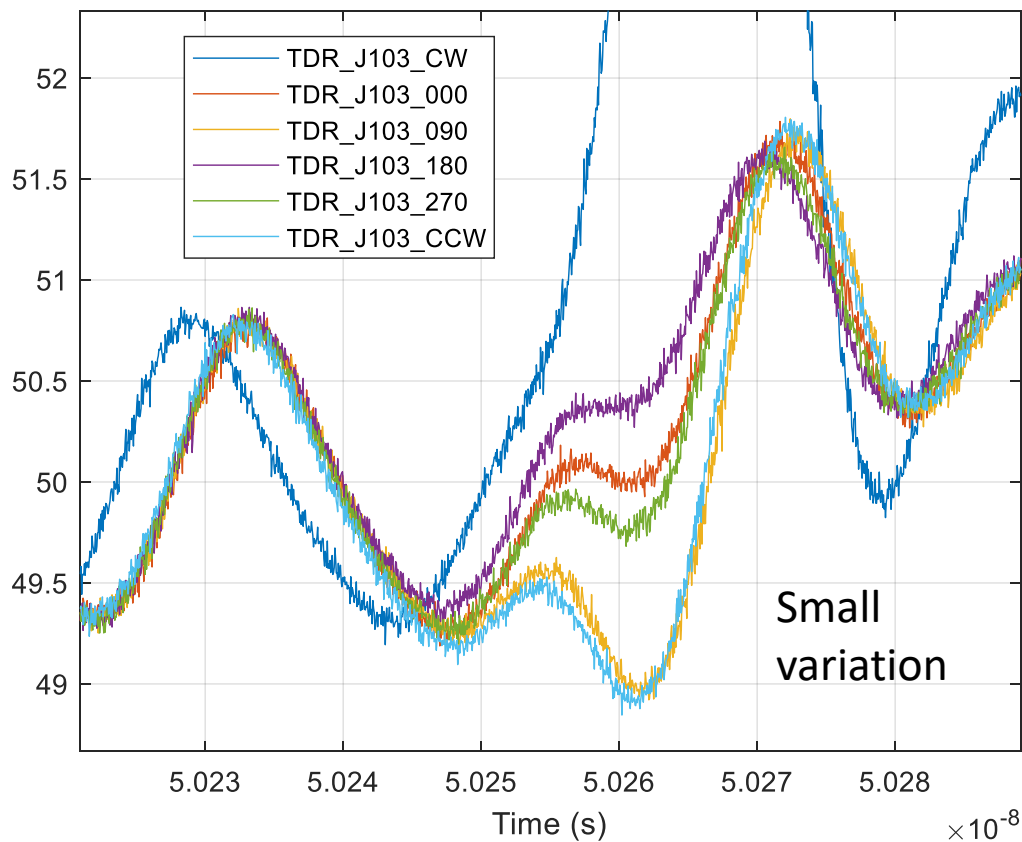


# Connector Registration

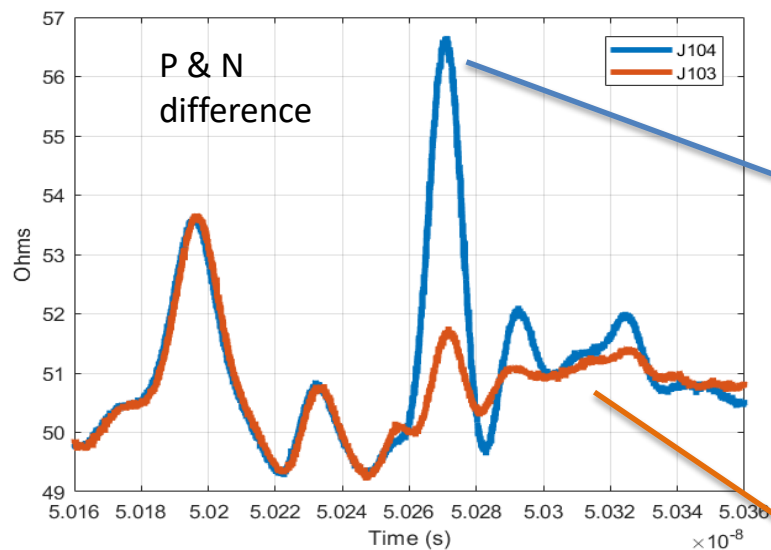
Opened the mounting holes and offset the connector as much as possible in all directions.



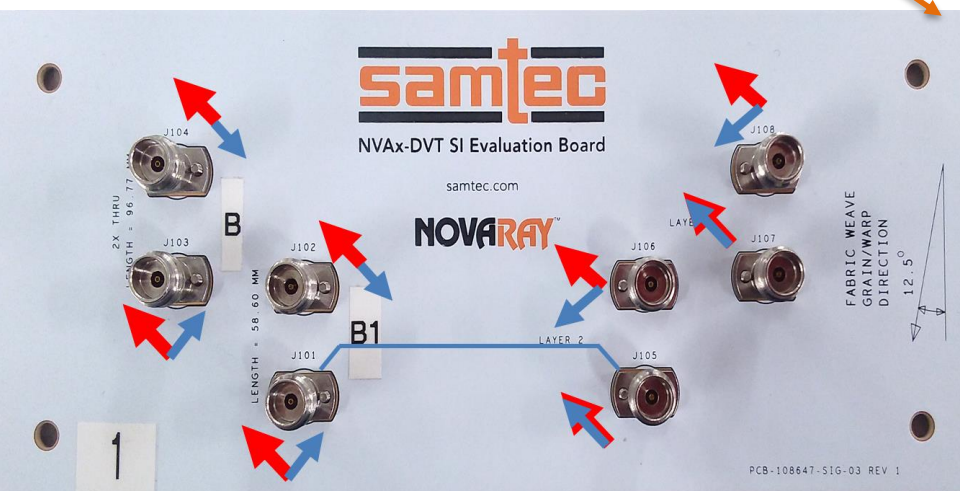
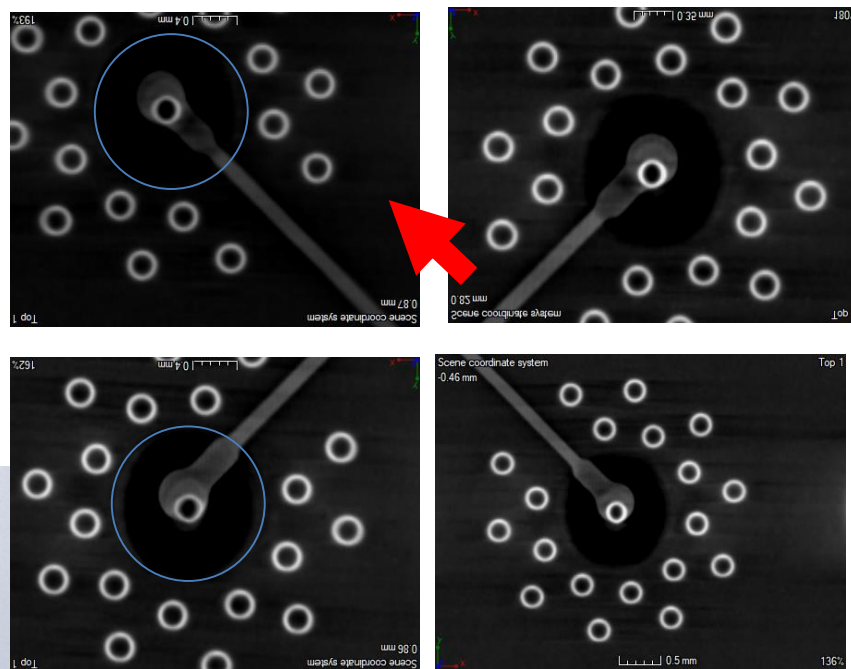
TDR J103







## Layer Registration

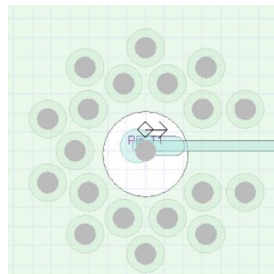
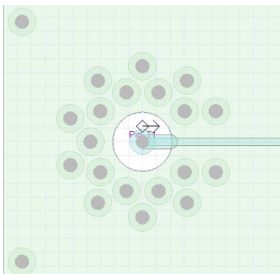
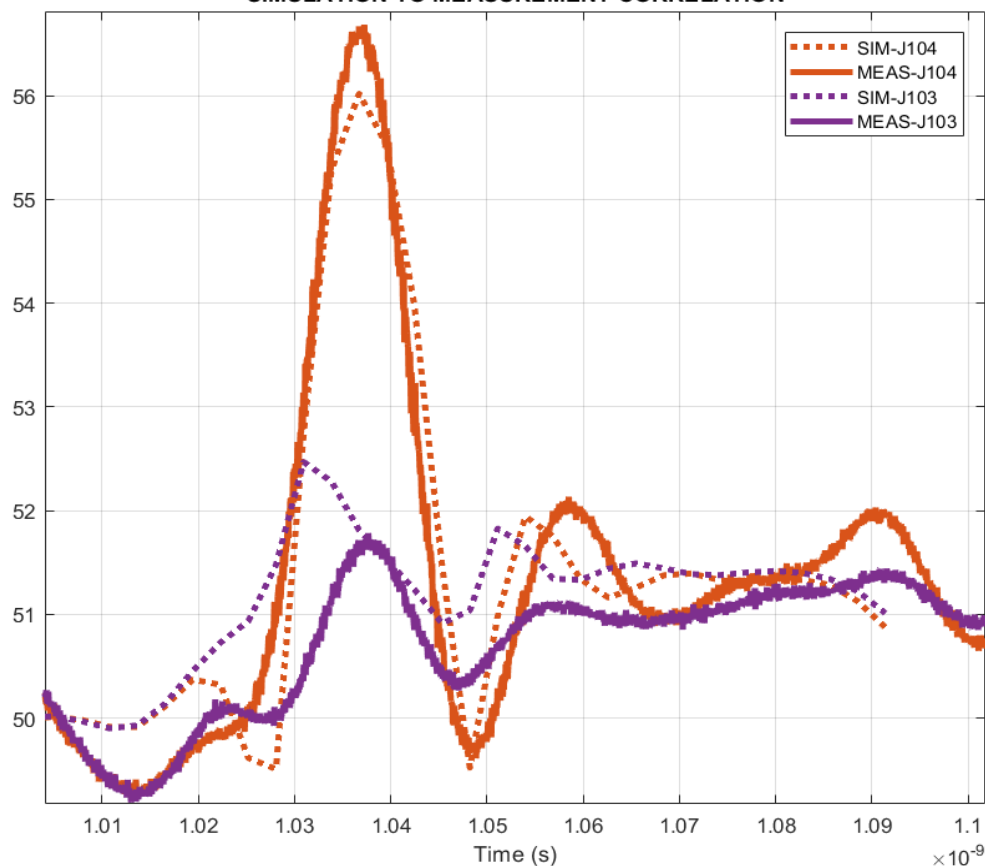


- In cases of misregistration perpendicular to the exit trace, we would expect relatively small impedance effects
- The main impact is from miss registration along the axis of the launch trace exit

# Modeling to Measurement Correlation

- Feature sizes adjusted per CT Scan
- Layer registration offsets per CT Scan
- Sim TDR rise time adjusted to match measurement rise time
- **Impedance bimodality confirmed**

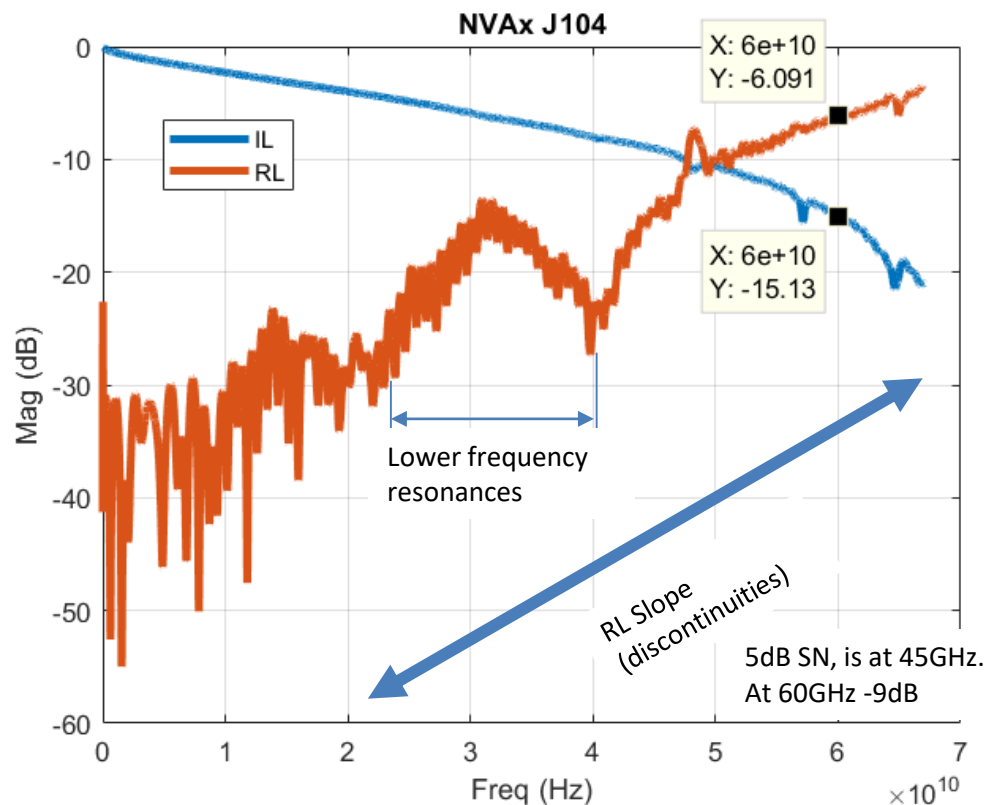
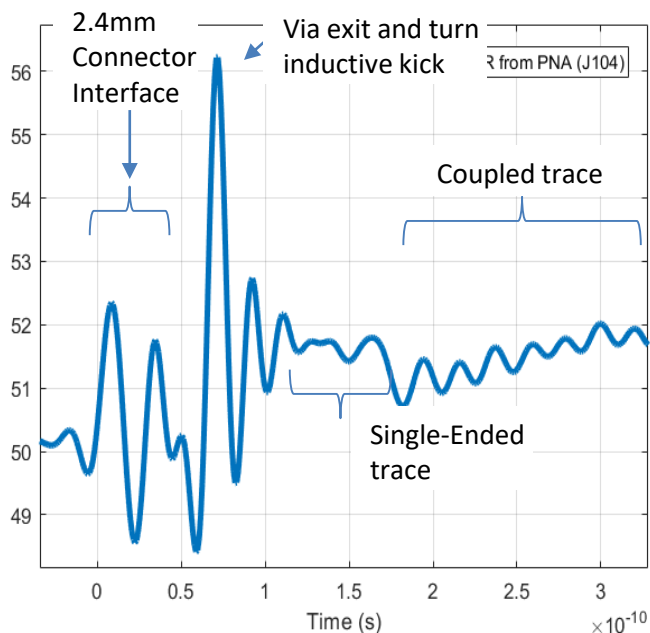
SIMULATION TO MEASUREMENT CORRELATION



# Figure of Merit Definition

## Application dependent

For our calibrations we'll define a figure of merit of 5dB  
( $IL - RL \geq 5\text{dB}$ )





# Launch Anatomy

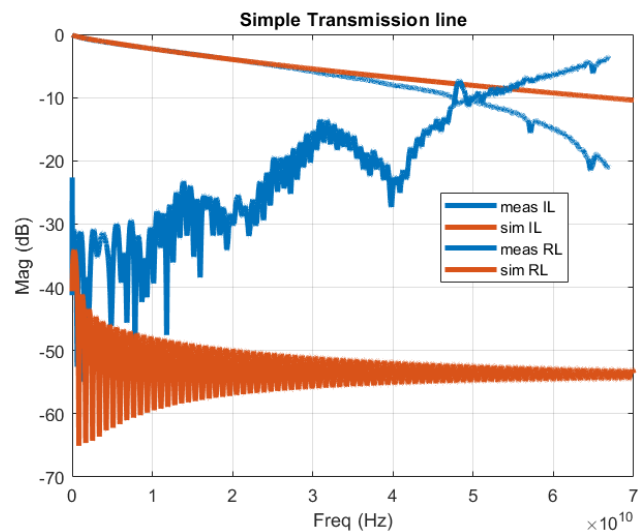
## Discontinuity Impact

- Mathematical model developed to understand (**gut feel!!**) launch discontinuity effects
- With a mathematical model we can:
  - Understand launch behaviors
  - Sensitivity analysis
  - What if scenarios

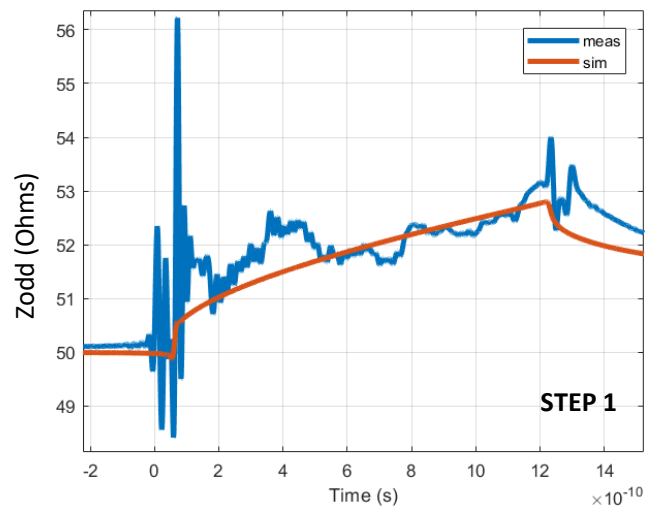


$Z_c=50.5\text{Ohms}$ ,  $99.7\text{mm}$ ,  
 $t_{\text{and}}=0.004$ ,  $dk=3.2$ ,  $w=5.5\text{mils}$

Frequency  
Domain

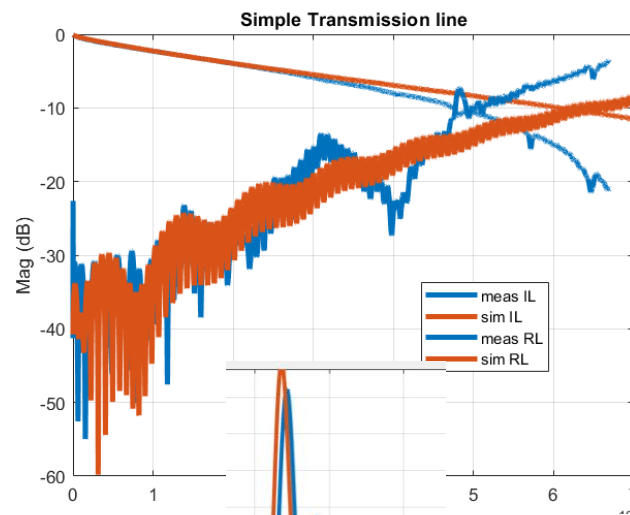
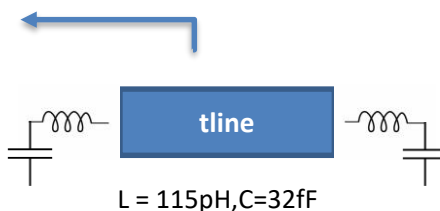
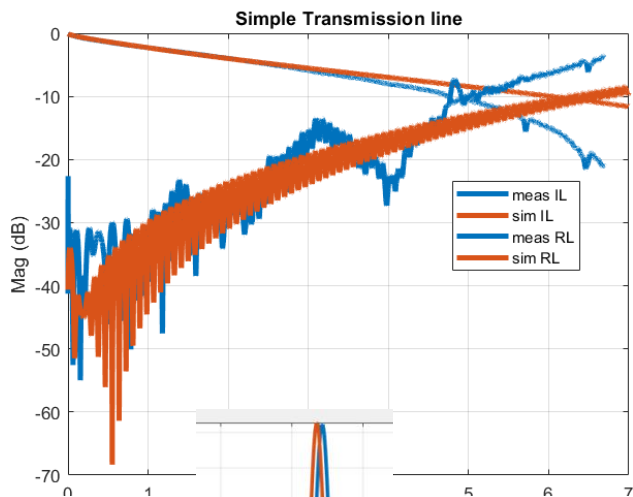


Time  
Domain

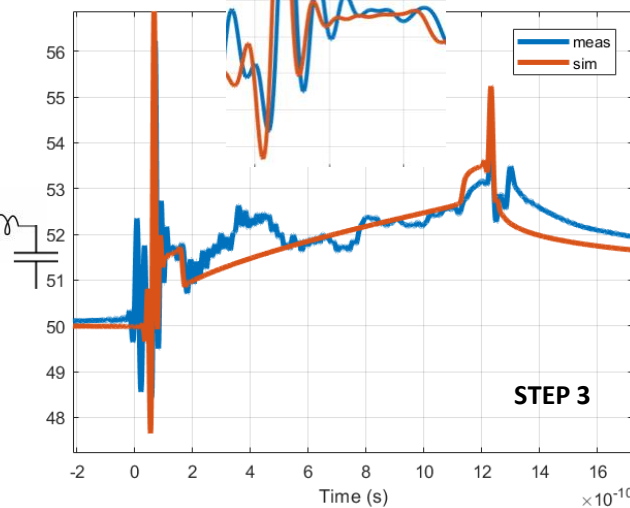
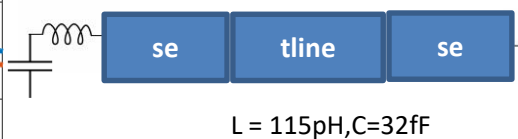
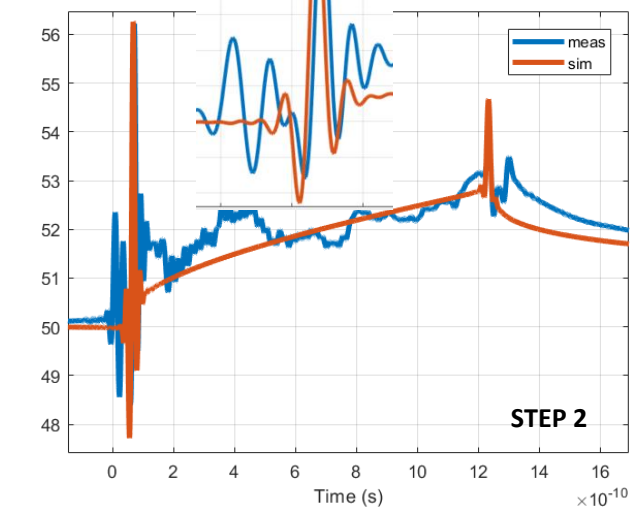




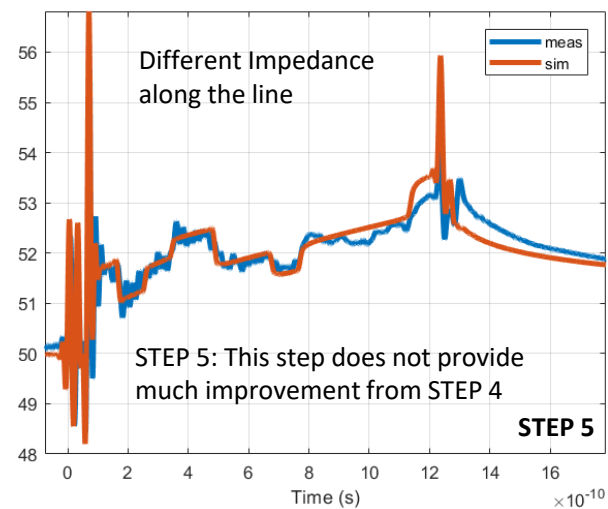
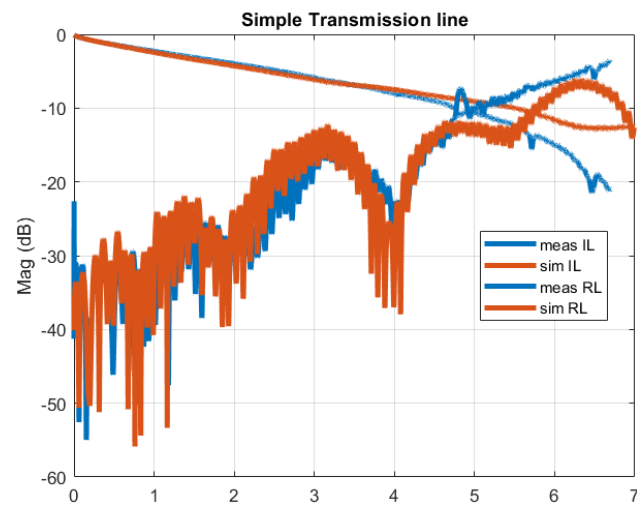
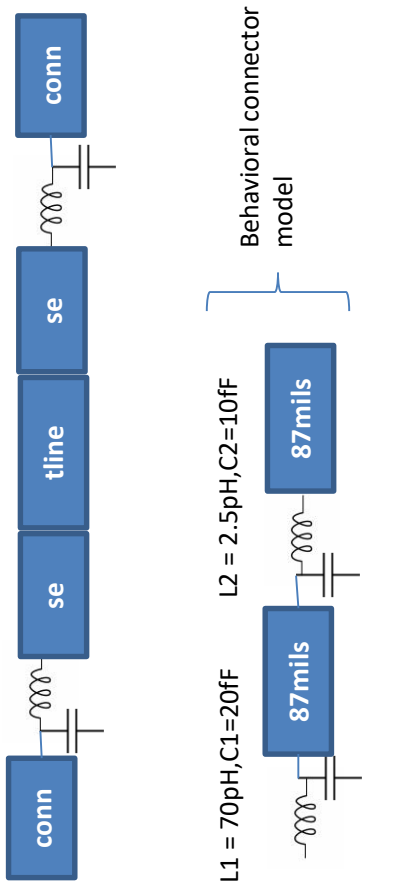
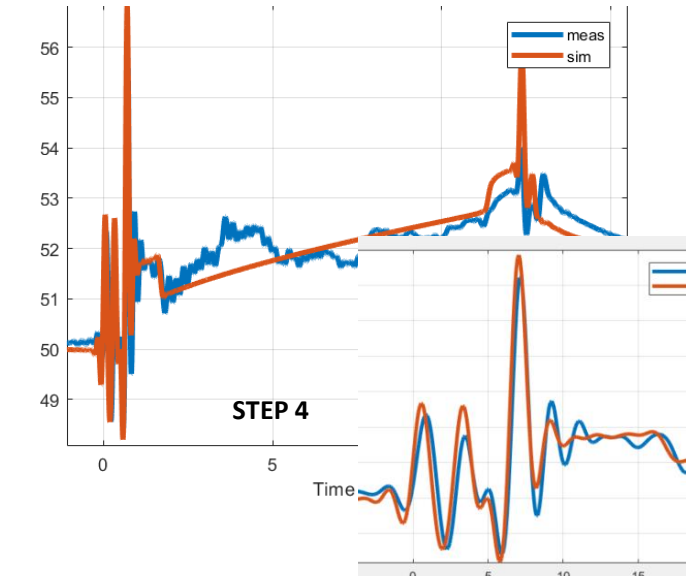
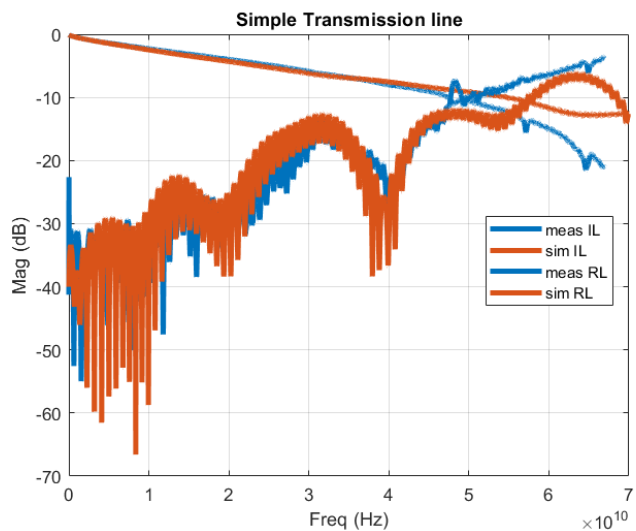
## Launch Anatomy (2)



Remarkable how very simple models allows us to match very closely a complex physical structure



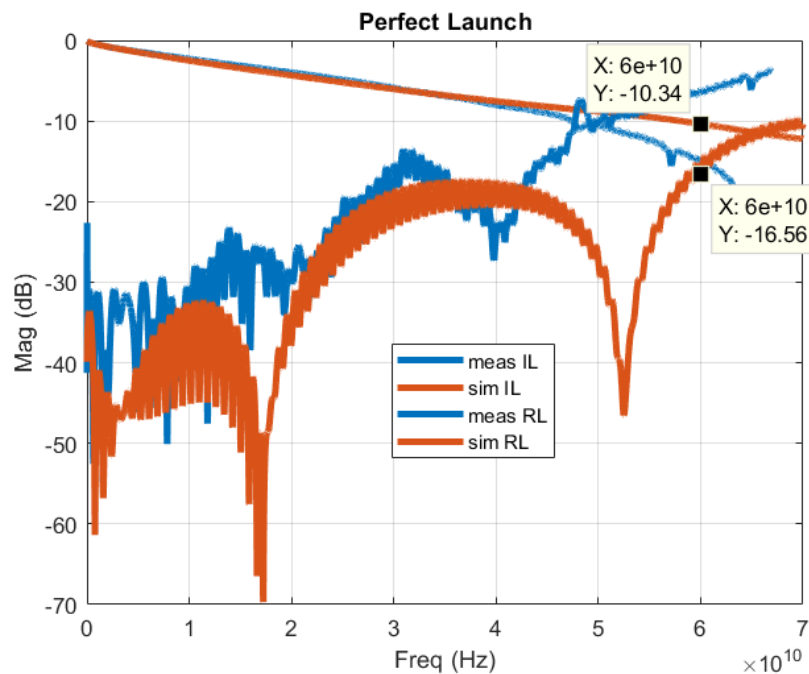
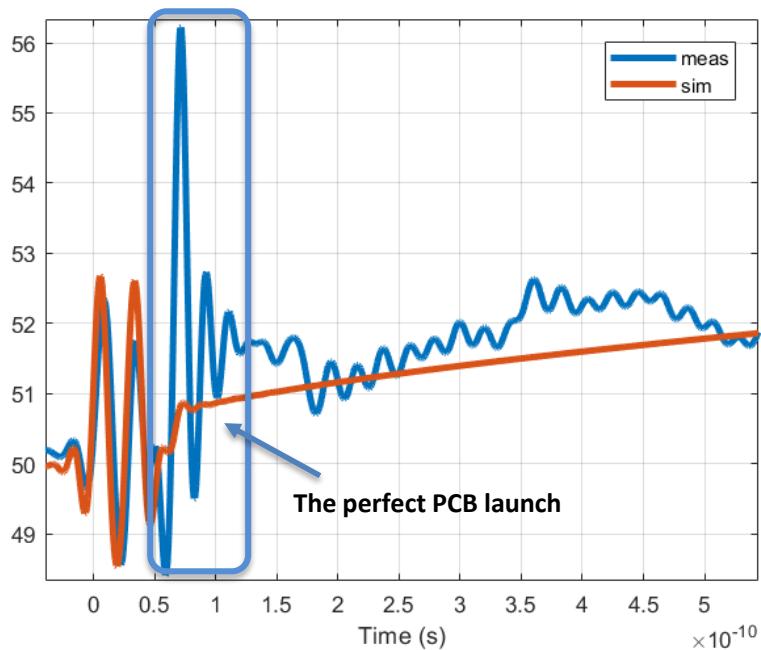
## Launch Anatomy (2)



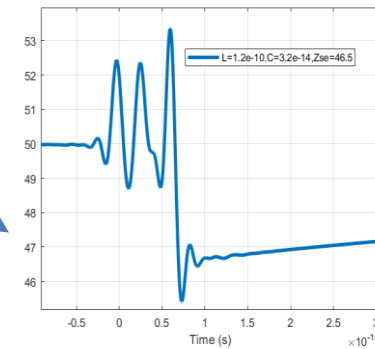
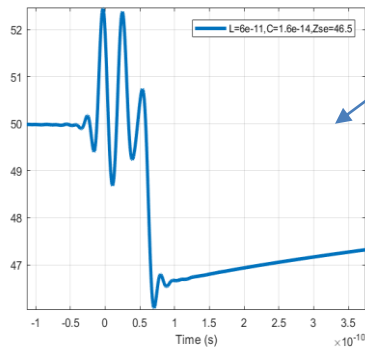
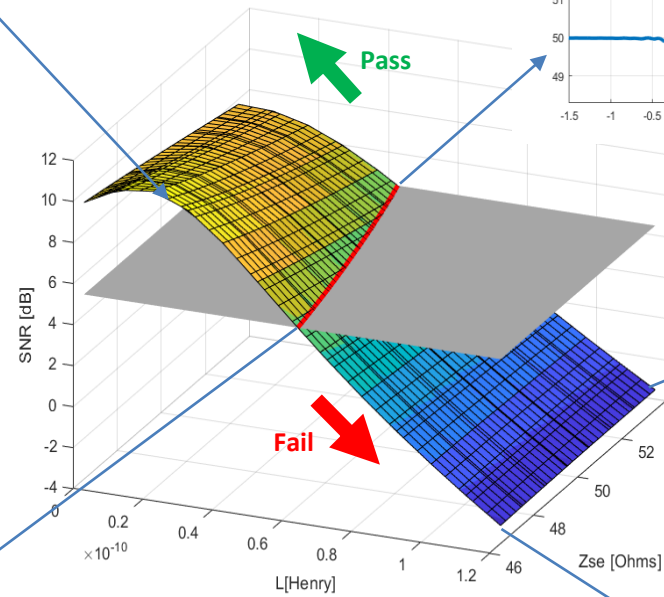
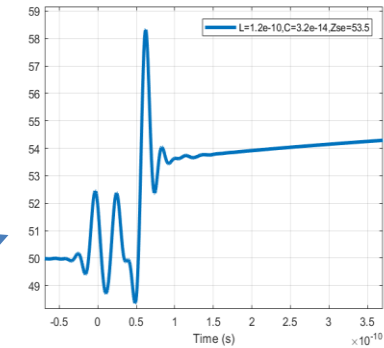
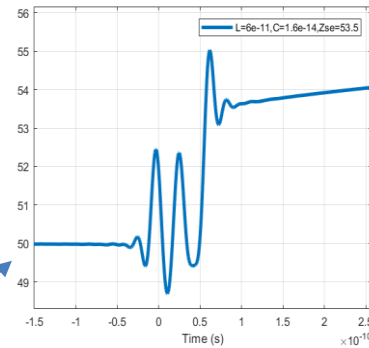
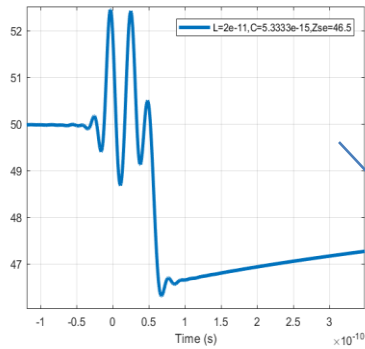
STEP 5: This step does not provide much improvement from STEP 4

# Connector Only Impact

- Even with a perfect launch we achieve only 6.22dB & only 1.22dB of margin



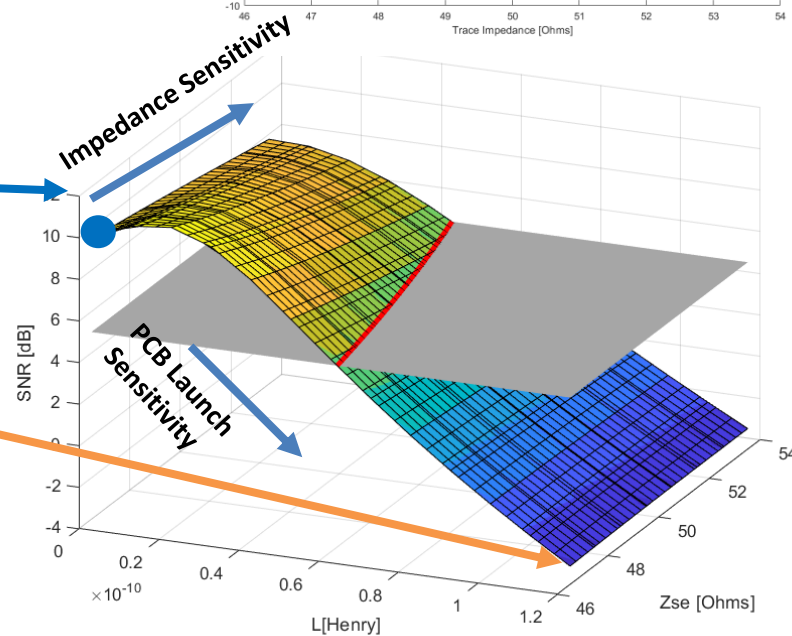
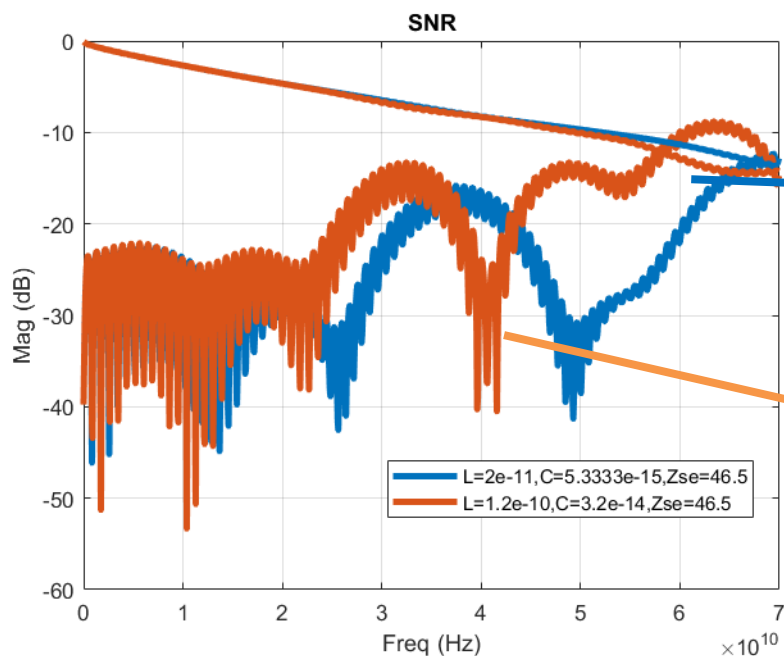
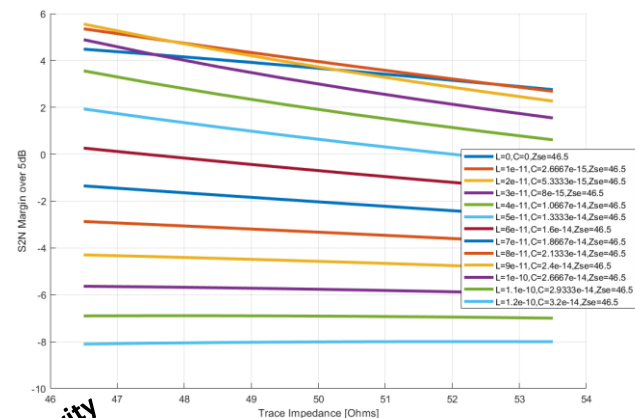
## Launch Sweeps





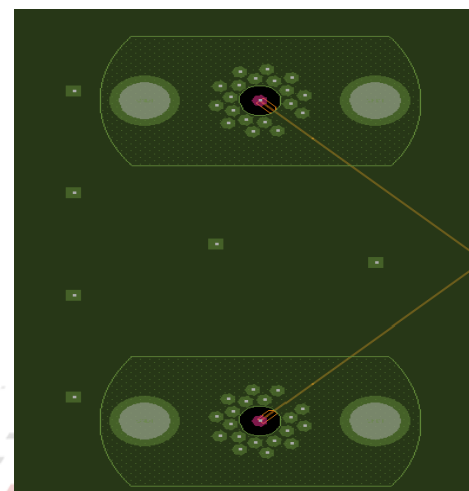
## 5dB Sensitivity

- The best the launch, the higher the impedance sensitivity
- Higher  $\frac{1}{2}$  resonance, better margin *why?*



# Typical SMA Launch routing implementation

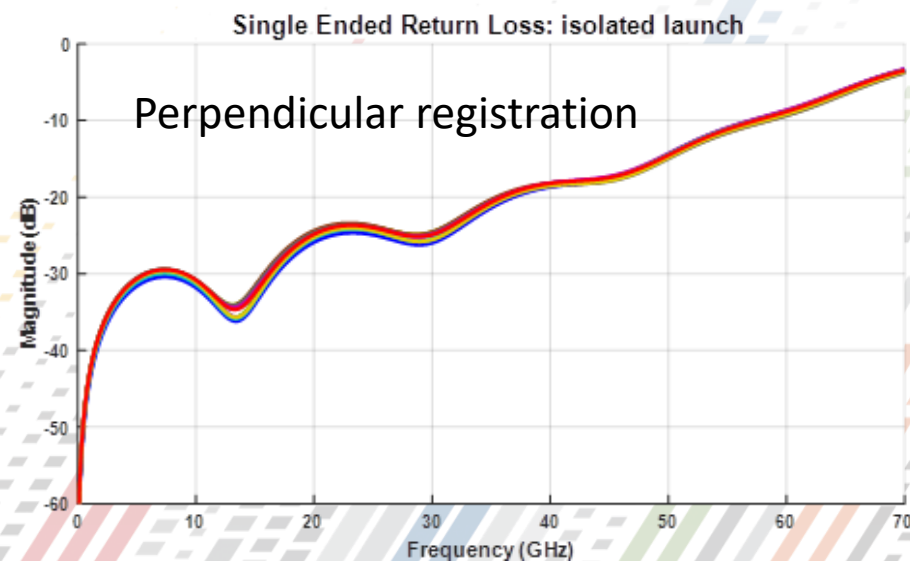
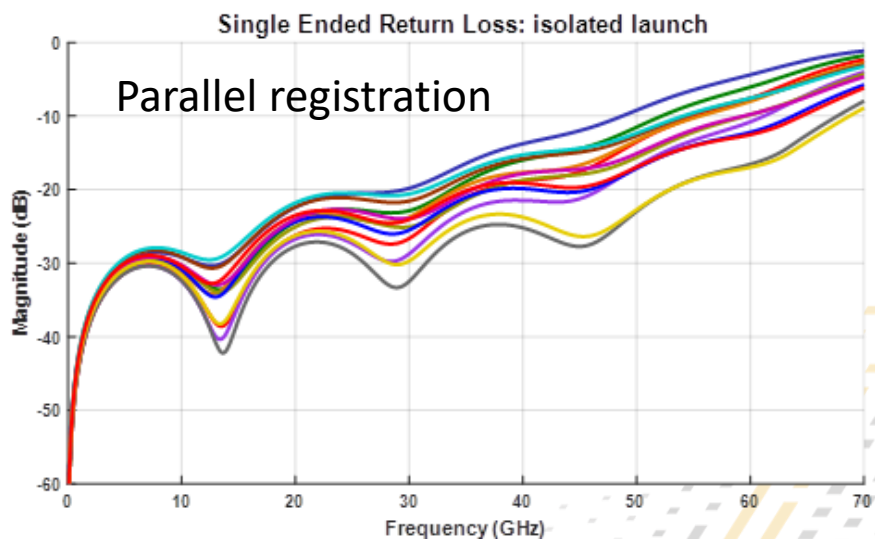
- One launch is 90 degrees rotated from the other
- Layer misregistration and drill placement tolerances are directional
- What affects the X-axis for P-launch is impacting the Y-axis for the N-launch
- X/Y impacts are not the same!
- This is the key SI issue for the L1 → L2 SMA launch



# Impact of fab tolerances

## Return loss variation

Big difference when registration aligns with the trace exit

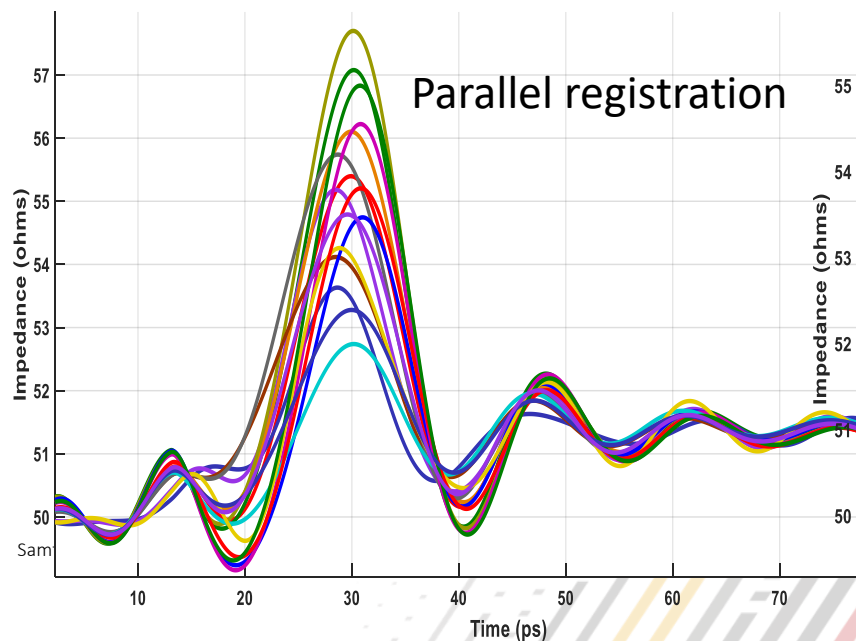


# Impact of fab tolerances

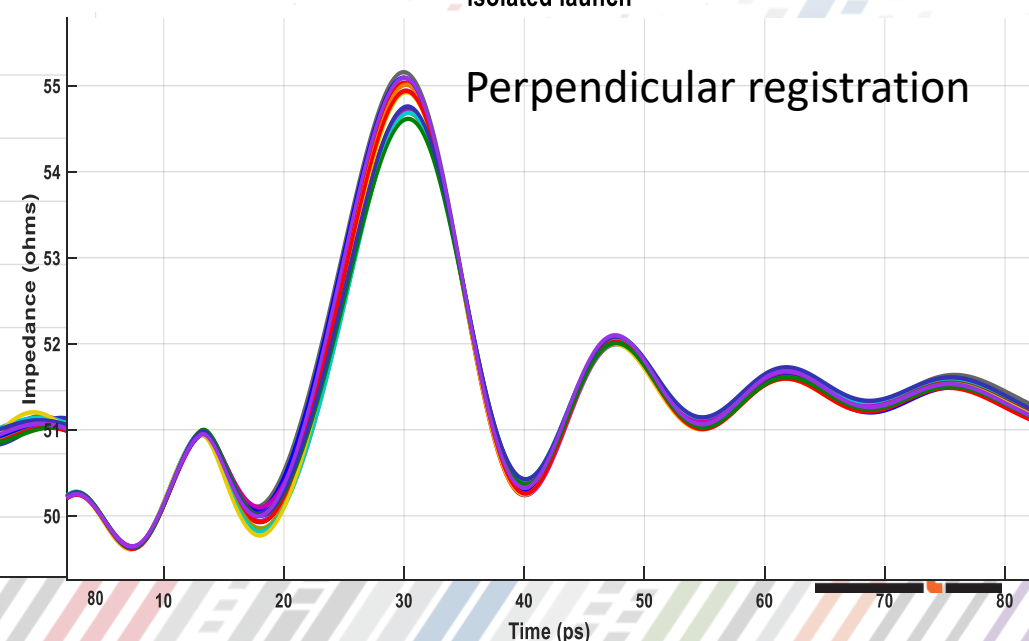
## TDR Variations

TDR impacts broken out between the P and N launch orientations

Single Ended TDR: isolated launch  
Trise = 13 ps [0 to 100%]  
isolated launch



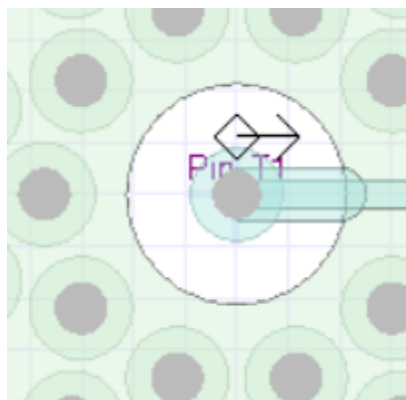
Single Ended TDR: isolated launch  
Trise = 13 ps [0 to 100%]  
isolated launch





# PCB Launch Design Improvements

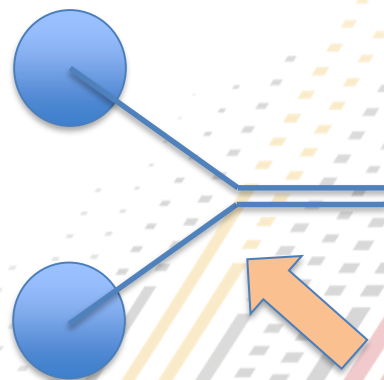
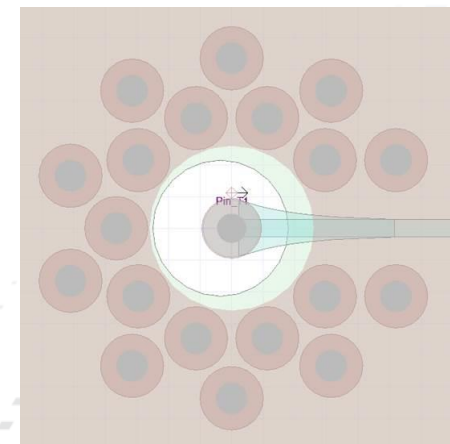
- Ideas to improve registration sensitivities and asymmetries
- There are other parameters that can be tweaked to improve on sensitivities



Reduces registration sensitivity



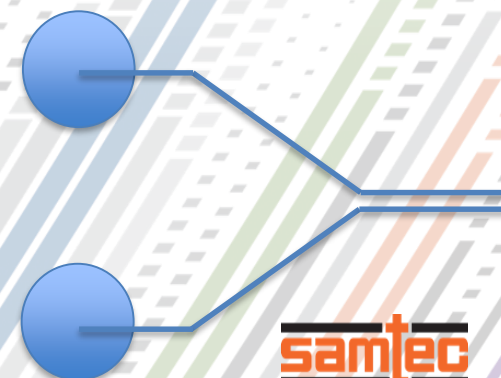
Offset anti-pad, exponential taper



Minimize launch asymmetry

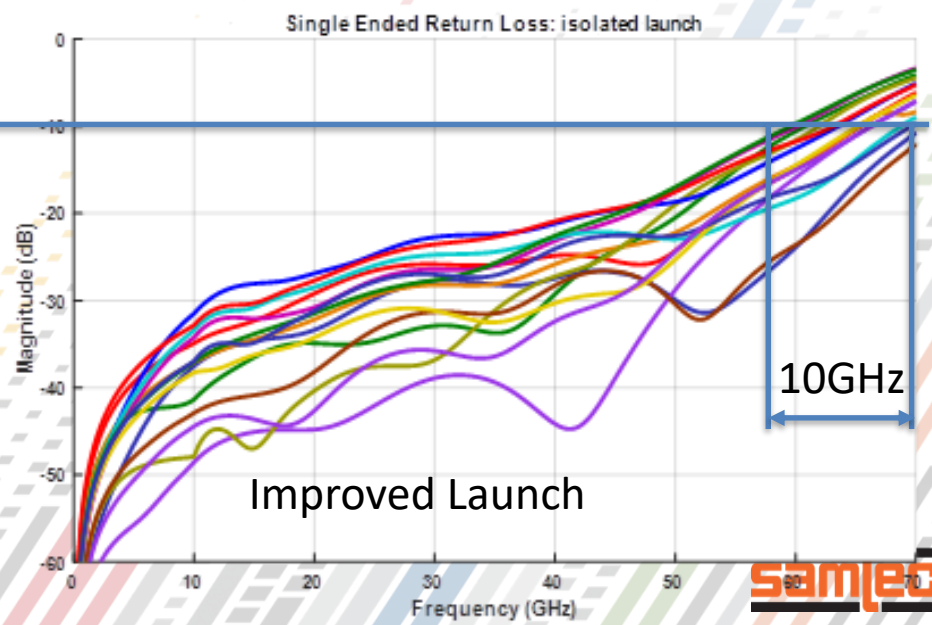
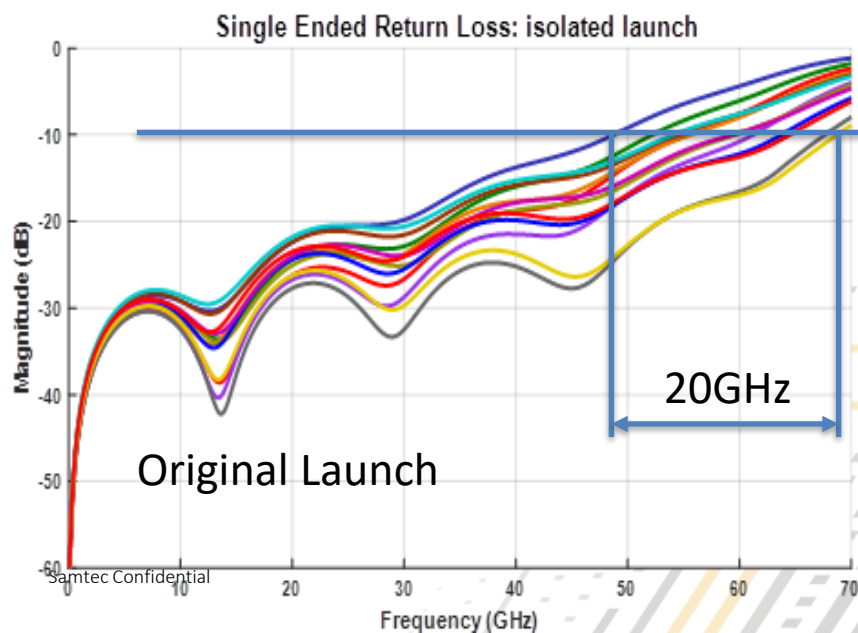


Layer registration direction



## Comparison of the OLD AND NEW

- Put TDR and RL comparison between both implementation (New and OLD)



# Conclusions

- Weak sensitivity to impedance, but high sensitivity for discontinuities at the end, **(important to keep a clean launch)**
- 2.4mm connectors produce resonances that rises the S11, leaving only a few dB of margin for the PCB launch, *1.85mm connectors would help*
- Connector movement with respect to TOP landing pad has an small effect on the launch
- High manufacturing layer registration have a high impact above 40GHz
- Look to design with registration in mind, apply methods that minimize launch sensitivity

