IBIS-AMI Generation

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KEYSIGHT TECHNOLOGIES

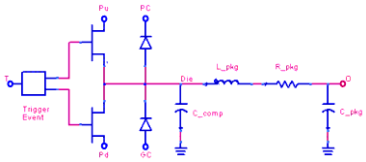
Agenda

- Background
- AMI Model Generation Barriers
- Automated AMI Model-generation flow
- Benefits of Automated AMI flow
- IBIS-AMI model ADS
- PAM 4 applications at 28 and 56 GB/s (DesignCon 2015)

Why You Can't Use SPICE For Multigigabit/s SERDES

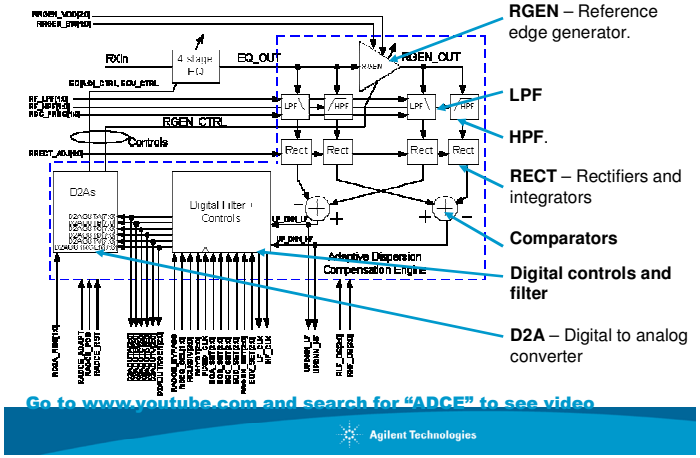
- Circuitry is too complex
- 10's k transistors in the Design space is too big
  - Tx settings × Channel design × Rx setting
    = Thousands of simulations
  - ic block

Sub-gigabit/s yesterday



Multigigabit/s today

Altera's Adaptive Equalizer



Source: Altera/Agilent joint webcast

IBIS: Input/output Buffer Information Specification

- IBIS Open Forum is an organization developing industry standards
  - http://www.eda-stds.org/ibis/
- IBIS 5.0 ratified August 2008 adds an Algorithmic Modeling Interface (AMI) flow as an alternate to the traditional flow

IBIS Open Forum Minutes

Meeting Date: **February 3, 2011**
Meeting Location: **DesignCon IBIS Summit, Santa Clara, CA, USA**

VOTING MEMBERS AND 2011 PARTICIPANTS

Agilent	Radek Biernacki*, Fangyi Rao*
AMD	(Nam Nguyen)

- Keysight supports IBIS:
  - Two Keysight engineers serve on IBIS Open Forum
  - SystemVue AMI Modeling Kit for AMI model builders (typically IC vendors)
  - Channel Simulator in ADS Transient Convolution for model users (typically OEMs)

What Does IBIS AMI Flow Offer?

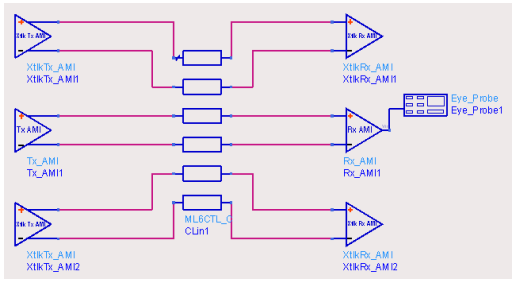
- **Portability & IP Protection**: One IC model runs in many EDA tools, without the need for non-portable, proprietary encryption keys
- **Interoperability**: IC Vendor A←→IC Vendor B
- **Performance**: Ultralow BER contours in seconds not days
- **Flexibility**:
  - Simulator has statistical and bit-by-bit ("time domain") modes
  - Models can have LTI and/or NLTV algorithms
  - IC vendor can expose arbitrary model-parameters

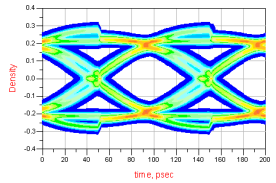
Optimization: Simulator can sweep model-specific parameter quickly

KEYSIGHT TECHNOLOGIES

…OK, But What's the Catch?

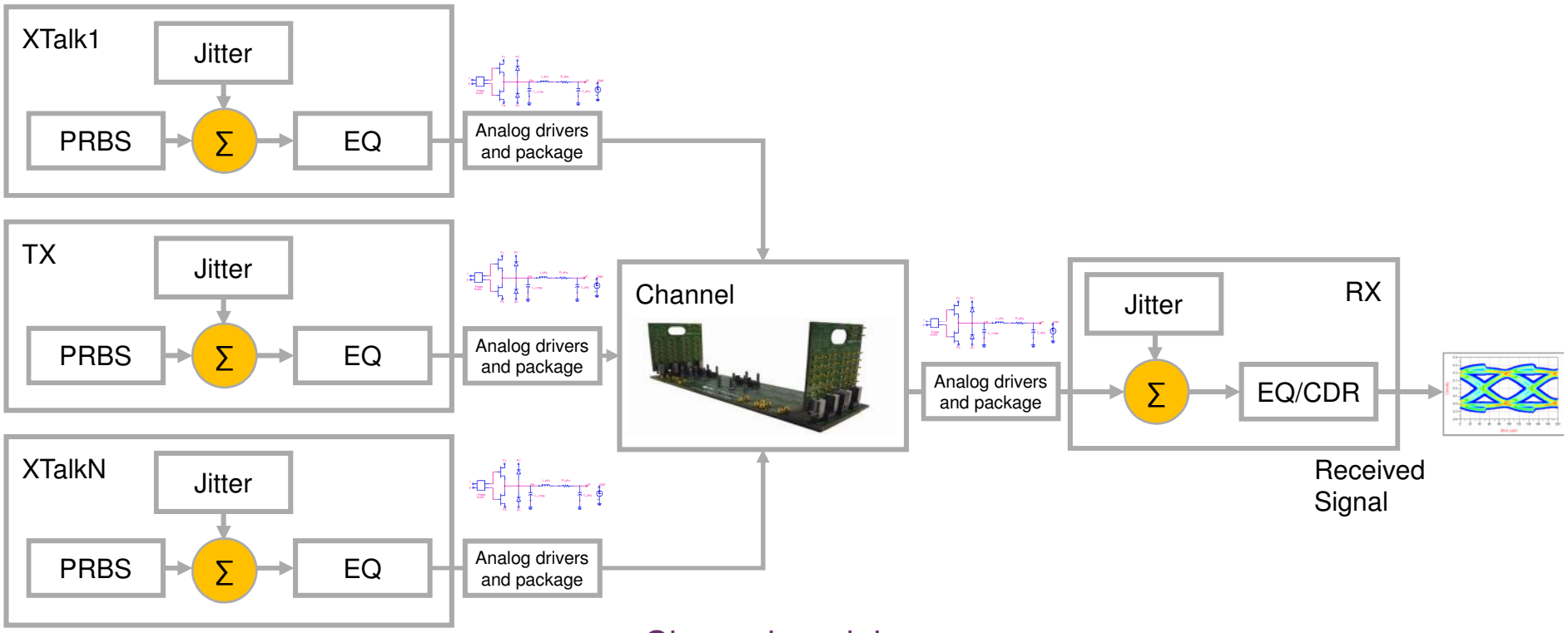
- Must use a channel simulator, not transient simulator (SPICE)
  - …although channel simulator can call other simulators (transient, EM) for generalized channel characterization
- In version 5.0, channel must be linear and time invariant (LTI)
  - …although this restriction is being lifted in a future version to accommodate re-drivers, re-timers etc. (e.g. BIRD 133)
- Non-linear time varying Tx and Rx must be expressed as compiled C code with a specific API
- *.dll or *.so is OS-specific
- Fixed topology
  - …although channel can be made of any arbitrary lumped or distributed elements (if LTI)
- Patching machine code into simulator, not parsing lang.





KEYSIGHT TECHNOLOGIES

What Do the Two New Files Represent?



*.ami and *.dll files

*.ibs files

Channel model in ADS lumped and distributed components

*.ibs files

Rx *.ami and *.dll files

KEYSIGHT TECHNOLOGIES

AMI Model Generation Barriers

#1 AMI modeling barrier
Model Generation Time

AMI Modeling suppose to Speed-up System Design Cycle,
BUT, Model-generation takes Significant Time & Resources

….System Vendors have to wait a LONG time before accurate AMI models become available

Note: Vendors with NO experience in AMI modeling are spending 6-12+ months to come up with first-generation models

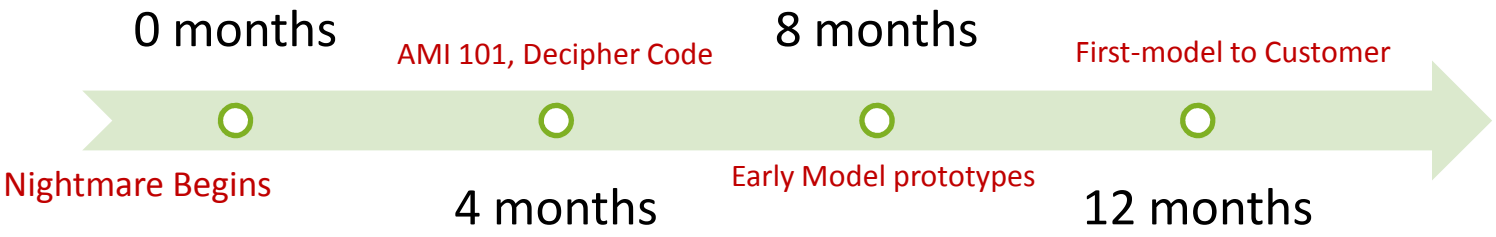
Models come very late in Design Cycle → used only for Validation, NOT Design

Why AMI-model generation takes so long?

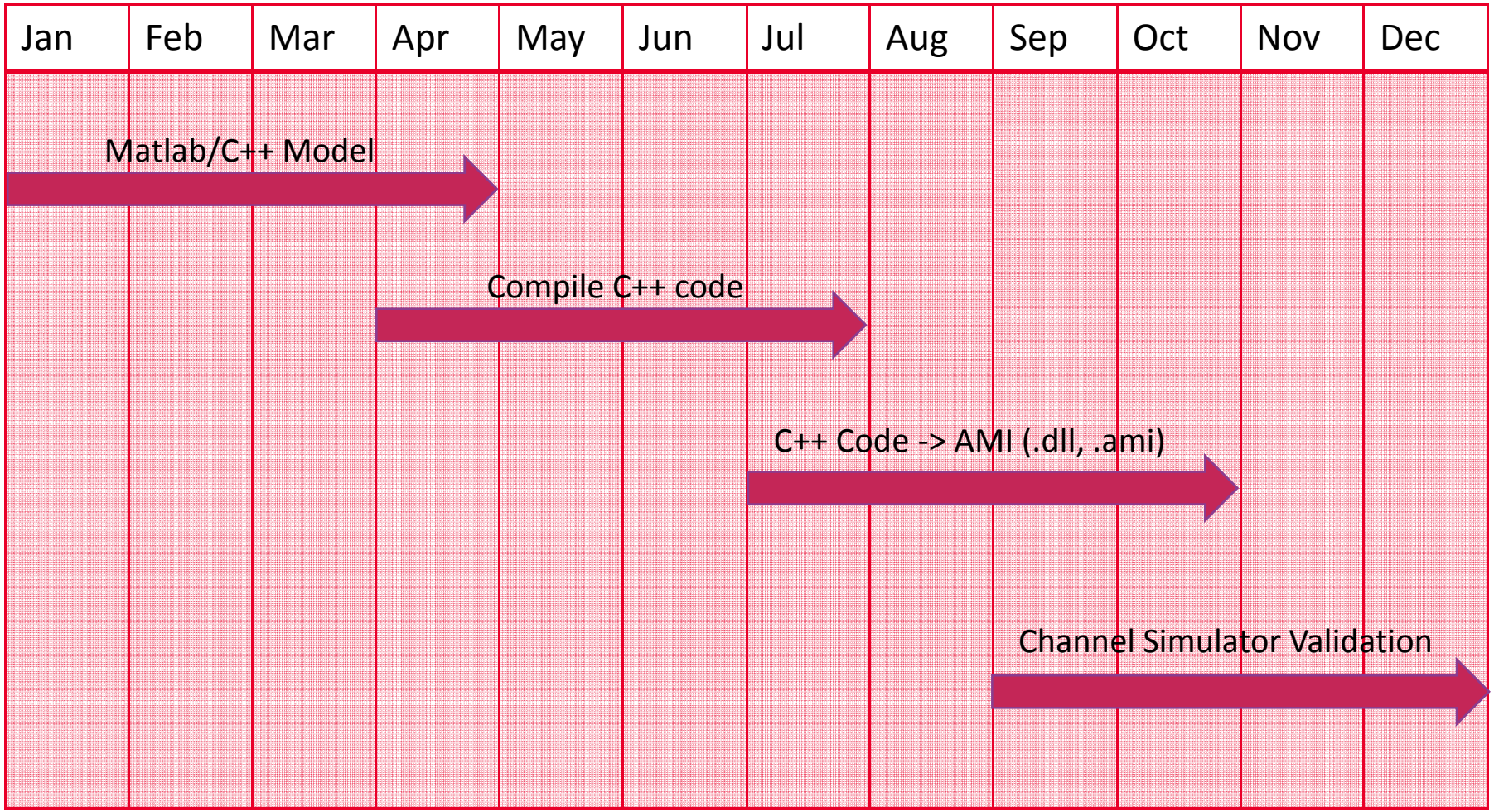
Typical Signal Integrity Engineers are NOT programmers

….they are having “Nightmares” in trying to develop AMI models

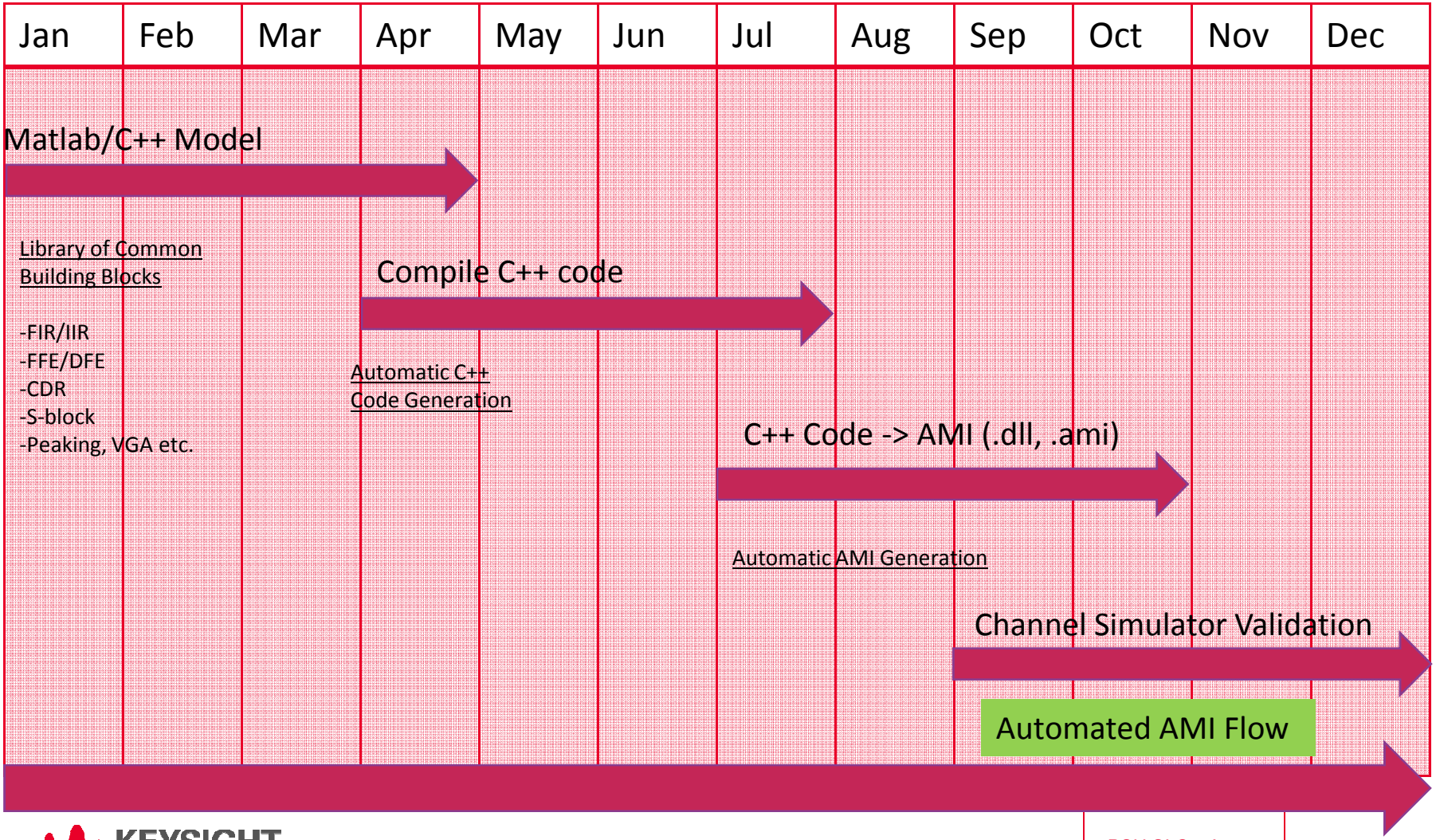
- Cryptic Matlab/C++ code passed from System-Architectures → AMI Modeler (if lucky)
- Challenge to Convert Algorithm design Code → AMI format



Typical AMI model generation flow…



Automated AMI model generation flow…

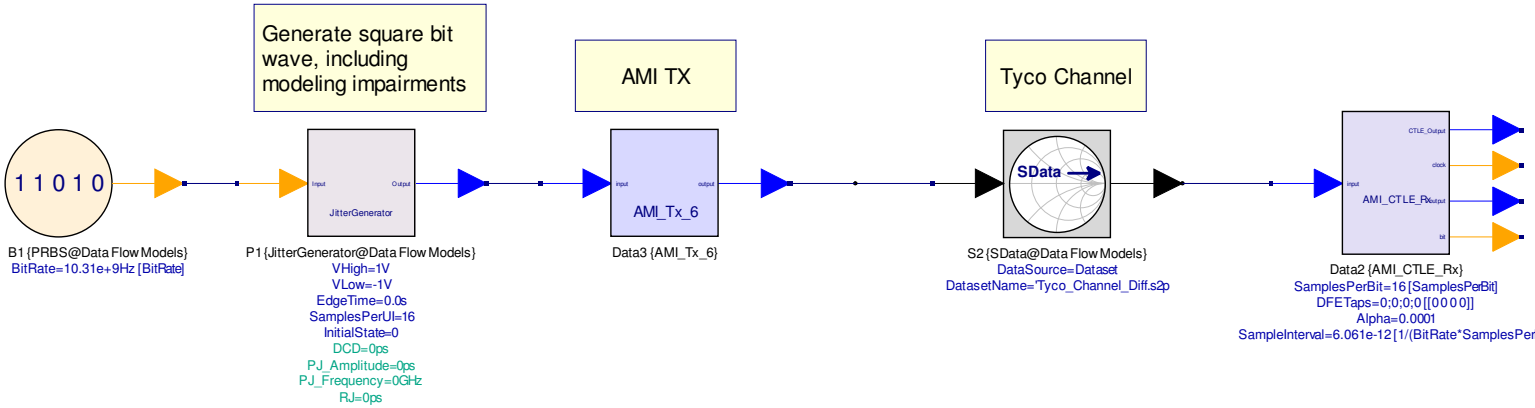


ESL flow for Automated AMI Modeling

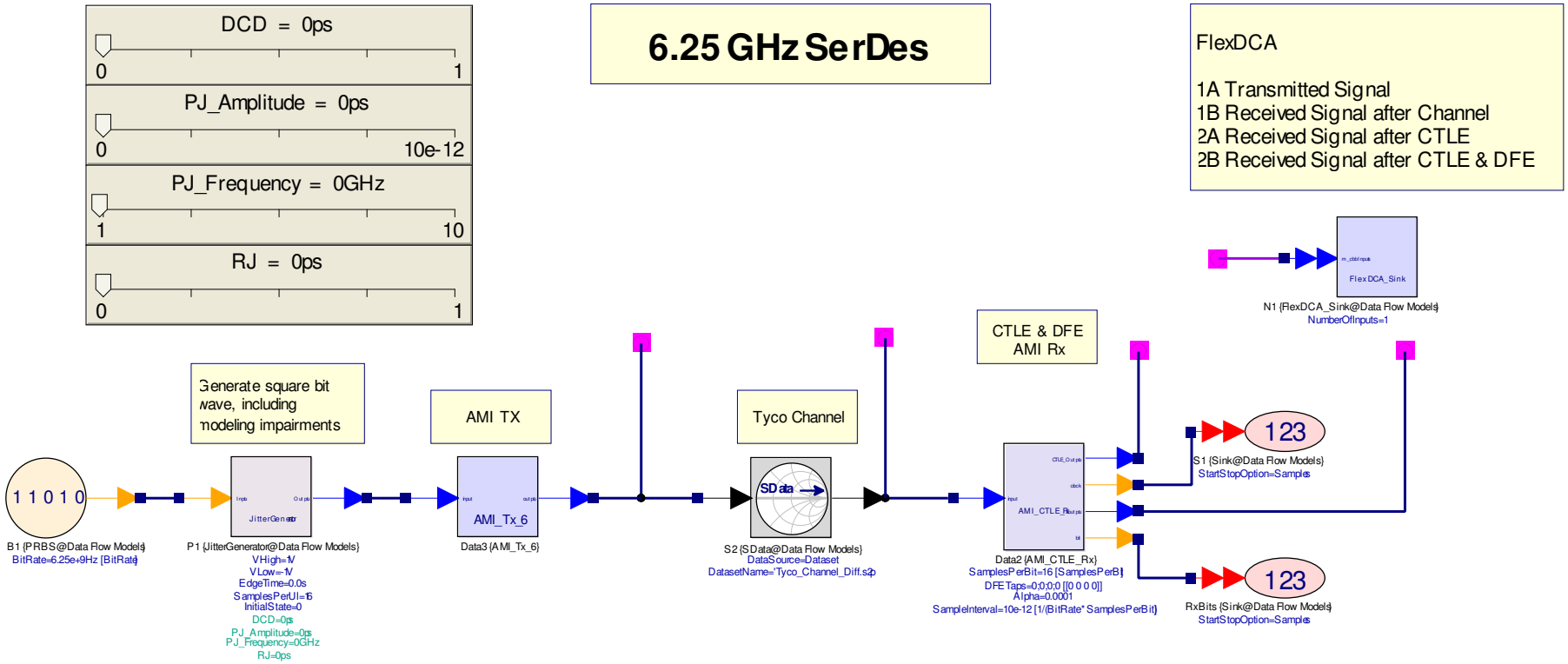
Electronic System Level (**ESL**) design and verification is an emerging electronic design methodology that focuses on the *higher abstraction* level concerns first and foremost.

ESL flow facilitates utilization of appropriate abstractions in order to *increase comprehension about a system*, and to enhance the probability of a successful implementation of functionality in a *cost-effective* manner

Here is an Example of SerDes modeling in SystemVue:

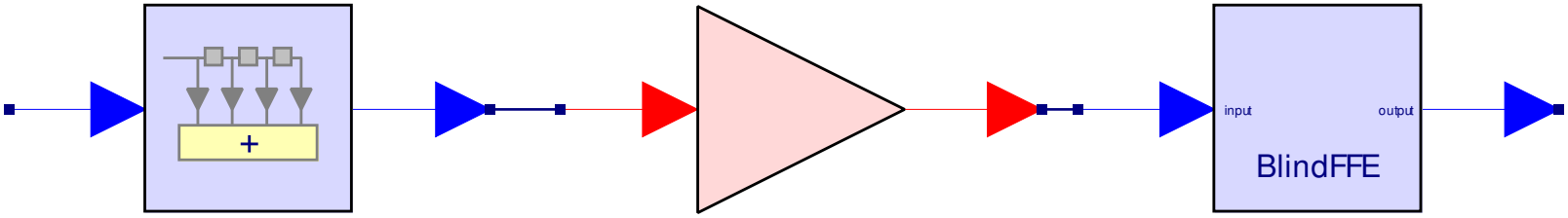


Example
6.0 Gb/s (SATA 3.0)



TX Modeling
6.0 Gb/s (SATA 3.0)

Step-1: Architecture Design of Tx with built-in models



S1 {TimeResponseFIR@Data Flow Models}
ResponseType=Step Response
Response=Real Array (46x1)
ResponseTimeStamps=Real Array (46x1)
TimeStep=1e-12 [sample_interval]

FIR filter

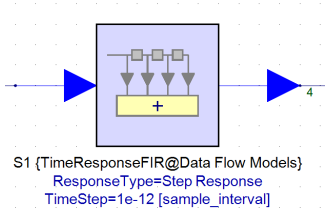
G1 {Gain@Data Flow Models}
Gain=1 [Gain]

B2 {BlindFFE@Data Flow Models}
Coefficients=0;1;0 [Taps]
SamplesPerBit=16 [SamplesPerBit]

3-tap FFE

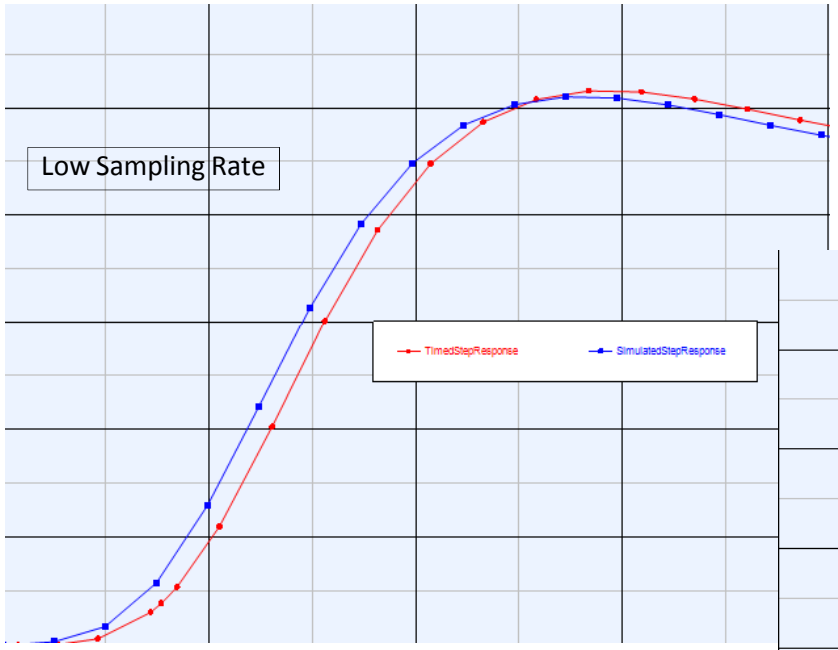
Note: The BlindFFE in the example has 3 implementations: built in C++ model, M code, and compiled M code. Use the manage model list to select the different ones. The example workspace has instructions to load the compiled M code model. See the slides for SV2: C++ Model Builder more information on the compile M code model.

TimeReponseFIR Filter enables importing HSpice or measured data

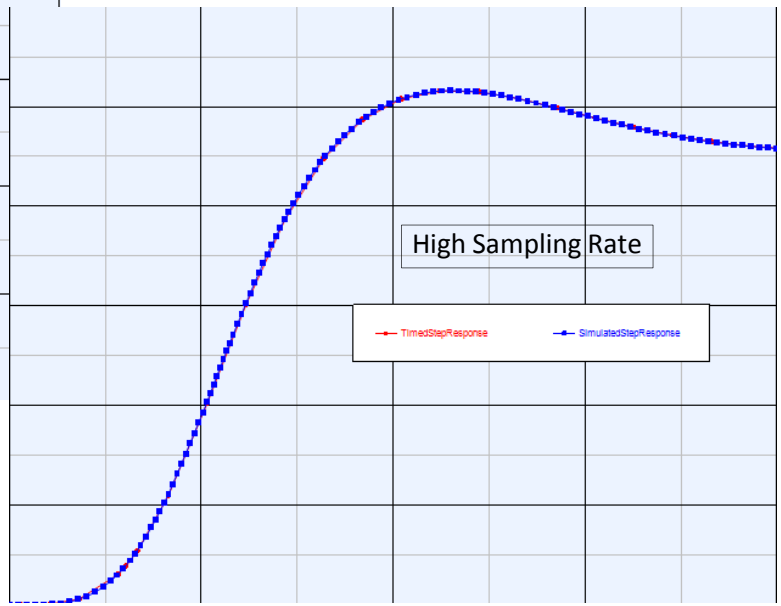


Challenges:

1. Typical Simulation and Measured Data is not equally time-stepped



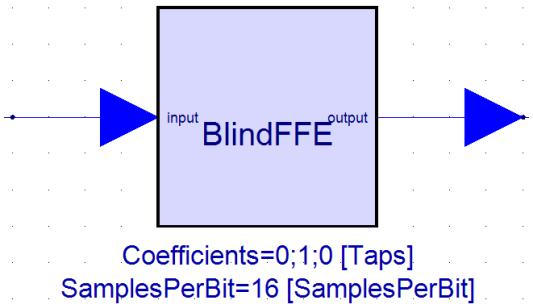
Sampling Rate determines Simulation Accuracy



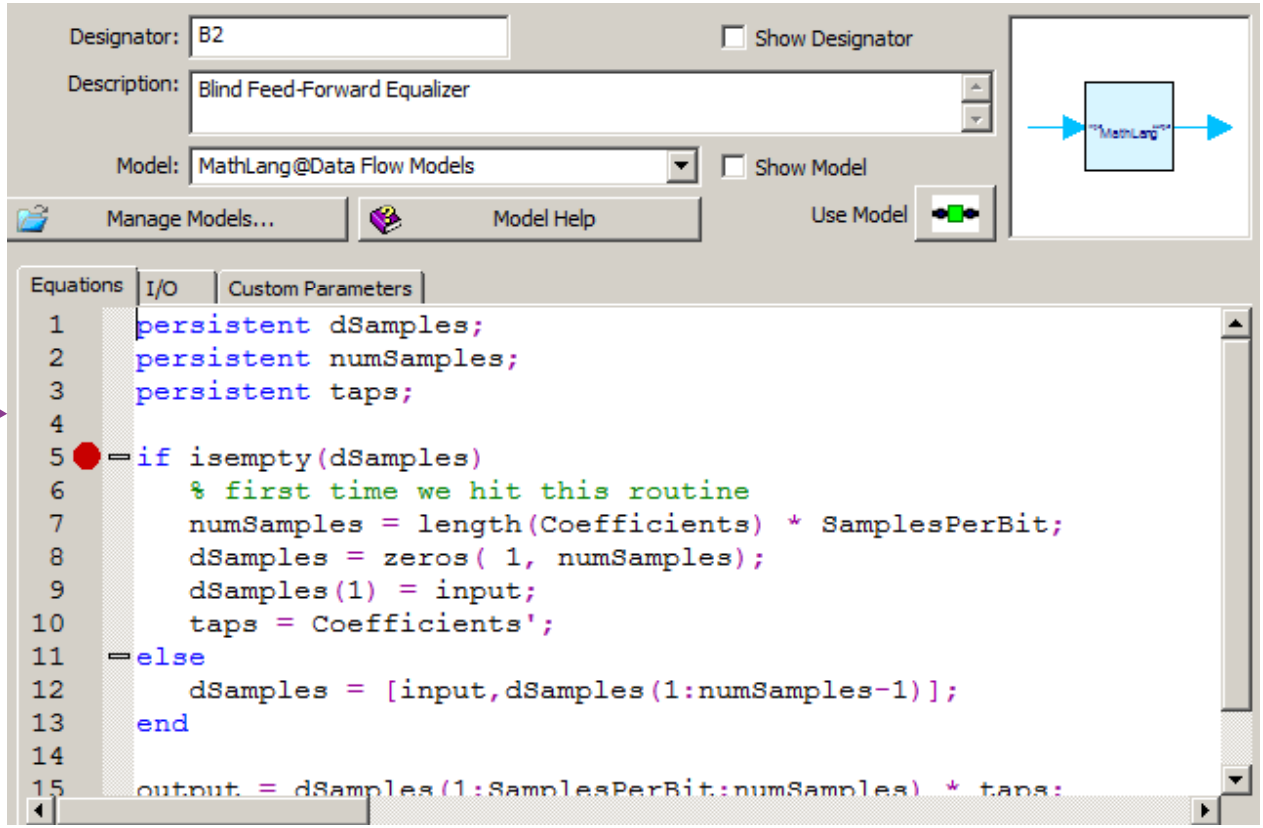
FIR model should support "Arbitrary" Sampling Rate

ESL flow: TX Modeling Example (2)

Step-2: Customize IP -> Bring in Matlab, mathlang, or C++ Code

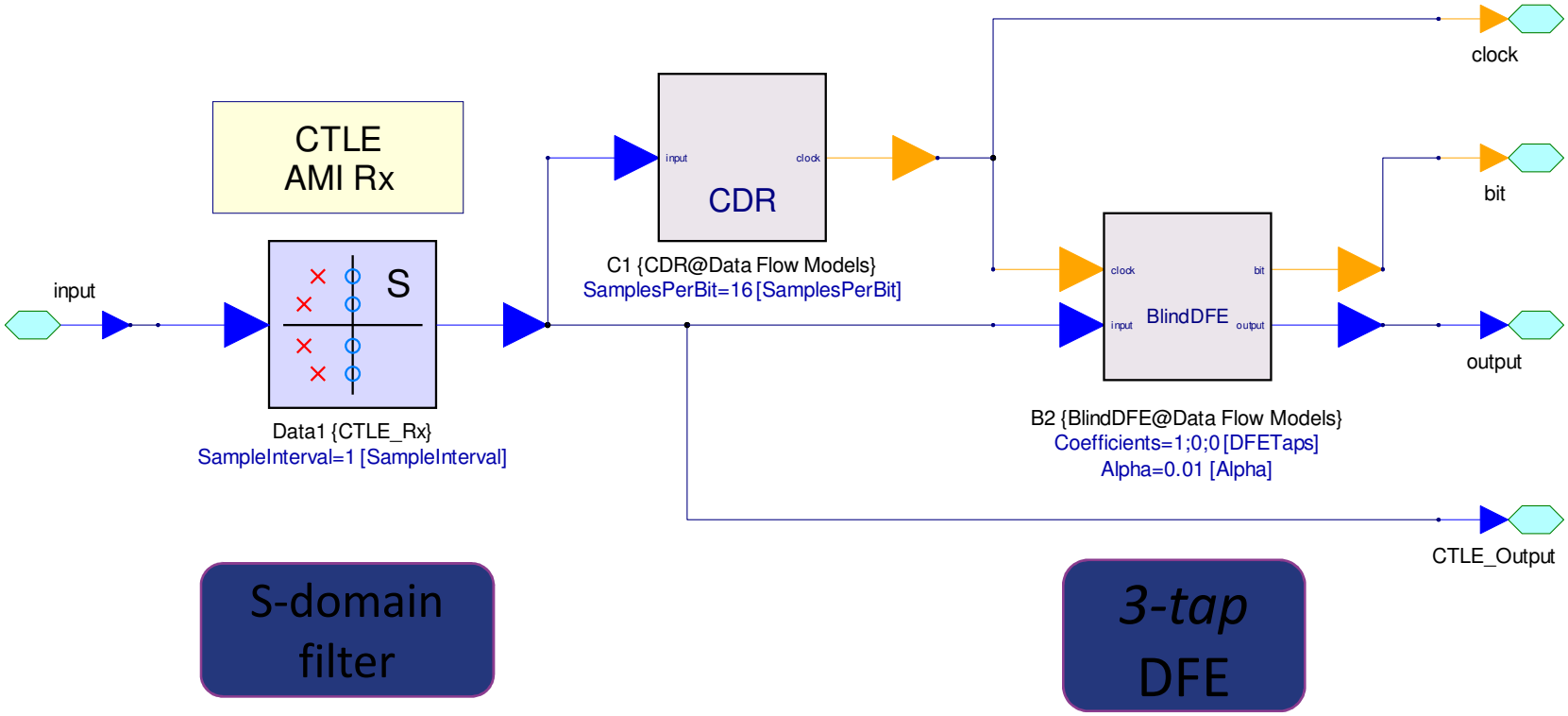


Fine-tune and Customize models with Math Lang and/or C++ code



RX Modeling
6.0 Gb/s (SATA 3.0)

Step-3: Architecture Design of Rx with built-in models



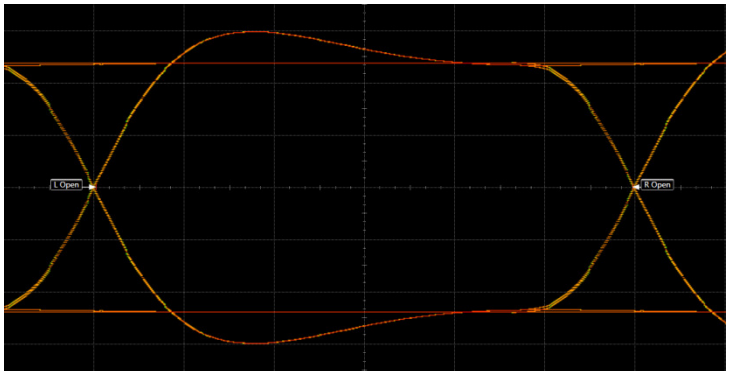
Note: The CTLE design used here is the one detailed in the EDN article: "Continuous-time equalizers improve high-speed serial links". The CDR in this implementation is simple and provides a useful C++ model template to import a custom C++ CDR code. A second Rx design is provided that implements a more realistic CDR (use manage models list on top-level to select).

Results – Displayed in Agilent FlexDCA

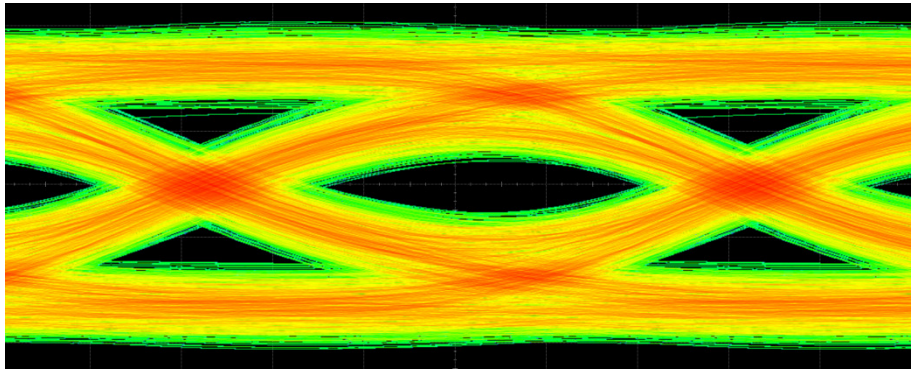
6.0 Gb/s (SATA 3.0)

Step-4: Verify design using Agilent FlexDCA

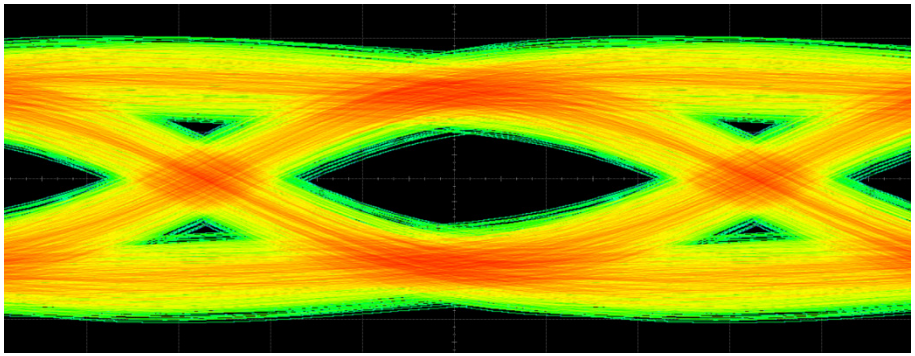
TX Output



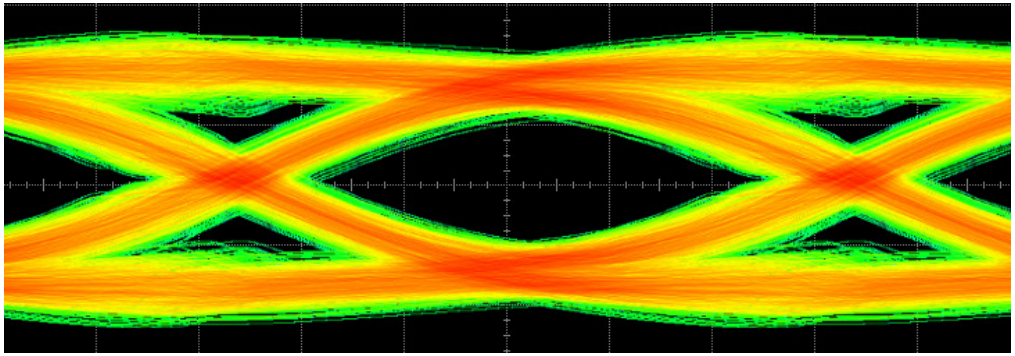
After Channel



After CTLE EQ

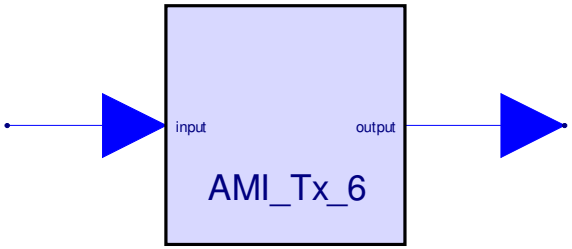


After CTLE+DFE EQ



Note: FlexDCA Eye and Oscilloscope Modes are included as part of base SystemVue product! Separate installation is required.

One-click AMI Code-Generation

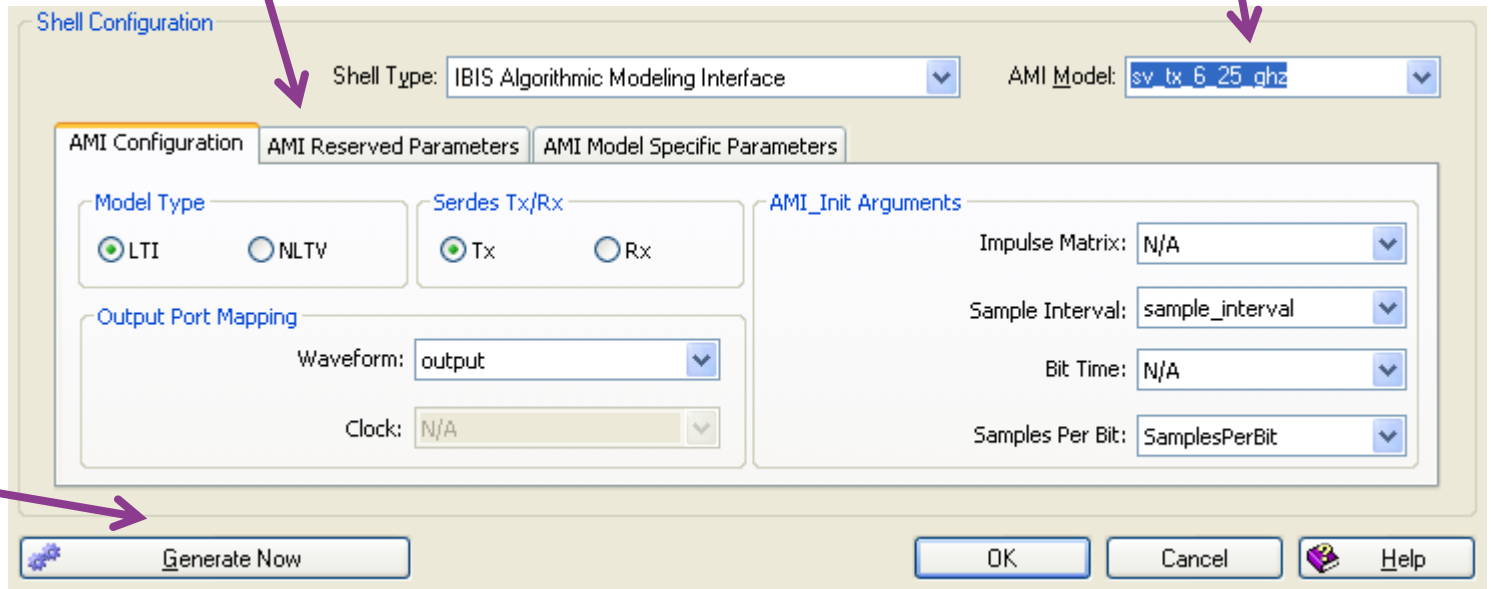


Data3 {AMI_Tx_6}

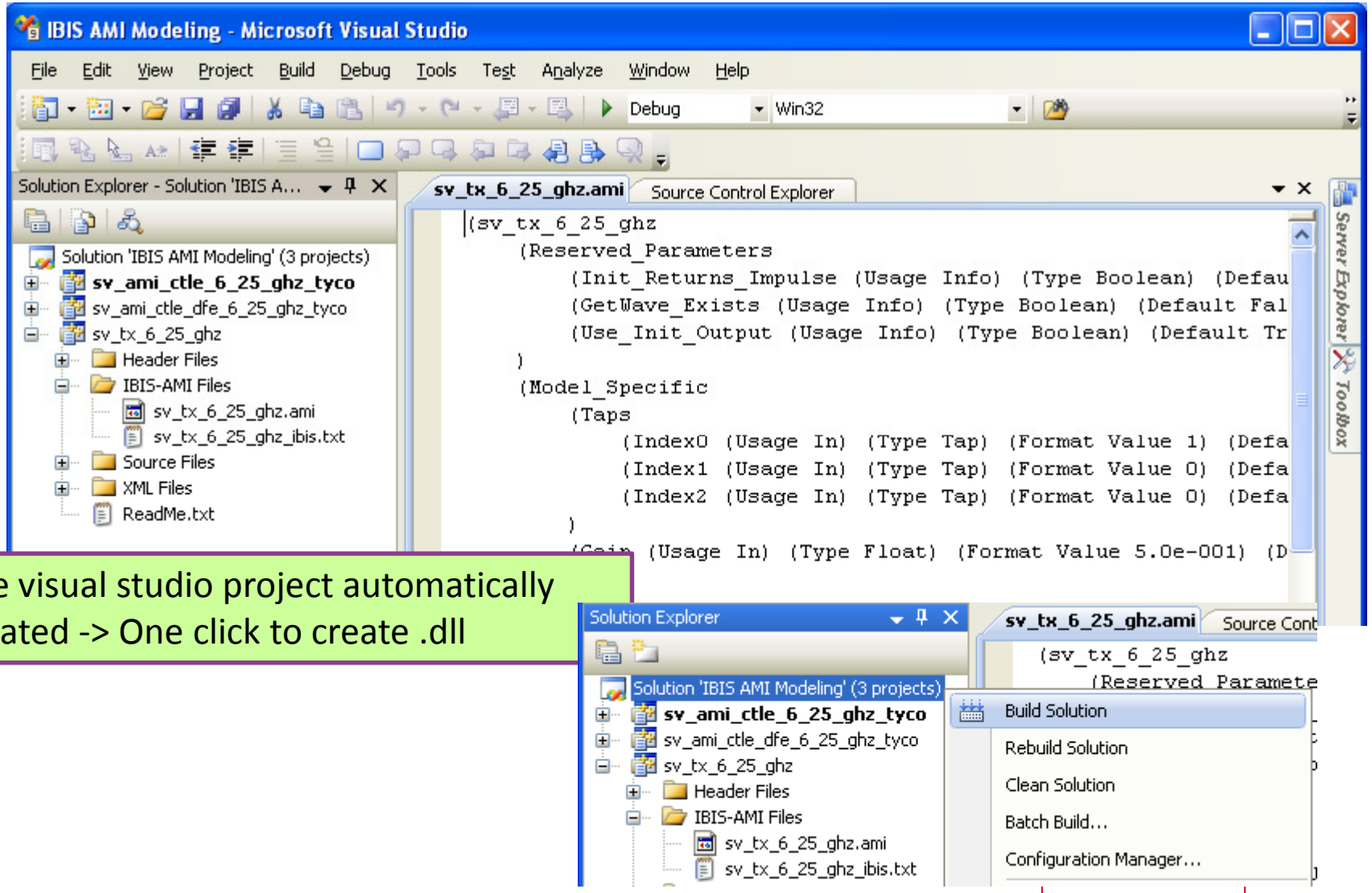
Step-5: Configure AMI models and generate models with one click.

Define Reserved and Model Specific Parameters -> Automatically configure appropriate AMI wrapper

One-click AMI Code-generation



Automatically generated .ami and Visual-Studio project



The visual studio project automatically created -> One click to create .dll

Benefits of ESL Design Flow

Automated AMI-Model Generation

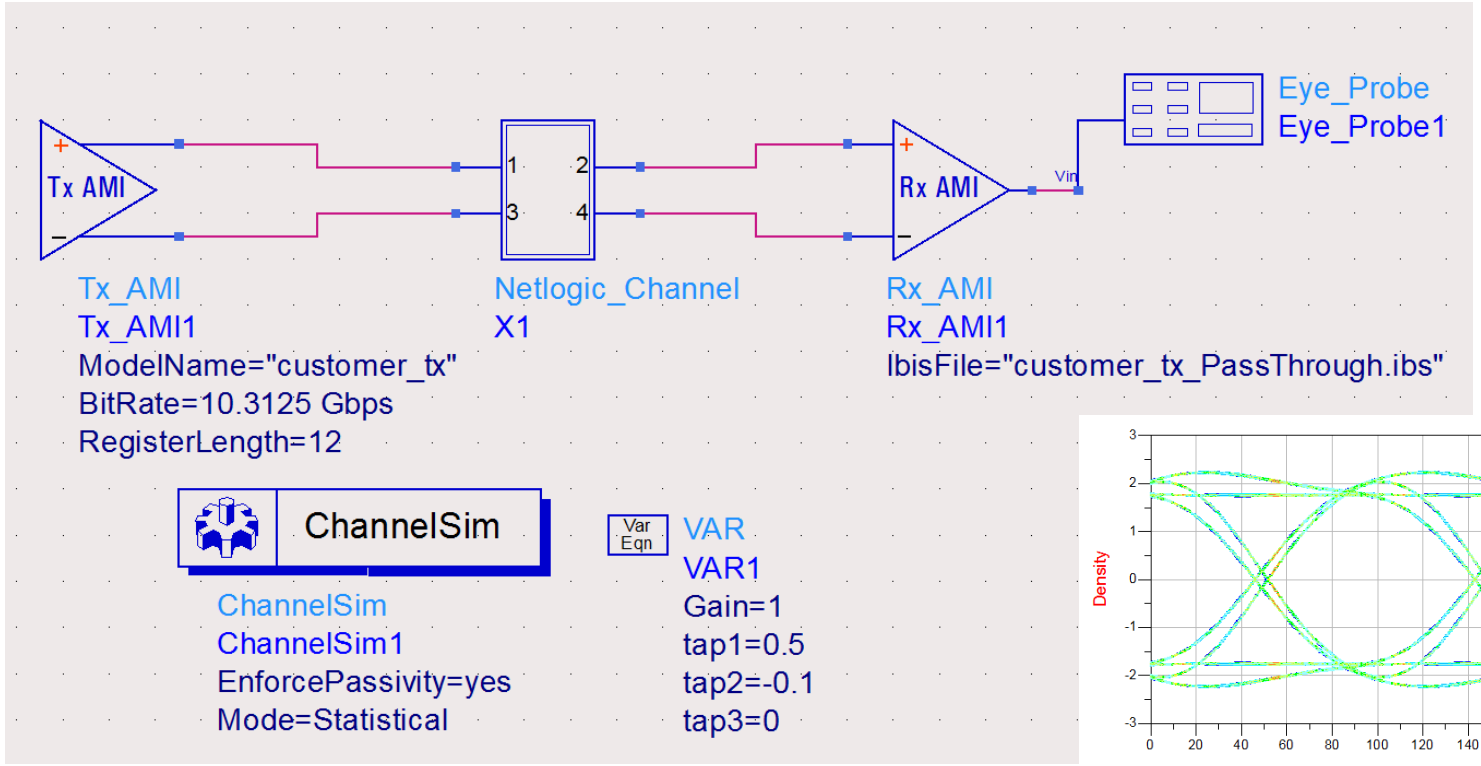
1. Complete “Automation” of Code-generation and Model Compilation
   a task that routinely takes months because of its complexity

2. Basic building blocks that can used to start model development
   FIR/IIR filters, FFE, DFE, CDR etc.

3. Easily customize models to include custom IP
   Custom C++ and Matlab

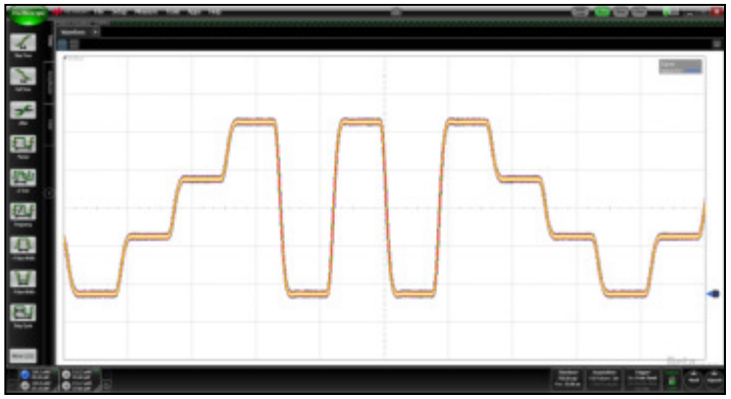
Validating AMI-Model in ADS Channel Simulator

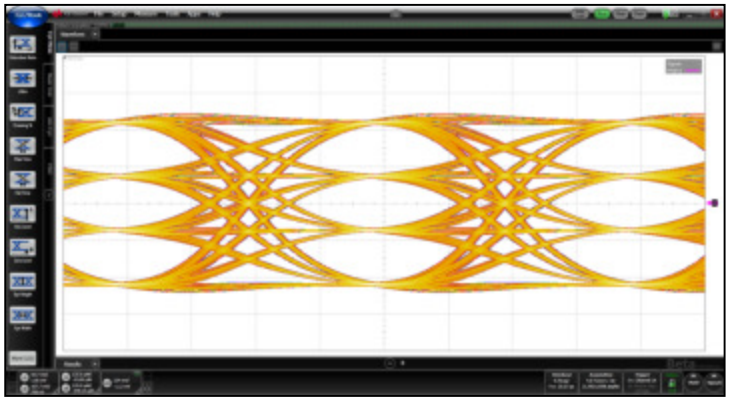
1. Verify generated AMI models in ADS.
2. Generated AMI models support all IBIS-5.0 compliant channel simulators.2.



Keysight Education Forum

Simulation and Characterization of PAM-4 signals in 28G and 56G Designs using IBIS-AMI models





KEYSIGHT TECHNOLOGIES

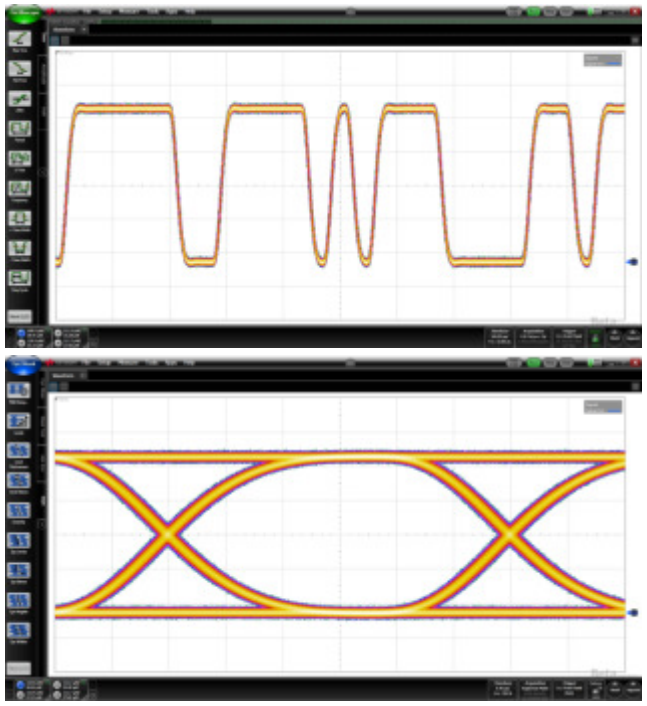
Simulation and Characterization of PAM-4 signals in 28G and 56G Designs using IBIS-AMI models

- Overview: Pulse Amplitude Module (PAM-4)
- PAM-4 End-to-End Link Simulation
- PAM-4 TX Characterization
- Summary
- Q&A

KEYSIGHT TECHNOLOGIES

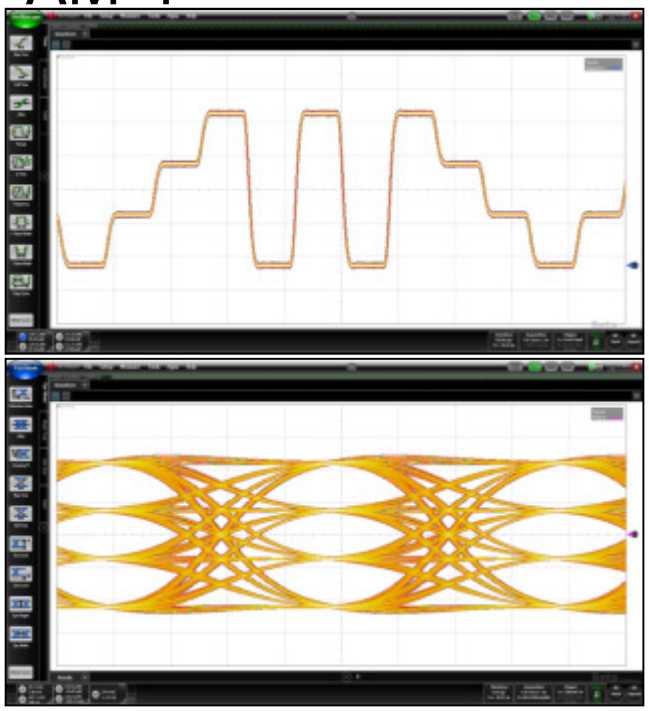
NRZ (Non-Return-to-Zero) **vs. PAM** (Pulse Amplitude Modulation)

NRZ (PAM-2)



- 2 amplitude levels
- 1 bit of information in every symbol

PAM-4



- 4 amplitude levels
- 2 bits of information in every symbol
  - ✓ 2x throughput for the same Baud rate
  - ✓ 28 GBaud PAM-4 = 56 Gb/s
- Lower SNR, more susceptible to noise
- More complex TX/RX design, higher cost

KEYSIGHT TECHNOLOGIES

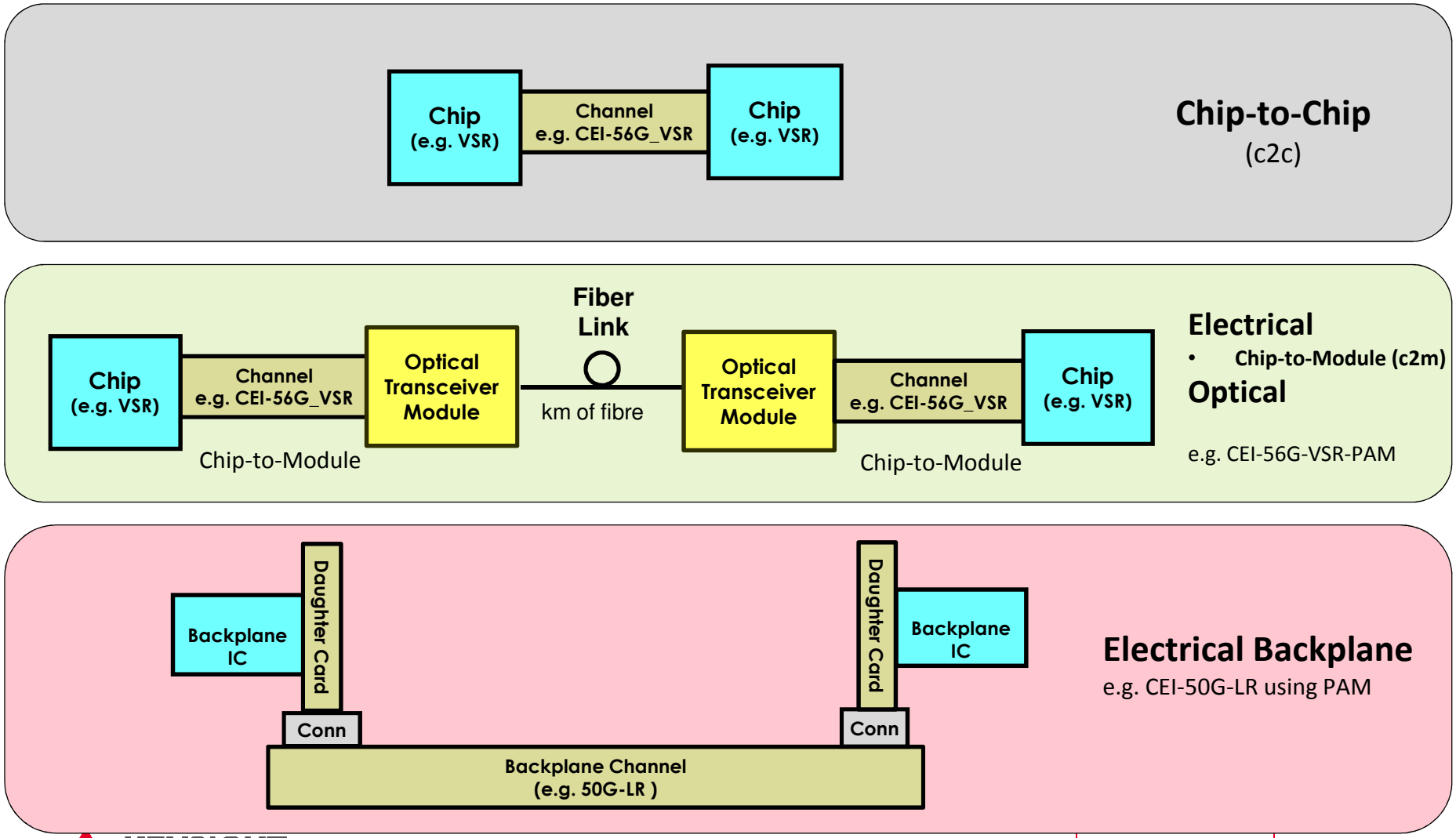
Status of Standards using PAM-4

- **Implemented**
  - IEEE 802.3bj clause 94 (25.78 Gb/s as 13.6 GBaud PAM-4 in 1m backplane)
    - Low adoption rate – limited advantages over clause 93 – 25.78 G NRZ
- **Under development/discussion**
  - OIF CEI 4.0 (56G-VSR, MR, LR)
    - 28 GBaud using PAM-4
    - Basis for other standards – Ethernet, Fiber Channel, Infiniband, ...

    Note - 56 GBaud NRZ for Ultra Short Reach applications
  - IEEE 802.3bs
    - PAM-4 Proposals being discussed to support 400 GbE Chip-to-Chip (c2c) and Chip-to-Module (c2m)
    - PAM-4 to work on existing CAUI-4 (100G) infrastructures
  - 64G Fibre Channel

Typical PAM-4 Communication Systems

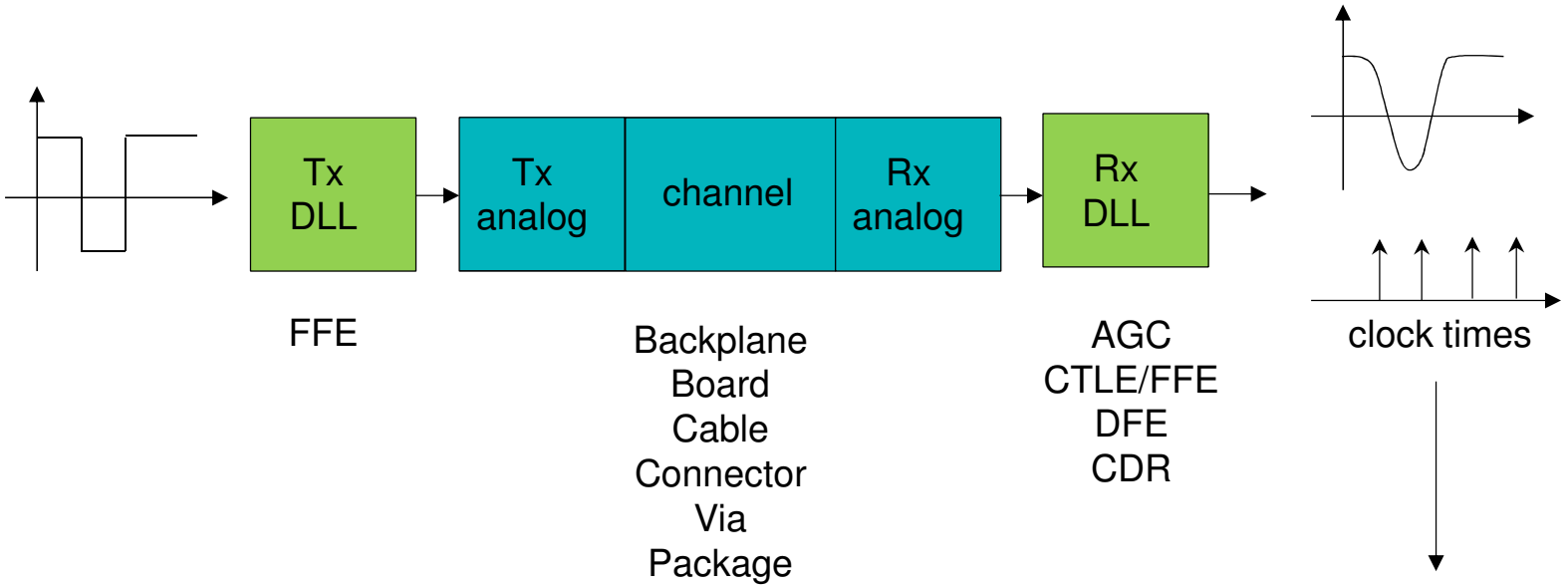
Transmitter, Channel, Receiver

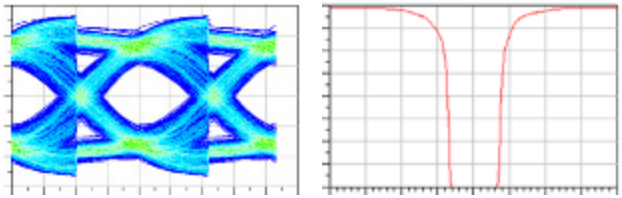


AMI-based End-to-end Link Simulation

- At 56 Gb/s equalization and clock-data-recovery are indispensable
  - Tx: FFE
  - Rx: CTLE/FFE, DFE, CDR
- Full channel analyses must account for both passive channel characteristics and SerDes functionalities
- AMI behavioral models are provided by IC vendors to model SerDes operations
- AMI successfully brings SerDes vendors' models and EDA tools together
  - **Interoperability**: AMI defines a common interface between SerDes model and simulator
  - **IP protection**: SerDes behavior is concealed in model DLL
- AMI has been widely adopted by IC, system and EDA companies

AMI Simulation Flow for NRZ





simulated by vendor supplied AMI model DLL

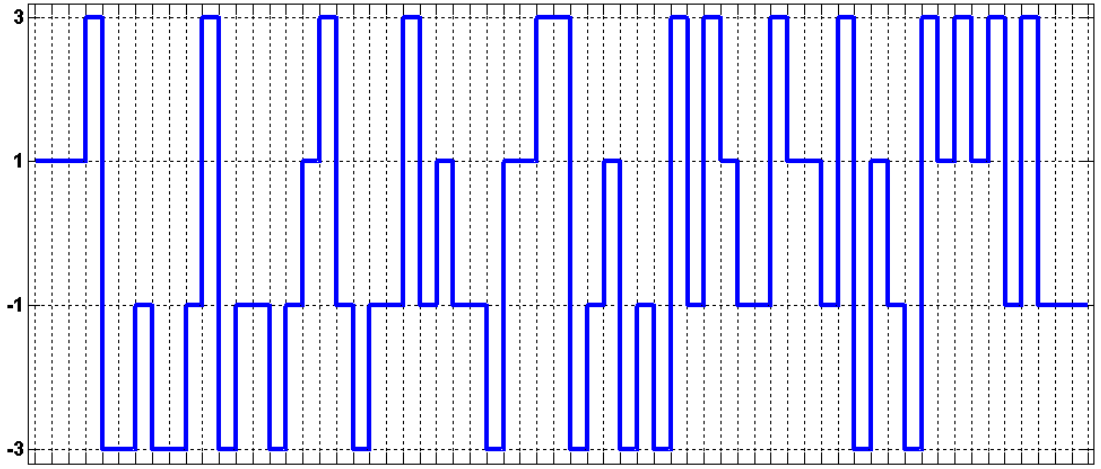
simulated by EDA tool

AMI Modeling for PAM4 Signaling: Tx

– For NRZ, input stimulus to Tx DLL has two levels, representing 1 and 0 bits

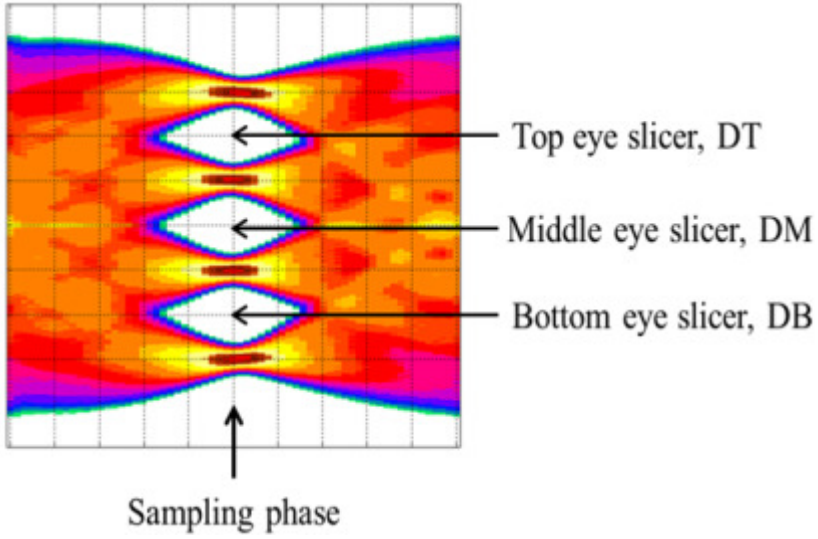
– For PAM4, input to Tx DLL needs to have four levels, representing symbols 3, 1, -1 and -3 (or 3, 2, 1 and 0 in other convention)

– Tx DLL interface is unchanged in PAM4



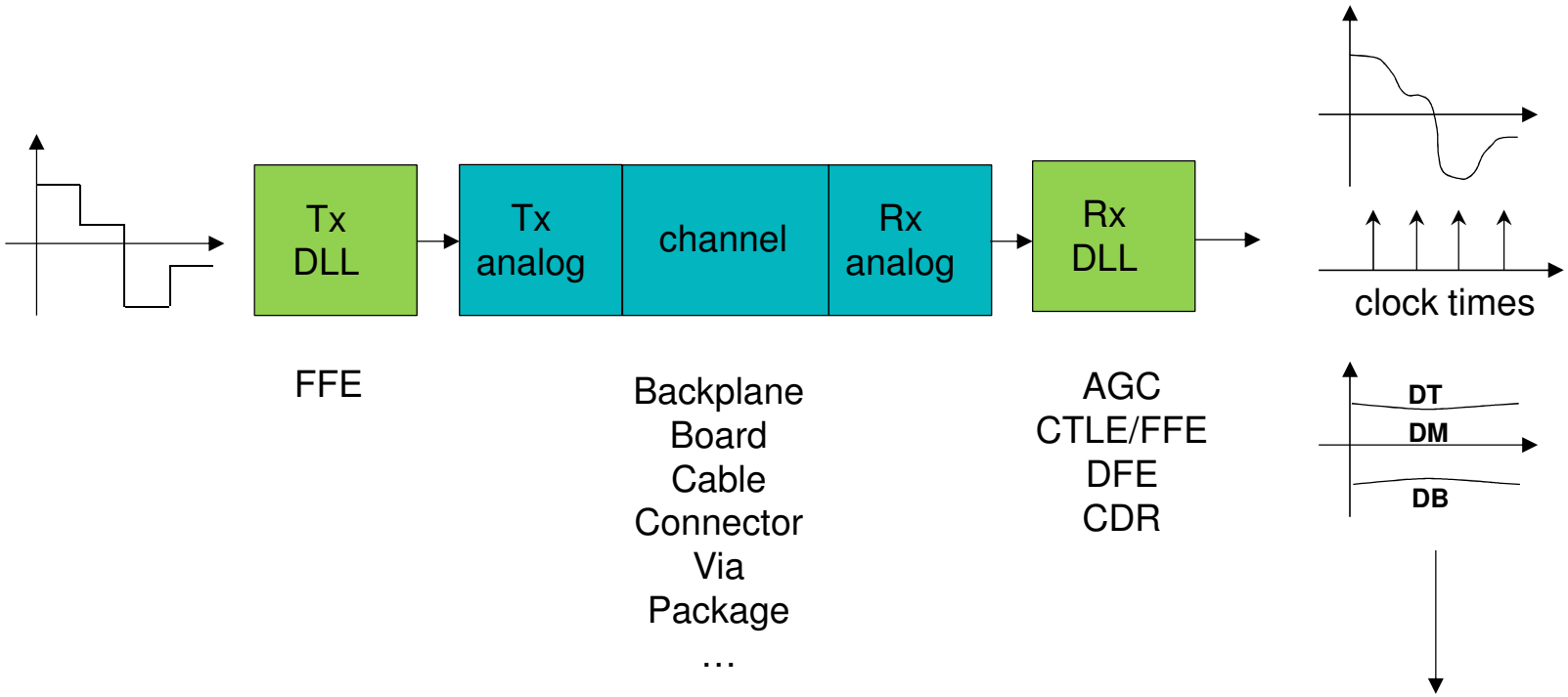
AMI Modeling for PAM4 Signaling: Rx

- PAM4 Rx symbol decision relies on three slicers
- Slicer reference levels are adjusted adaptively and can vary with time
- Rx DLL needs to provide transient slicer levels (DT, DM and DB) to simulator for SER calculation



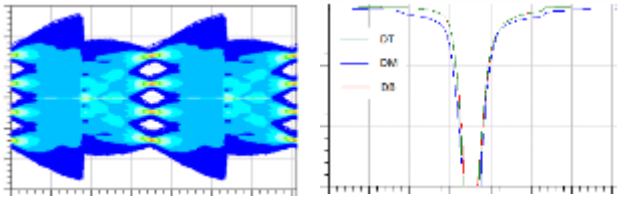
Note: models for ADC based Rx need to hypothetically oversample to generate output waveform

AMI Simulation Flow for PAM4



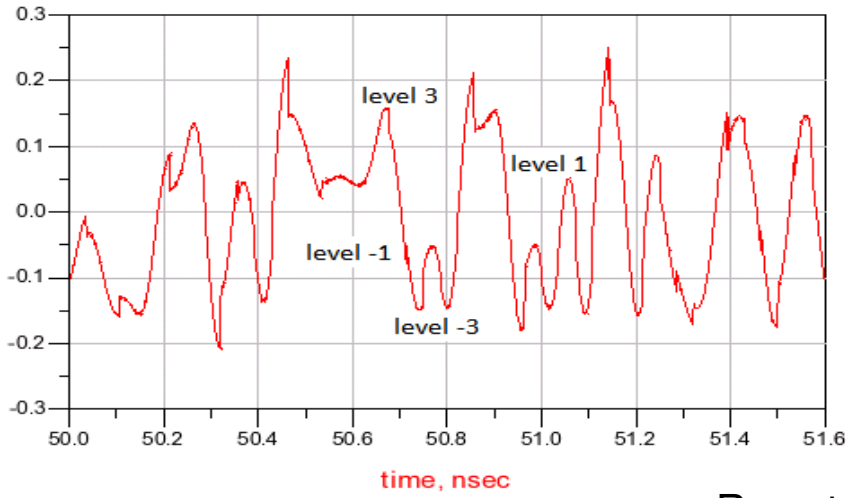
simulated by vendor supplied AMI model DLL

simulated by EDA tool

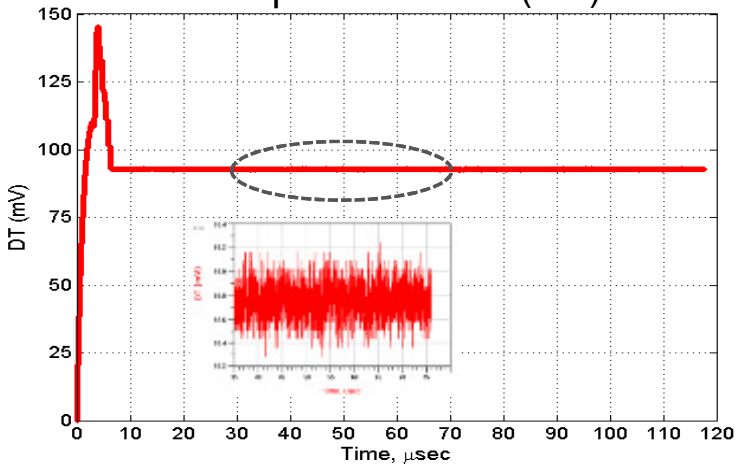


Example

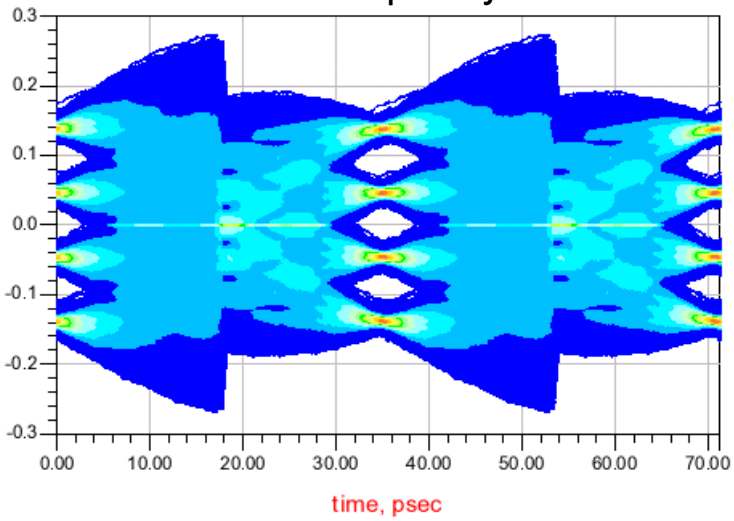
Rx DLL output signal



Rx top slicer level (DT)



Rx output eye



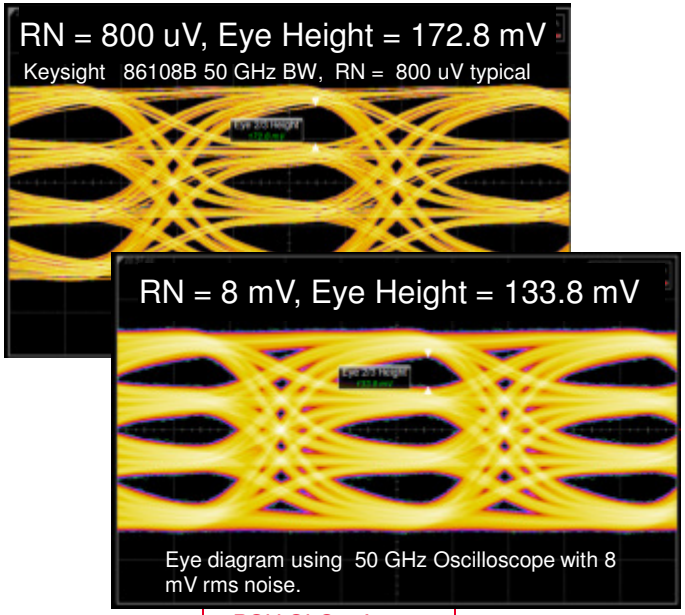
PAM-4 Measurement Challenges

- **Clock Recovery (CR) – used to track out low-frequency jitter, trigger the scope**
  - Real-time oscilloscopes use software CR
    - New SW algorithms required.
  - Sampling oscilloscopes use hardware CR
    - Existing Keysight HW clock recovery designs work on PAM-4 signals

- **Noise**
  - Noise will reduce eye opening and degrade system BER
  - Random Noise (RN) from DUT TX will Root Sum Square (RSS) add to intrinsic RN from the scope\
  - Slower edge speeds (slew rate, S) exacerbate the issue due to AM-to-PM conversion

$$\text{Jitter}_{rms} = \frac{RN_{rms}}{S}$$

  - Sampling oscilloscopes offer the lowest noise solution for a given bandwidth
    (often 5-10x lower than a real-time scope that has equivalent BW)



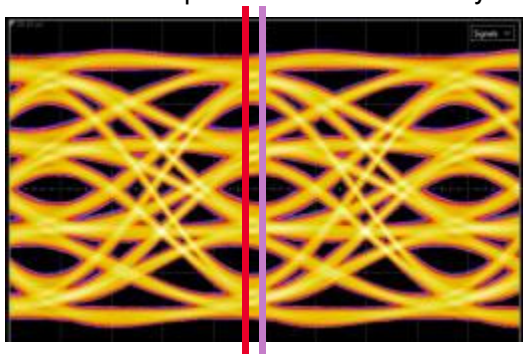
KEYSIGHT TECHNOLOGIES

Impairments that challenge PAM-4 receivers

– Eye Skew

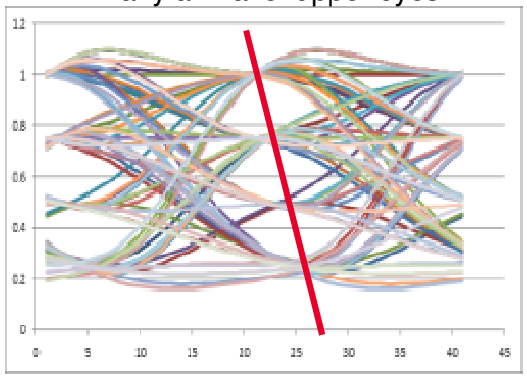
- Electrical Considerations
  - Example: Skew introduced due to misalignment of two NRZ patterns during PAM-4 generation
    - Top and bottom eyes are skewed relative to middle eye
  - Standards to check alignment of middle eye relative to upper and lower eyes

Skew between top/bottom and middle eyes



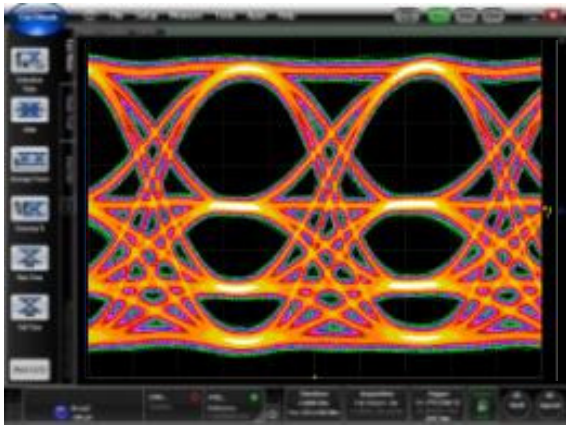
- Optical Considerations
  - Eye time skew from linear drive of VCSELs (optical)
    - Upper eyes arrive sooner than lower transitions
    - Will each eye need to be sampled with independent delay? More complex RX design.

Early arrival of upper eyes



Other impairments that challenge PAM-4 receivers

- Non-linearity - Amplitude compression in lower eyes
  - Non uniform effective SNR across individual eyes

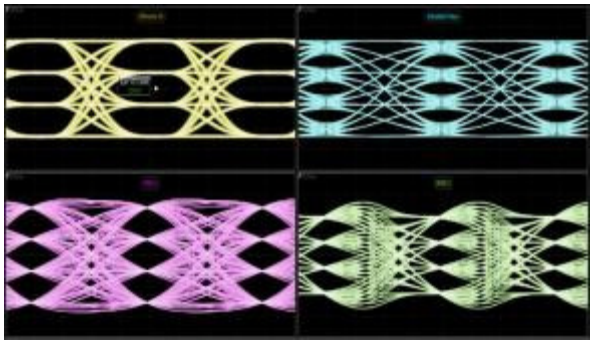


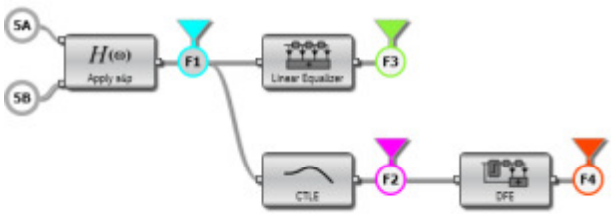
– Receivers sensitive to additional artifacts beyond “traditional” jitter types in NRZ

- Still learning what impairments cause problems
  - New measurements WILL be defined for Tx Outputs
  - New stress types WILL be defined for Rx Input testing

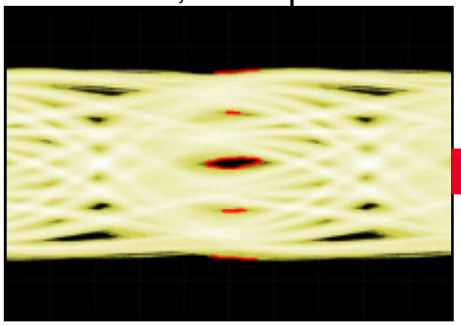
Other Measurement Considerations

- **Equalization**
  - Receiver equalization required to open eyes, allow RX to apply Forward Error Correction (FEC)
  - Some combination of:
    - Linear Feedforward Equalizer (FFE/LFE)
    - Continuous Time Linear Equalizer (CTLE)
    - Decision Feedback Equalizer (DFE)





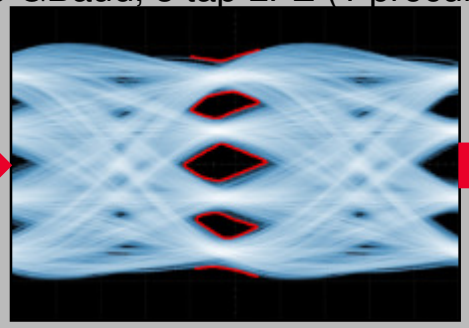
30 Gbaud, No equalization



RX input

Receiver

30 GBaud, 3 tap LFE (1 precursor)



Apply FEC to correct bit errors.

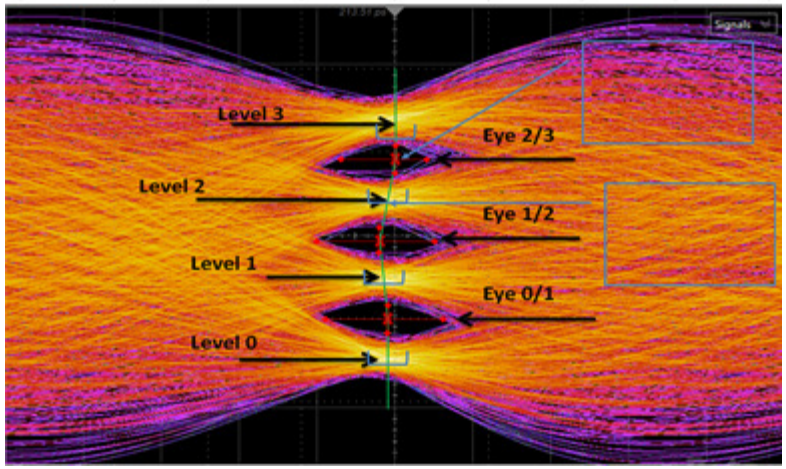
QPRBS13 – Eye Measurements

Quaternary PRBS13 Test Pattern

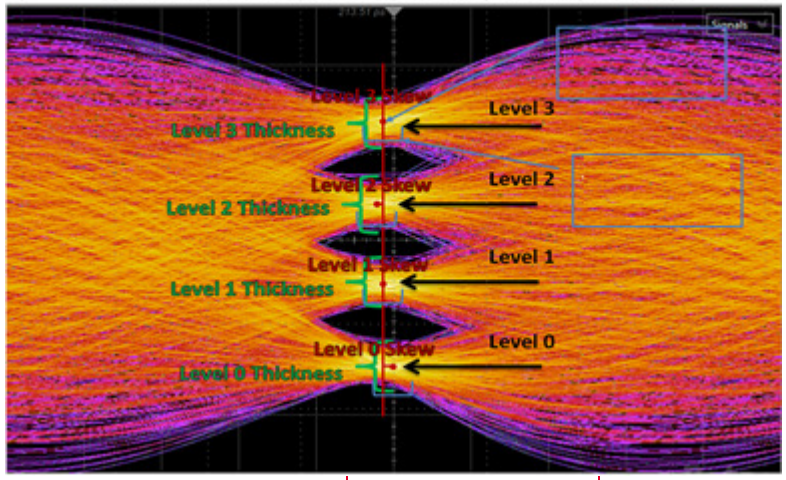
– Types of EYE-based measurements:
  - Eye Height
  - Eye Width
  - Eye Skew
  - EW and EH likely to be specified at a relatively high probability (e.g. EW @ 1E-6)

  - Level – mean, “thickness”, and skew at the points of minimum ISI.

Eye Centric Measurements



Level Centric Measurements



PAM-N 86100D DCA-X: Hardware Test Solutions

Electrical and Optical solutions to 32 Gbaud (contact Keysight for 56 Gbaud solutions)

Electrical – Highest Precision

(includes built-in clock recovery and precision timebase)

Keysight 86100D DCA-X with 86108B

- Channels: 2
- Bandwidth: 50 GHz
- Jitter: <45 fs rms typ.
- Electrical Clock Recovery – integrated HW Clock Recovery works with PAM-N signals up to 32 Gbaud

Note - PAM software works with any DCA module (optical and electrical)

Optical (add Electrical/TDR remote heads)

Keysight 86100D DCA-X with 86105D-281

- Channels: Up to 2 optical per module, 8 electrical
- Bandwidth: 34 GHz (optical), 60 GHz (electrical)
- Jitter: < 85 fs rms typ. (with 86100D-PTB)
- N1070A Optical Clock Recovery (external)
  - 32 Gbaud Single Mode
  - 14 Gbaud Multimode
- Electrical Remote Heads
  - N1045A 60 GHz Electrical Only
  - N1055A 50 GHz Electrical with TDR/TDT

KEYSIGHT TECHNOLOGIES

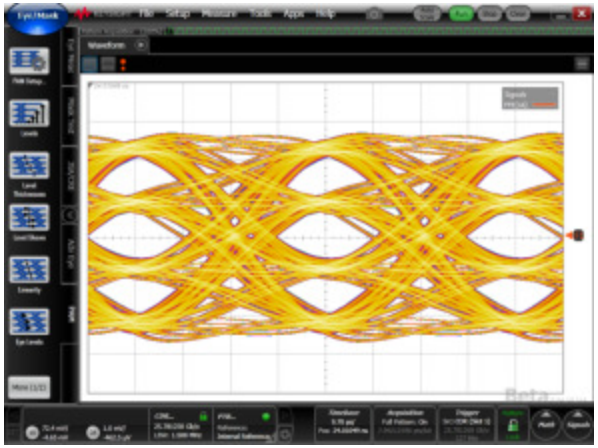
Summary (IBIS-AMI)

- AMI Modeling (SystemVue + premium services)
  - **Industry's only** ESL flow for SerDes design space exploration and IBIS AMI model generation
- Verification in ADS lets you **integrate** IBIS AMI simulation with circuits, layouts, Full wave 3DEM integration and EM Co-simulation (FEM and FDTD) for chip-to-chip link optimization

Summary (PAM-4)

– Several industry groups and standards bodies are using, or are actively considering using, PAM-4 technology

- Switch from NRZ to PAM-4 signaling presents many new design and measurement challenges



- Keysight provides powerful solutions for:
  - PAM-4 End-to-End Link Simulation
  - PAM-4 TX Characterization
  - PAM-4 RX Characterization

KEYSIGHT TECHNOLOGIES